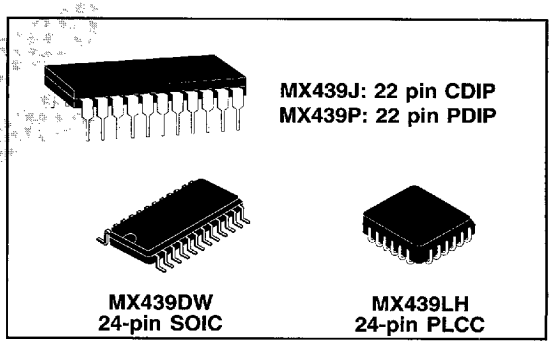
MSK MODEM

FEATURES

- 1200 Baud MSK Modem
- Meets Cellular & Trunked Radio Specifications
- Full-Duplex 1200 Baud
- On-Chip RX and TX Bandpass Filters
- Clock Recovery and Carrier Detect
- Pin Selectable Xtal/Clock Frequencies

APPLICATIONS

- Mobile & Cellular Radio Data Signaling
- Personal Radio
- Portable Data Terminals
- General Purpose Applications



DESCRIPTION

The MX439 is a single-chip CMOS LSI circuit which operates as a 1200 baud MSK modem. The mark and space frequencies are 1200Hz and 1800Hz phase continuous, and the frequency transitions occur at the zero crossing point. The transmitter and receiver will work independently, thus providing full-duplex operation at 1200 baud. The baud rate, transmit mark and space frequencies, and the TX and RX synchronization are all derived from a highly stable Xtal oscillator. The on-chip oscillator is capable of working at one of two input frequencies: 1.008MHz or 4.032MHz external Xtal/clock input. Frequency is pin-selectable with the "Clock Rate" logic input. The device includes circuitry for carrier detect and facility for the RX clock recovery. An on-board switched capacitor 900Hz - 2100Hz bandpass filter provides optimum carrier filtering. The use of switched capacitor analog filters and digital signal processing results in excellent dynamic performance with few external components; the CMOS process and current-saving techniques offer low standby supply current for portable battery-powered applications.

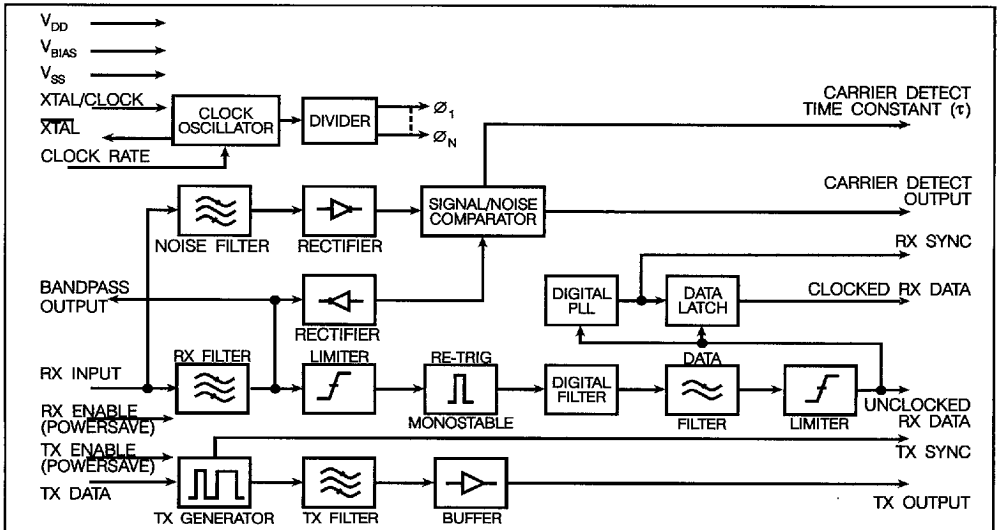


Figure 1 - Internal Block Diagram

PIN FUNCTION TABLE

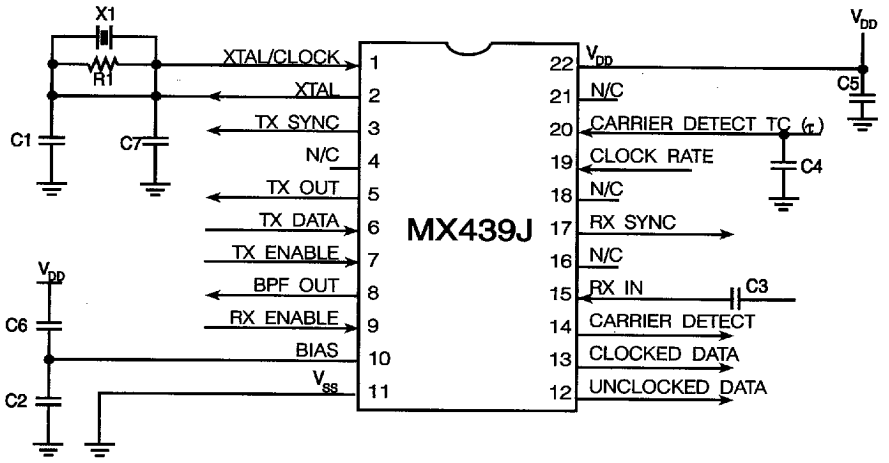
Pin DW	Pin J,P	Pin LH	Function
1	1	1	Xtal/Clock: The input to an on-chip inverter for use with either a 1.008MHz or a 4.032MHz Xtal. Alternatively, an external clock may be used. Xtal frequency is selectable on the "Clock Rate" input pin.
2	2	2	$\overline{\text{Xtal}}$: Output of the on-chip inverter. (See Figure 2.)
3	3	3	TX Sync O/P: MSK signal centered at a DC level of V_{BIAS} - 0.7V. (See Figure 5.)
5	5	5	TX Signal O/P: With the transmitter disabled, this pin is set to a high impedance state. When the transmitter is enabled, this pin outputs the 1200/1800Hz MSK signal centered at a DC level of V_{BIAS} - 0.7 V. (See Figure 5.)
7	6	7	TX Data I/P: Serial logic data to be transmitted is input to this pin and synchronized by the "TX Sync O/P." (See Figure 5.)
8	7	8	$\overline{\text{TX Enable}}$: A logic "1" applied to this input will put the transmitter into powersave while forcing "TX Sync O/P" to a logic "1" and "TX Signal O/P" to a high impedance state. A logic "0" will enable the transmitter (See Figure 5). This pin is internally pulled to V_{DD}.
9	8	9	Bandpass O/P: This is the output of the RX 900Hz-2100Hz bandpass filter. The output impedance of this pin is typically 10kΩ and may require buffering prior to use.
10	9	10	RX Enable: This is the control of the RX function. The state of other outputs is given below:
11	10	11	Bias: Provides bias internally and should be decoupled externally to V_{ss} by capacitor (C_2). (See Fig. 2.)
12	11	12	V_{ss}: Negative supply rail (GND).
13	12	13	Unclocked Data O/P: This pin outputs recovered asynchronous serial data from the receiver.
14	13	14	Clocked Data O/P: This pin outputs recovered synchronous serial data from the receiver and is internally latched out by a recovered clock appearing on the "RX Sync O/P" pin. (See Figure 6.)
15	14	15	Carrier Detect O/P: This pin will output a logic "1" when an MSK signal is being received.
16	15	16	RX Signal I/P: This is the MSK signal input for the receiver. It should be decoupled using capacitor C_3.
18	17	18	RX Sync O/P: This is a flywheel 1200Hz squarewave output which, upon presentation of the MSK data signal, is synchronized internally to the incoming data. (See Figure 6.)

RX Enable	RX Function	Clock Data O/P	Carrier Detect	RX Sync Out
"1"	Enabled	Enabled	Enabled	Enabled
"0"	Powersave	"0"	"0"	"1" or "0"

When both TX and RX functions are disabled, the bias voltage is switched internally to V_{SS} and Bias pin output impedance is approximately 12.5kΩ. When the Bias pin is decoupled by a 1.0μF capacitor (C2) the MX439 may require up to 25ms to establish correct operation after enabling the RX function. This period may be decreased by either reducing the value of C2, lowering the Bias pin impedance externally, or adopting a different powersaving strategy (such as using C2 and C5 and supplying V_{DD} via a series switch). This pin is internally pulled to V_{DD}.

Pin			Function
DW	J,P	LH	
21	19	21	Clock Rate: This logic input selects and allows the use of either a 1.008MHz or 4.032MHz Xtal/clock input to the on-chip inverter. Logic "1" = 4.032MHz; logic "0" = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
22	20	22	Carrier Detect Time Constant (τ): This input forms part of the carrier detect integration function. The value of C_4 connected to this pin will affect the carrier detect response time and hence noise performance. (See Figure 2, Note 3.)
24	22	24	V_{DD}: Positive supply rail. A single 5 volt supply is required.
4,6,17 19,20 23	4,16, 18,21	4,6,17 19,20, 23	No Connection.

Note: Output Loading. Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of (typically) 100Ω put in series with the load should minimize this effect.



Component References	
Component	Value
R1	1M
C1	33p
C2	1.0µ
C3	0.1µ
C4	0.1µ
C5	1.0µ
C6	1.0µ
C7	33p
X1	1.008MHz or 4.032 MHz

Tolerances: R = ±10%
C = ±20%

Notes:

1. Bias may be decoupled to V_{SS} and V_{DD} using C2 and C6 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C2 only.
2. Use C5 when input signals are referenced to V_{SS} to decouple V_{DD}.
3. The value of C4 determines the carrier detect time constant. A long time constant results in improved noise immunity but increased response time. C4 may be varied to trade-off response time for noise immunity.
4. The value of C7 reduces XTAL voltage overshoot. Refer to MX-COM's Crystal Oscillator Application Note (see Appendix).
5. X1 can be either a 1.008 MHz or 4.032 MHz crystal, depending on the Clock Rate setting.

Figure 2 - External Component Connections

DIAGRAMS

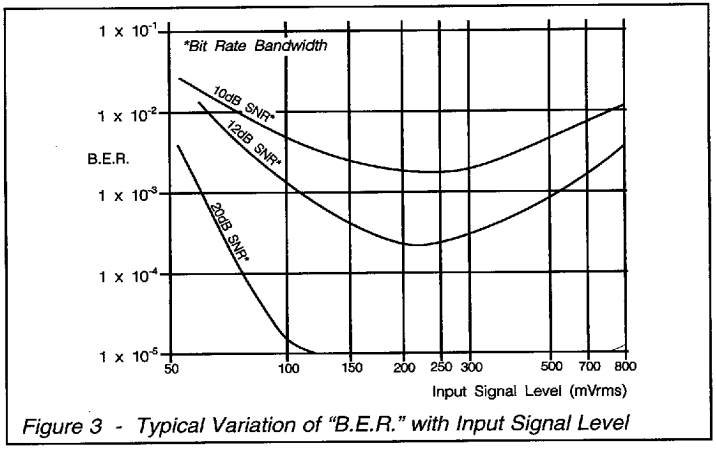


Figure 3 - Typical Variation of "B.E.R." with Input Signal Level

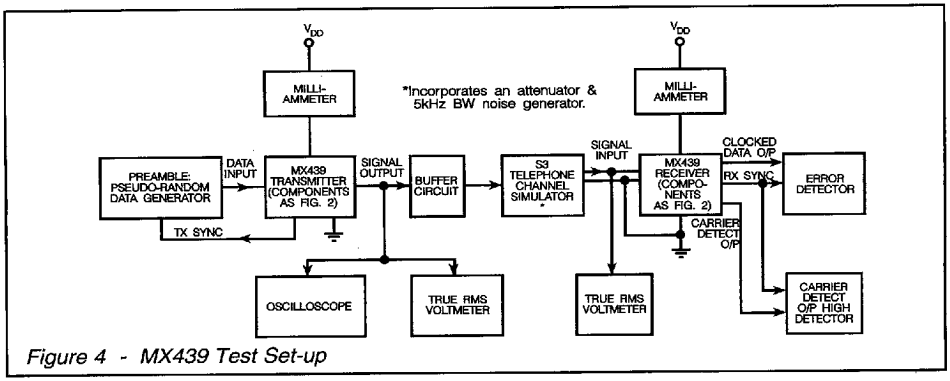
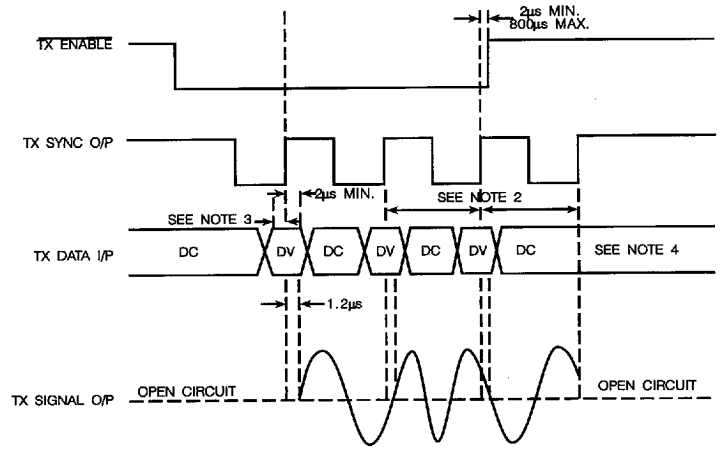


Figure 4 - MX439 Test Set-up



NOTES:

1. All timings are related to the TX SYNC OUTPUT.
2. 0.833ms for 1.008MHz or 4.032MHz Xtal.
3. 2µs min. + crystal tolerance.
4. DC = Don't Care. DV = Data Valid.

Figure 5 - Transmitter Timing Diagram

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (Total)	20mA
Total Device Dissipation @ T_{AMB} = 25°C	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All charactistics are measured using the standard test circuit (Figure 4) with the following test parameters and is valid for all tests unless otherwise stated:

V_{DD} = +5V
T_{AMB} = 25°C
Xtal (X1) Frequency: 1.008MHz
0dB reference = 300 mVrms
Noise (band limited 5kHz gaussian white noise)
SNR ratio measured in bit rate bandwidth (1200Hz)

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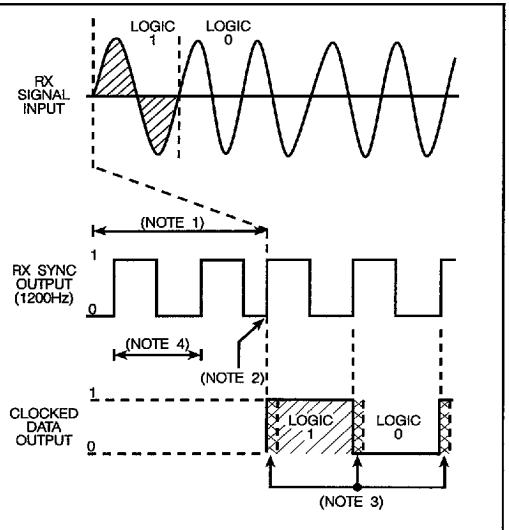
Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Volts		4.5	5.0	5.5	V
Supply Current:					
RX Enabled, TX Disabled		-	3.6	-	mA
RX Enabled, TX Enabled		-	4.5	-	mA
RX Disabled, TX Disabled		-	650	-	µA
Logic "1" level		80%V_{DD}	-	-	V
Logic "0" level	-	-	-	20%V_{DD}	V
Digital Output Impedance		-	4	-	kΩ
Analog and Digital Input Impedance		100	-	-	kΩ
TX Output Impedance		-	10	-	kΩ
On-Chip Crystal Oscillator:					
R_{in}		10	-	-	MΩ
R_{out}		5	-	15	kΩ
Inverter Gain		10	-	20	dB
Gain Bandwidth Product		3×10^6	-	-	
Crystal Frequency	1,9	-	1.008	-	MHz
Crystal Frequency	1,10	-	4.032	-	MHz
Dynamic Values					
Receiver:					
Signal Input: Dynamic Range (50dB SNR)	2,3	100	230	1000	mVrms
Bit Error Rate:					
12dB SNR	3	-	7.0	-	10^{-4}
20dB SNR	3	-	1.0	-	10^{-8}
Receiver Synchronization 12dB SNR:	6				
Probability of Bit 8 being correct			99	-	%
Probability of Bit 16 being correct			99.5	-	%
Carrier Detect	4				
Sensitivity	6,7	-	-	125	mVrms
Probability of Carrier Detect being high:					
12dB SNR after Bit 8	4,8	-	98	-	%
12dB SNR after Bit 16	4,8	-	99.5	-	%
0dB Noise (No Signal)	8	-	5	-	%

Characteristics	See Note	Min.	Typ.	Max.	Unit
Transmitter Output					
TX Output Level		-	775	-	mVrms
Output Level Variation 1200/1800Hz		0	-	±1.00	dB
Output Distortion		-	3	5	%
3rd Harmonic Distortion		-	2	3	%
Logic "1" Carrier Frequency	5	-	1200	-	Hz
Logic "0" Carrier Frequency	5	-	1800	-	Hz
Isochronous Distortion					
1200Hz - 1800Hz		-	25	40	µs
1800Hz - 1200Hz		-	20	40	µs

Notes:
1. Crystal frequency, type and tolerance depends on system requirements.
2. See Figure 3.
3. SNR (Bit Rate Bandwidth).
4. See Figure 2, Note 3.
5. Depending on crystal tolerance.
6. 10101010101... pattern.
7. Measured with 100 mVrms signal (No noise).
8. 0dB level for CD probability measurements is 230mVrms.
9. Clock rate pin at logic "0."
10. Clock rate pin at logic "1."



NOTES:
1. Internal delay typically 1.5ms.
2. From freely running to Sync in 8 data bits (See spec).
3. Undetermined state: 2µs max.
4. Min 800µs, Max. 865µs.

Figure 6 - Receiver Timing Diagram

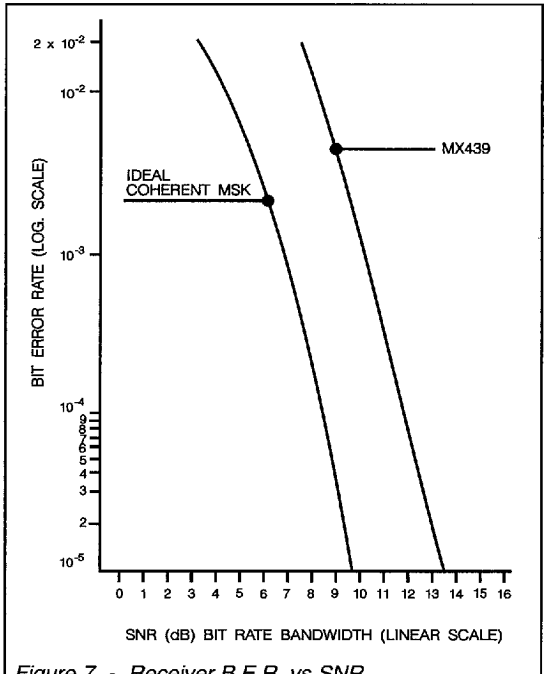


Figure 7 - Receiver B.E.R. vs SNR