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ICs for Communications

Network Termination Controller (2B1Q)
NTC-Q

PEB 8091 Version 1.1

PEF 8091 Version 1.1

Data Sheet 10.97

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83	updated Electrical Characteristics
95	added chapter Power Consumption Measurements in the Application
96	added chapter External Component Sourcing
100	added chapter Differences to IEC-Q NTE, SBCX
101	added chapter Glossary
103	added chapter Quick Reference Guide

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1 Overview

The Network Termination Controller (2B1Q) (NTC-Q) is a Network Termination (NT) circuit for the basic rate Integrated Services Digital Network (ISDN). It combines a U-transceiver and an S-transceiver on one chip. The NTC-Q provides the 2B1Q-U-interface as defined by ETSI ETR 080 1995 and ANSI T1.601 1992 together with the S/T-interface as specified in ITU Rec. I.430, ANSI T1.605 and ETSI ETS 300 012.

The NTC-Q works as a stand-alone NT1 with completely automatic handling of all layer-1 procedures without a microcontroller. It transparently exchanges the 144 kbit/s user data between the U- and the S/T-interface

An optional IOM-2 interface and various test modes ease chip evaluation and testing.

The NTC-Q is a CMOS device which is available in a P-TQFP-64 and P-MQFP-64 package and operates from a single +5V supply with very low power consumption.

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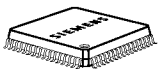
Network Termination Controller (2B1Q) **PEB 8091**
NTC-Q **PEF 8091**

Version 1.1 **CMOS**

1.1 Features

P-TQFP-64



P-MQFP-64

- Single chip solution including U- and S-transceiver
- Perfectly suited for the NT1 in the ISDN
- Fully automatic activation and deactivation
- U-interface (2B1Q) conform to ANSI T1.601, ETSI ETR 080 and CNET ST/LAA/ELR/DNP/822:
  - Meets all transmission requirements on all ANSI, ETSI and CNET loops with margin
  - Conform to British Telecom's RC7355E
  - Compliant with ETSI 10ms micro interruptions
  - Pin programmable CSO-bit
  - Pin programmable ACT-bit in loop 2 meets ETSI and ANSI specification
  - MLT input and decode logic (ANSI)
  - Function compatible to IEC-Q, IEC-Q TE and IEC-Q NTE
- S/T-interface conform to ITU Rec. I.430, ETS 300 012 and ANSI T1.605
  - Supports point-to-point and bus configurations
  - Meets and exceeds all transmission requirements
  - Function compatible to SBCX
- Activation status LED supported
- Optional IOM-2 interface eases chip testing and evaluation
- Single 5 Volt power supply
- Low power CMOS technology
- 285 mW power consumption with random data over typical line (15kft, 26AWG)

1.2 Logic Symbol

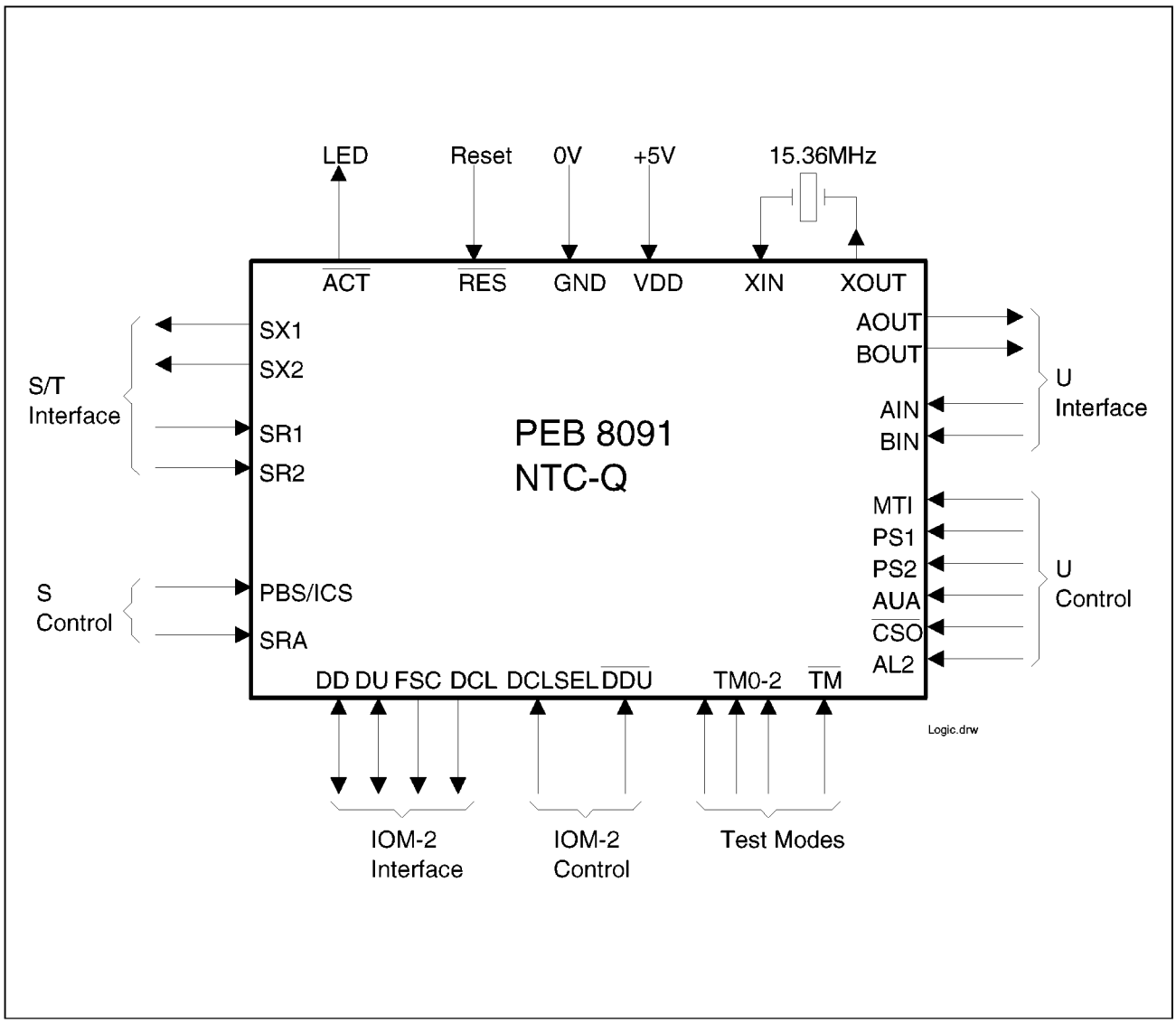


Figure 1 Logic Symbol

1.3 Pin Configuration

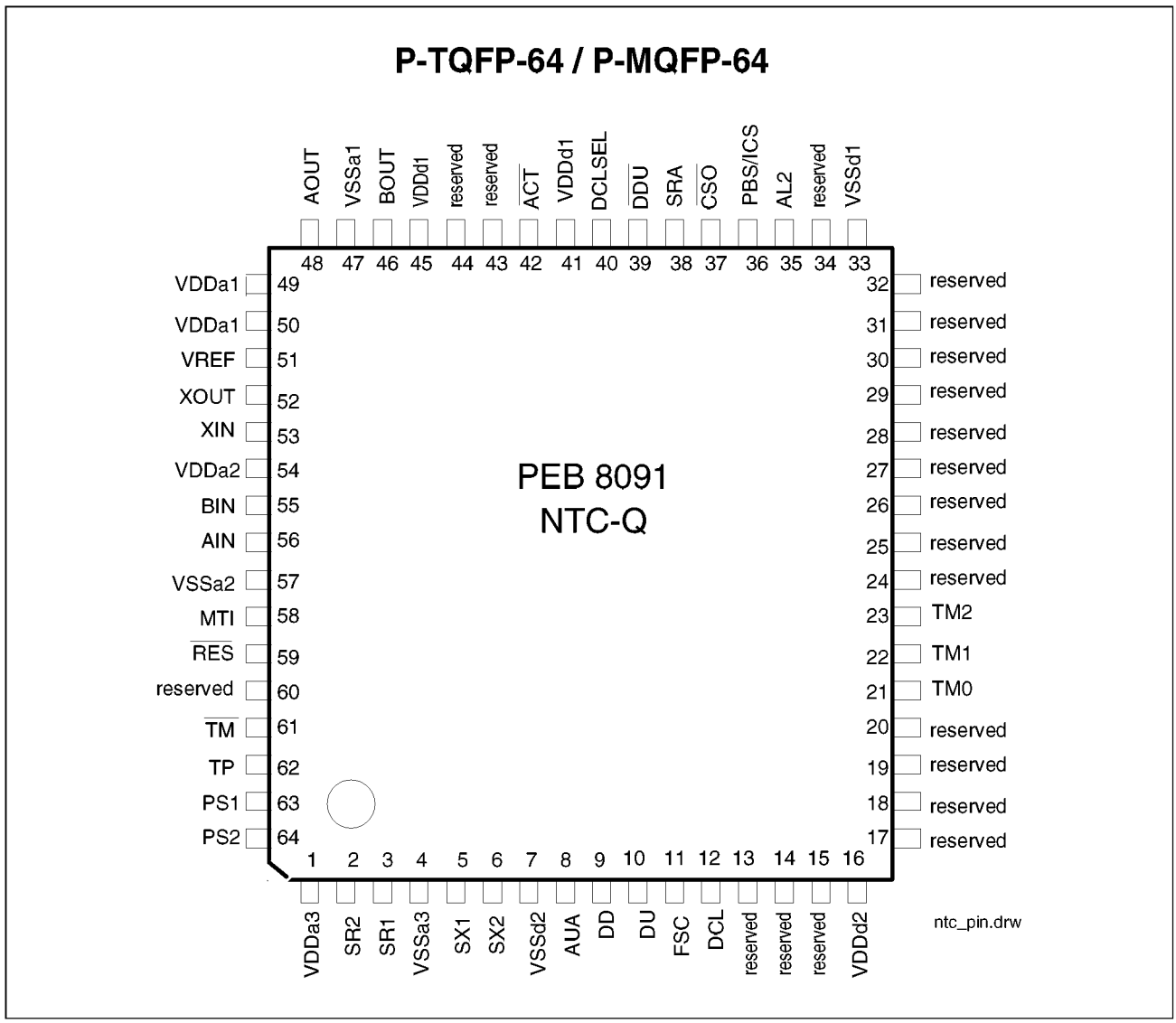


Figure 2 Pin Configuration

1.4 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type and a brief description of the function

Pin No.	Symbol	I/O	Description
Power Supply Pins			
1, 49, 50, 54	VDD_A1-3		+5V +/-5% supply voltage, analog
16, 41, 45	VDD_D1-2		+5V +/-5% supply voltage, digital
4, 47, 57	VSS_A1-3		Analog GND
7, 33	VSS_D1-2		Digital GND
U-Interface			
48	AOUT	O	Differential U-interface output
46	BOUT	O	Differential U-interface output
56	AIN	I	Differential U-interface input
55	BIN	I	Differential U-interface input
S/T-Interface			
5	SX1	O	S/T-interface positive transmit output
6	SX2	O	S/T-interface negative transmit output
3	SR1	I	Differential S/T-interface receive input
2	SR2	I	Differential S/T-interface receive input
IOM®-2 interface			
9	DD	I/O	**Data Downstream.** IOM-2 data downstream synchronous to DCL clock. Push-pull, open-drain or high Z (see pp.20).
10	DU	I/O	**Data Upstream.** IOM-2 data upstream synchronous to DCL clock. Push-pull, open-drain or high Z (see pp.20).
11	FSC	O	**Frame synchronization clock.** The start of the B1 channel in time slot 0 is marked. Push-pull or high Z (see pp.20).

Pin No.	Symbol	I/O	Description
12	DCL	O	**Data clock.** 512 kHz if DCLSEL='1', 1.536 MHz if DCLSEL='0'. Push-pull or high Z (see pp.20).

Control and Status Pins

42	$\overline{\text{ACT}}$	O	**Activation LED.** Low Active. Indicates the activation status of U- and S-transceiver. Can directly drive an LED. Open-drain.
63	PS1	I (PD)	**Power Status (primary).** The pin status is passed to the overhead bit 'PS1' in the U frame to indicate the status of the primary power supply ('1' = ok).
64	PS2	I	**Power Status (secondary).** The pin status is passed to the overhead bit 'PS2' in the U frame to indicate the status of the secondary power supply ('1' = ok).
8	AUA	I/O (PU)	**Auto U Activation.** '1': U-transceiver attempts one automatic activation after reset. Tie to '0' in applications that do not require auto-start after reset.
37	$\overline{\text{CSO}}$	I (PU)	**Cold Start Only.** '0' selects CSO-bit to '1'. '1' selects CSO-bit to '0'. The pin only controls the cso-bit in the U-frame. The U-transceiver itself is always a warm-start transceiver according to ANSI and ETSI.
35	AL2	I (PU)	**ACT-bit Loop 2.** '1' selects the control of loop 2 according to ETSI, '0' sets it according to ANSI.
58	MTI	I	**Metallic Termination Input.** Input to evaluate Metallic Termination pulses. Tie to '1' if not used.

Pin No.	Symbol	I/O	Description
38	SRA	I	**S-Receiver Amplifier.** '1' selects 1:1 amplifier ratio (2:1 transformer). '0' selects 2:1 amplifier ratio (external capacitive coupling).
36	PBS ICS	I (PU)	**Point- Bus Selection.** Selects between point-to-point (1) and bus (0) mode of S-receiver. **IOM®-2 channel S-Transceiver** Applies only when DCL = 1.536 MHz (DCLSEL='0'). Point-Bus selection is possible via programming (refer to page 53). '0' on this pin maps S-transceiver to IOM-2 channel 1, '1' maps it to channel 0.
40	DCLSEL	I	**DCL Select.** Selects between 512 kHz (1) and 1.536 MHz (0) DCL clock rate. Pin AUA must be tied to '0' if 1.536 MHz are selected. Normal NT1 operation if '1'. (see pp.20)
39	$\overline{\text{DDU}}$	I	**Disconnect DU.** '0' disconnects DU between S- and U-transceiver for test purposes. Normal NT1 operation if '1'. (see pp.20)

Test Pins and Miscellaneous Pins

61	$\overline{\text{TM}}$	I (PU)	**Test Mode**. Activates test mode of pins TM2-0 if tied to VSS (see page 66).
23	TM2	I/O (PU)	**Test Mode 2.** Selects test modes if $\overline{\text{TM}}$ = 0 (see page 66).
22	TM1	I/O (PU)	**Test Mode 1.** Selects test modes if $\overline{\text{TM}}$ = 0 (see page 66).
21	TM0	I/O (PU)	**Test Mode 0.** Selects test modes if $\overline{\text{TM}}$ = 0 (see page 66).
62	TP	I (PD)	**Test Pin.** Used for factory device test. Do not connect.
59	$\overline{\text{RES}}$	I	**Reset Input.** Active low. Tie to '1' if not used.

Pin No.	Symbol	I/O	Description
53	XIN	I	**Crystal IN.** Connect 15.36 MHz clock input or 15.36 MHz crystal.
52	XOUT	O	**Crystal OUT.** Connect 15.36 MHz crystal. Leave open if not used.
51	VREF	I/O	**Reference Voltage.** Connect 100nF vs. VSS_A to buffer internally generated reference voltage.
15, 24, 25, 26, 27, 28, 29, 30, 31, 32, 34	reserved	I	Tie to '1'.
43, 44, 60	reserved	I	Tie to '0'
13, 14, 17, 18 19, 20	reserved	O	Leave open

PU: Internal pull-up resistor

PD: Internal pull-down resistor

1.5 System Integration

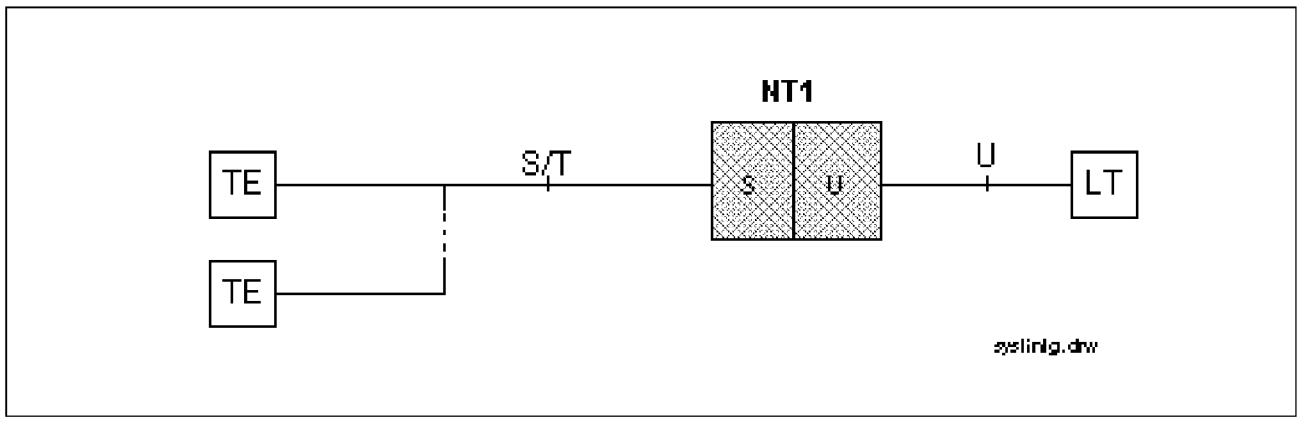


Figure 3 System Integration

The NTC-Q provides NT1 functionality without a microcontroller being necessary. **Figure 4** shows a block diagram of the NTC-Q.

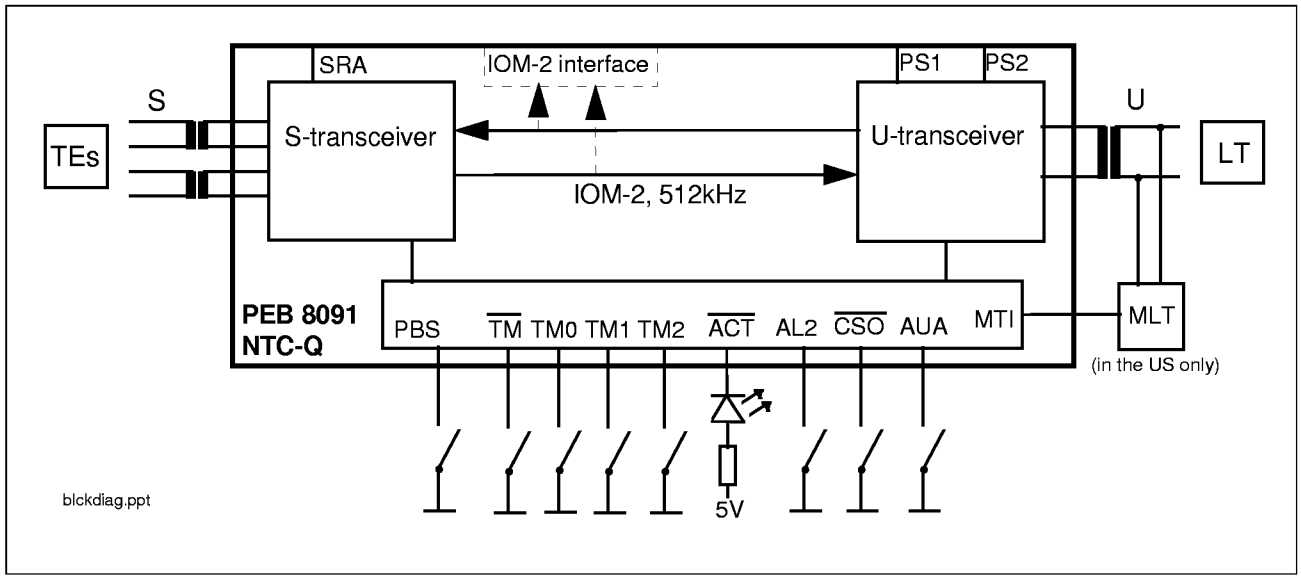


Figure 4 NT1 Block Diagram

Pin AUA is used to select automatic activation of the U-transceiver after power-on and reset. Additional pins control the state of the CSO-bit, ACT-bit during loop-back #2 and the PS1 and PS2 bits in the U-frame. The U-transceiver supports U-only activation according to ANSI and ETSI. The test modes 'quiet mode', 'send single pulses' and 'data through' can be selected via pins $\overline{TM}$ and TM0-2.

The S-transceiver timing mode may be switched between point-to-point and bus configuration. The amplifier of the S-receiver is configurable to a 2:1 ratio which allows the use of capacitive coupling for the receiver. Two test patterns (2 kHz, 96kHz) can be generated via pin strapping of $\overline{TM}$ and TM0-2.

All configuration pins which are intended for connection to a switch have internal pull-up resistors. An LED can be connected to indicate the activation status of the U- and the S-transceiver.

The communication between the S-transceiver and the U-transceiver can be monitored on a 512 kHz IOM-2 interface. The IOM-2 interface can be disabled to minimize power consumption. In addition to the 512 kHz mode, the 1.536 MHz IOM-2 mode may be selected via pin strapping (pin DCLSEL). The S-transceiver may then be configured to IOM-2 channel 0 or channel 1. If 1.536 MHz is selected the S-transceiver is in LT-S mode and the U-transceiver is in TE mode.

For US-applications, the metallic loop termination state machine is included which evaluates the signal provided on the MTI-input and automatically sets the NTC-Q in the proper test mode.

2 Functional Description

2.1 Device Architecture

The NTC-Q contains the following interfaces and functional blocks:

- IOM-2 Configuration see pp. 20
- IOM-2 Interface pp. 22
- U-Transceiver (IEC-Q NTE Core) pp. 26
- S-Transceiver (SBCX Core) pp. 53
- Activation Status LED pp. 65
- Power-on reset pp. 66
- Test Mode Unit pp. 66
- Clock Generation pp. 82
- Factory Test Unit

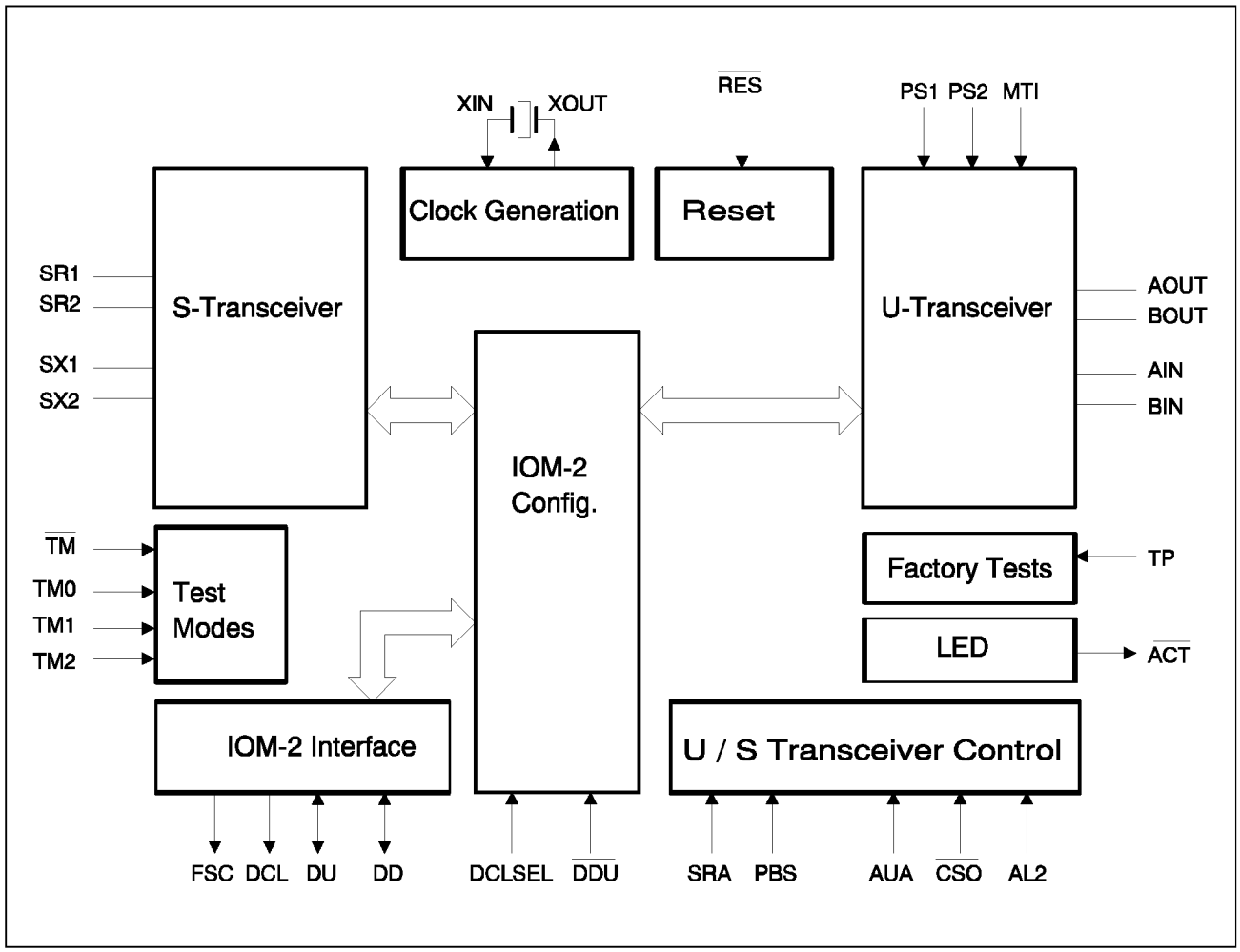


Figure 5 NTC-Q Device Architecture

2.2 IOM®-2 Interface

The IOM-2 interface may be used to monitor the interaction between the U- and the S-transceiver. It provides a symmetrical full-duplex communication link, containing user data, control/programming and status channels. The structure used follows the 2B + 1 D-channel structure of ISDN. The ISDN user data rate of 144 kbit/s (B1 + B2 + D) is transmitted in both directions over the interface.

2.2.1 IOM®-2 Configurations

It is possible to configure the IOM-2 interface for various test and evaluation scenarios.

Normal NT1 Operation

In a normal NT1 application, the pins $\overline{DDU}$, DCLSEL and $\overline{TM}$ are clamped to 'high', which disables the IOM-2 interface to minimize power consumption. If $\overline{TM}$=0 and TM0-2=111, the C/I-codes, B- and D-channels between the S- and U-transceiver can be monitored on the IOM-2 interface.

In case the IOM-2 interface is disabled, the data lines DU and DD shall be on a defined potential. In applications where pin $\overline{TM}$ is clamped to V_{DD} because the test modes are unused, DU and DD can be clamped directly to V_{DD} or V_{SS}. If pin $\overline{TM}$ is connected to a switch, pins DU and DD should be connected to V_{DD}/V_{SS} via pull-up/down resistors (e.g. 10 kΩ).

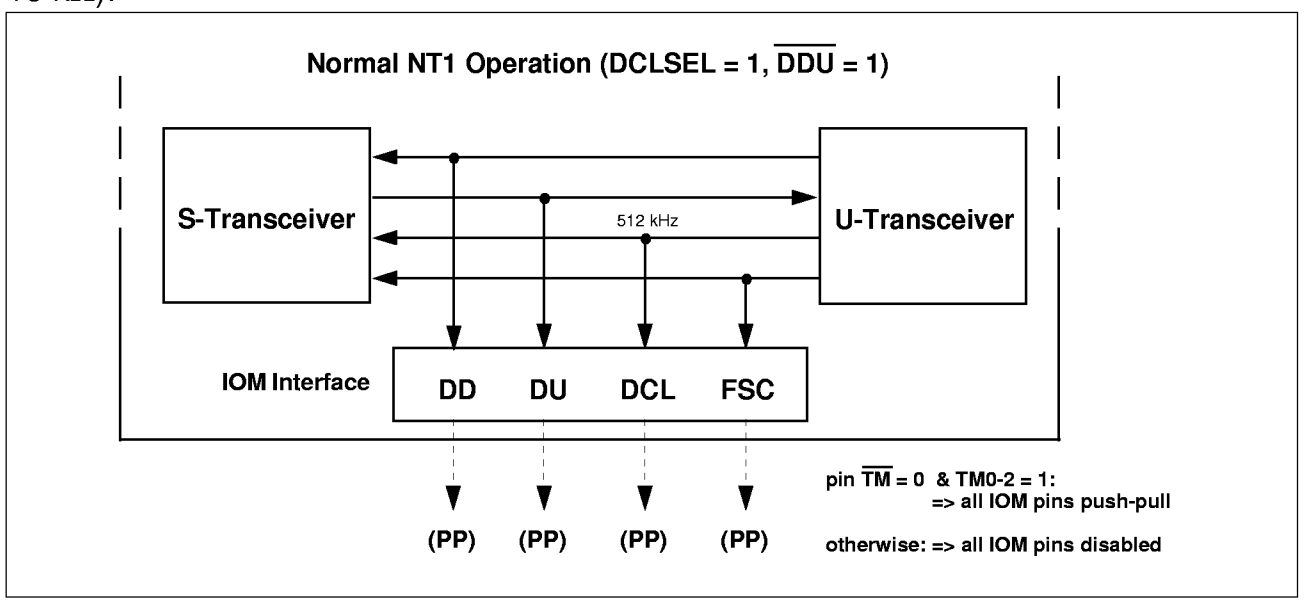


Figure 6 IOM®-2 Configurations (Pin DCLSEL = 1)

Direct Access to U-transceiver

In this configuration the U-transceiver of the NTC-Q is controlled via the IOM-2 interface. Therefore, it is possible to test the U-transceiver with the same test equipment as used for the IEC-Q. The chip-internal data output of the S-transceiver is disabled.

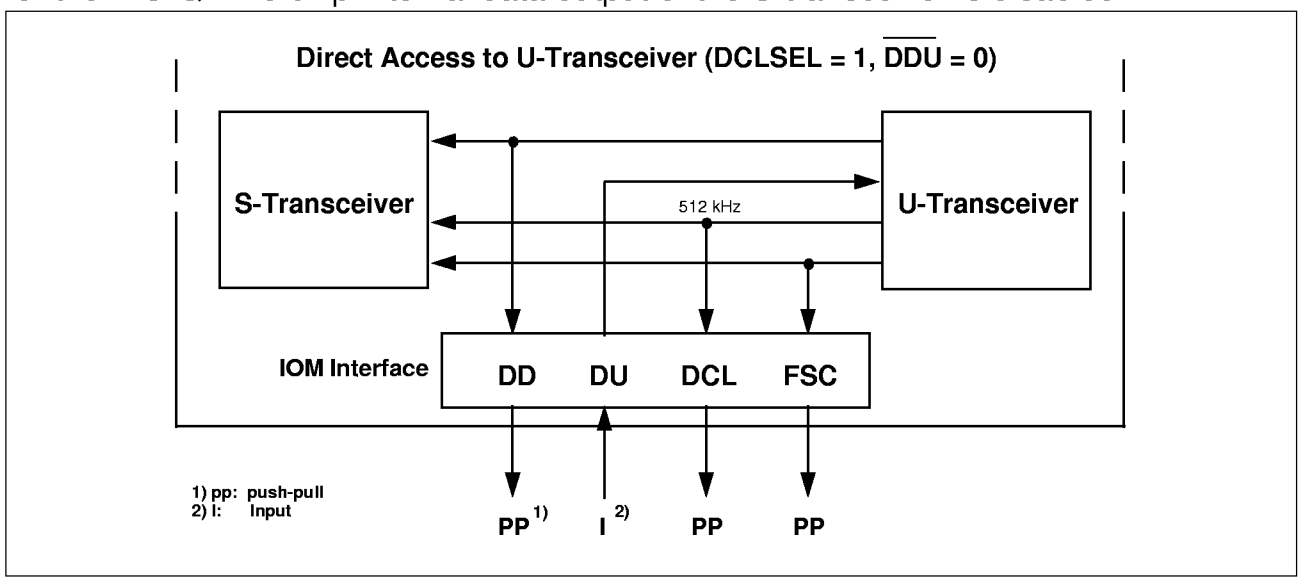


Figure 7 IOM®-2 Configurations (Pin DCLSEL = 1, $\overline{\text{DDU}}$ = 0)

DCL = 1.536 MHz (pin DCLSEL = 0, AUA = 0)

If DCLSEL = 0 the IOM-2 interface is always active. The IOM-2 data lines DD and DU are open drain in/outputs. Pin ICS selects the IOM-2 channel of the S-transceiver. ICS=0 maps the S-transceiver to IOM-2 channel 1, ICS=1 maps it to channel 0. Pin AUA must be 'low' if DCLSEL = 0.

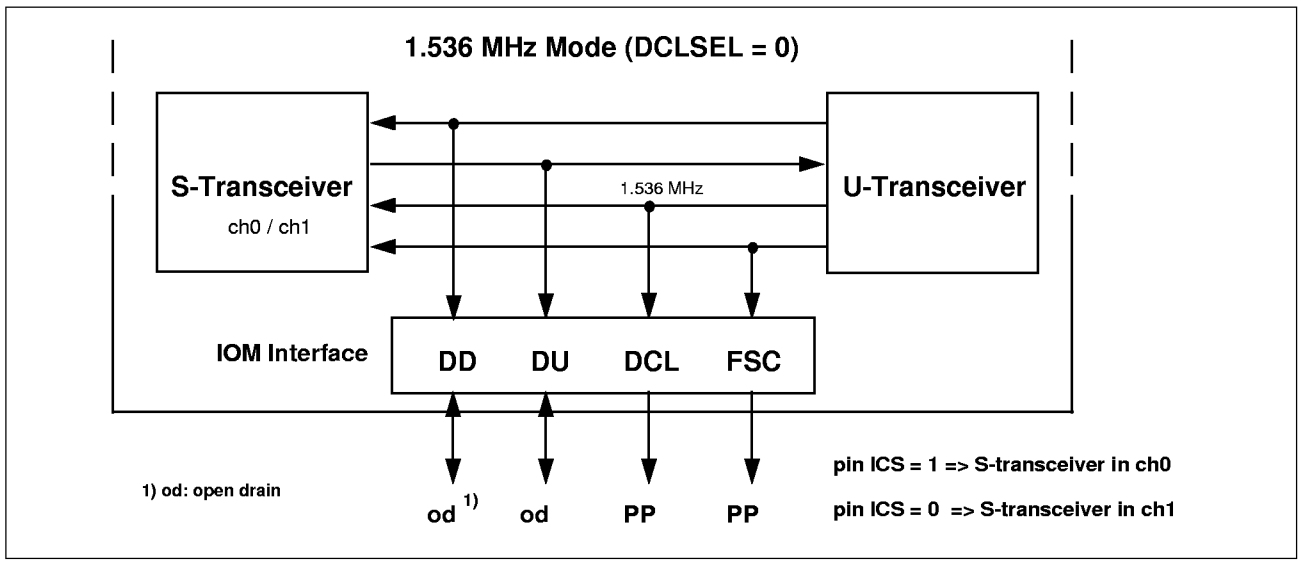


Figure 8 IOM®-2 Configurations (Pin DCLSEL = 0)

2.2.2 IOM®-2 Frame Structure

The IOM-2 interface comprises two clock lines for synchronization and two data lines.

Data is carried over Data Upstream (DU) and Data Downstream (DD) signals. The downstream and upstream direction are always defined with respect to the exchange. Downstream refers to information flow from the exchange to the subscriber and upstream vice versa respectively.

The data is clocked by a Data Clock (DCL) that operates at twice the data rate. Frames are delimited by an 8-kHz Frame Synchronization Clock (FSC). Incoming data is sampled on every second falling edge of the DCL clock.

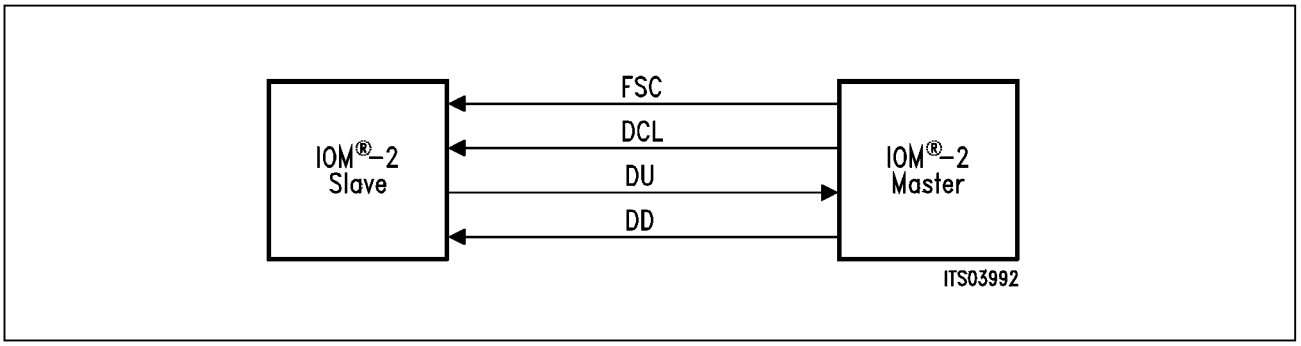


Figure 9 IOM®-2 Clocks and Data Lines

Depending on the frequency of DCL an IOM-2 frame carries one or several IOM-2 channels. The structure of an IOM-2 channel is given in **figure 10**.

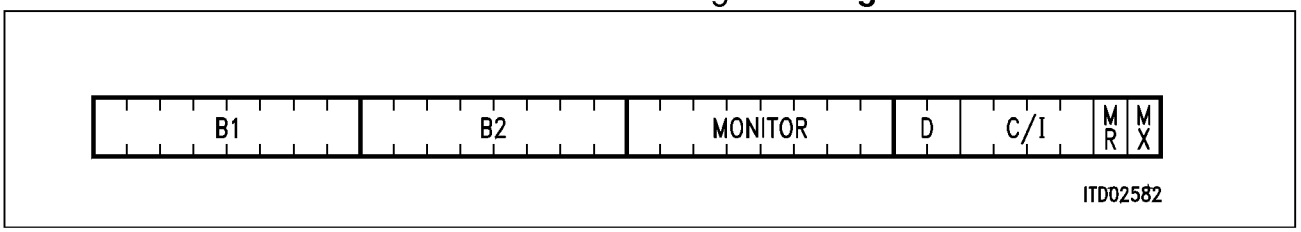


Figure 10 IOM®-2 Channel Structure

An IOM-2 channel consists of:

- two 64 kbit/s channels B1 and B2
- the monitor channel for transferring maintenance information
- two bits for the 16 kbit/s D-channel
- four command/indication (C/I) bits for controlling of layer-1 functions (U- and S-transceiver).
- two bits MR and MX for the handshake procedure in the monitor channel

2.2.2.1 NT1 Frame Structure (DCL = 512 kHz)

If DCL = 512 kHz the IOM-2 interface provides one IOM-2 channel with a nominal data rate of 256 kbit/s. The channel contains 144 kbit/s (for 2B+D) plus MONITOR and Command/Indication channels.

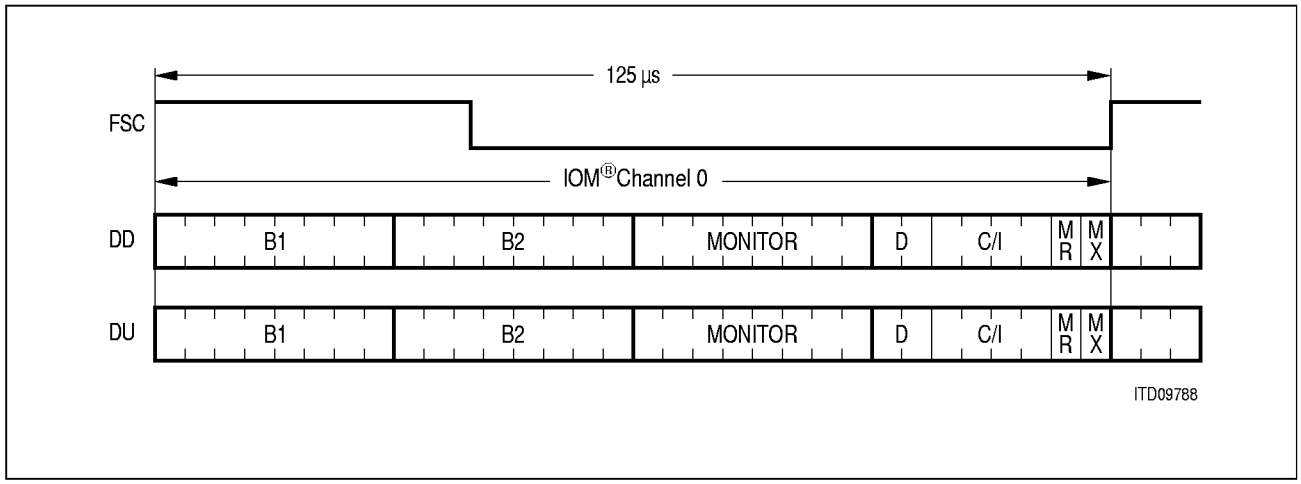


Figure 11 IOM®-2 Frame (DCL = 512 kHz)

2.2.2.2 TE Frame Structure (DCL = 1.536 MHz)

DCL can also be set to 1.536 MHz via pin DCLSEL. In this case the IOM-2 interface provides three IOM-2 channels (**figure 12**). The U-transceiver is tied to channel 0. The S-transceiver can be mapped to either channel 0 or channel 1 via pin ICS.

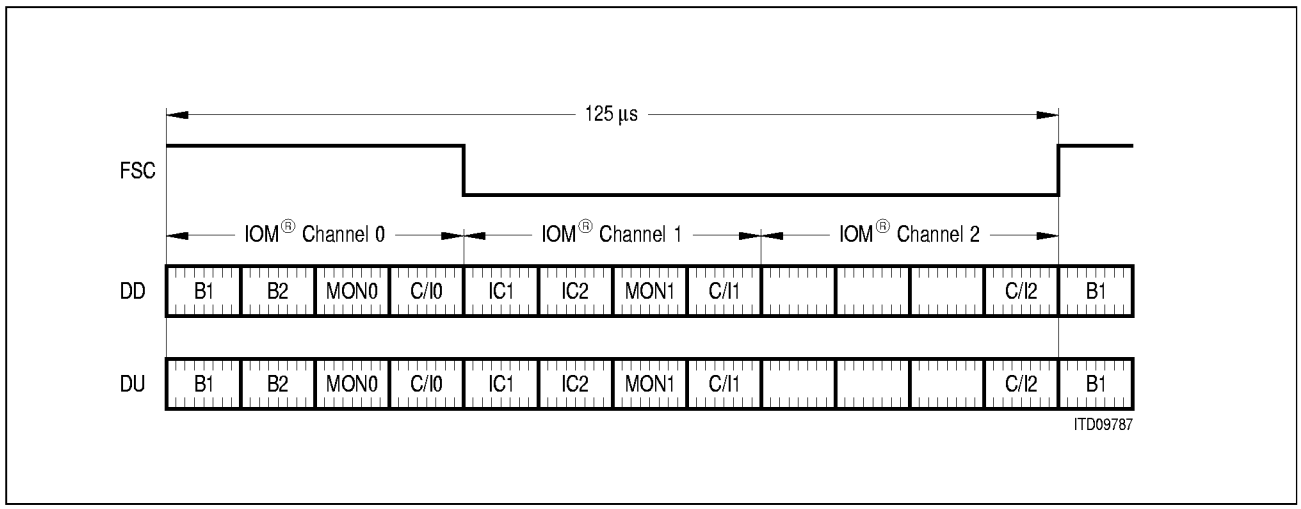


Figure 12 IOM®-2 Frame (DCL = 1.536 MHz)

2.2.3 IOM®-2 Command / Indication Channel

The Command/Indication (C/I) channel carries real-time control and status information between the U- and the S-transceiver. A new code must be detected in two consecutive IOM-2 frames to be considered valid (double last look criterion).

The C/I code is four bits long. A listing and explanation of the U-transceiver and S-transceiver C/I codes can be found in **chapter 2.3.6** and **2.4.5**.

2.2.4 IOM®-2 Monitor Channel

The monitor channel protocol is a handshake protocol used for programming and monitoring devices in the MONITOR channel. In an NT1 application the MONITOR channel is not used.

2.2.5 Activation/Deactivation of IOM®-2 Clocks

The IOM-2 clocks are switched off (power-down) after the U-transceiver enters state 'Deactivated'. This reduces power consumption to a minimum. During power-down the clock lines are held low and the data lines are high. The power-down state within the 'Deactivated' state will only be entered if no monitor messages are pending on IOM-2.

The **deactivation procedure** is shown in **figure 13**. After detecting C/I code DI the U-transceiver responds by transmitting DC during subsequent frames and stops the IOM-2 clocks synchronously with the end of the last C/I channel bit of the fourth frame.

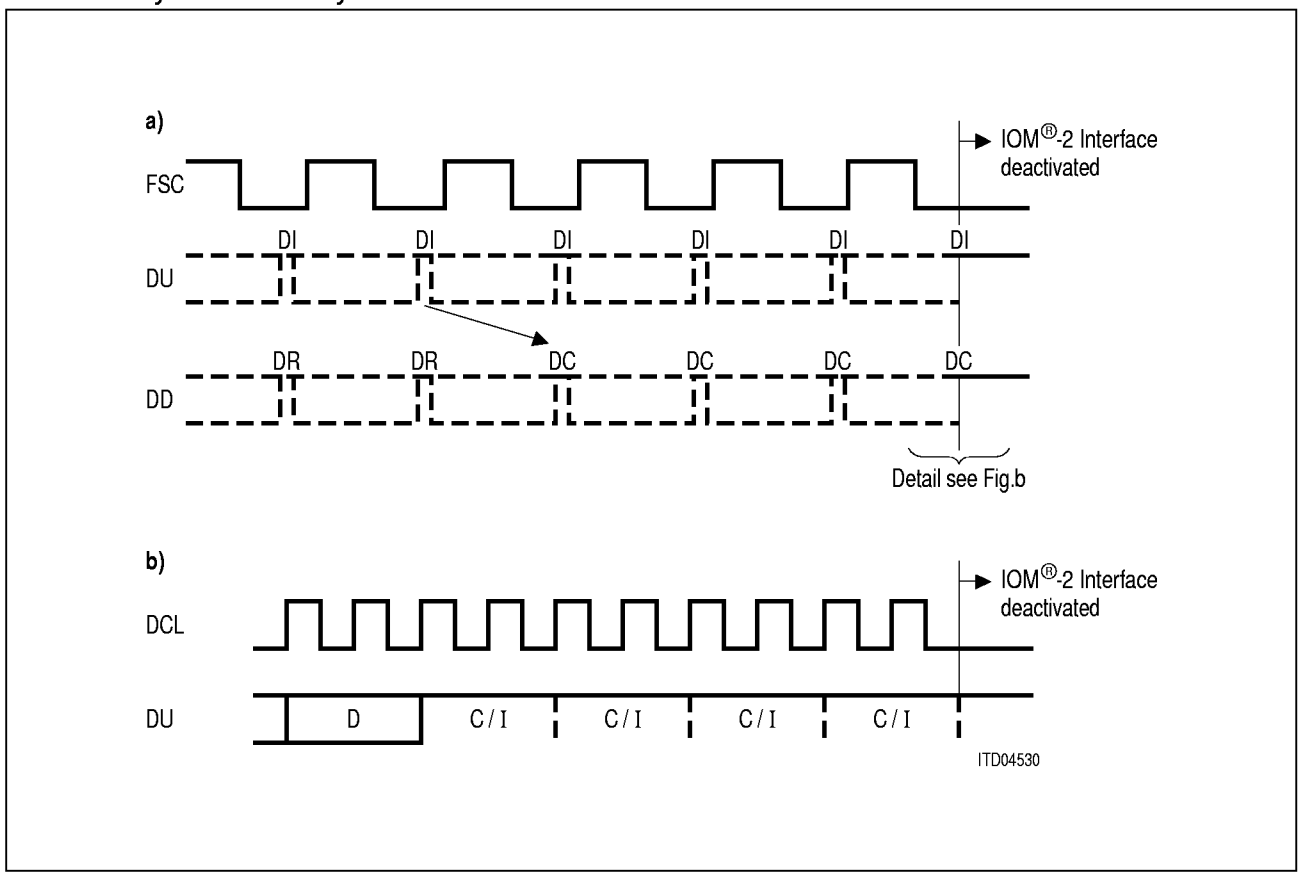


Figure 13 Deactivation of the IOM®-2 Clocks

The IOM-2 clocks are **activated** automatically when a line activation is detected either on the S- or the U-interface.

DCL is activated such that its first rising edge occurs with the beginning of the bit following the C/I channel. After the clocks have been enabled this is indicated by the PU code in the C/I channel.

2.3 U-Transceiver

The U-interface establishes the direct link between the exchange and the terminal side over two copper wires. Transmission over the U-interface is performed at a rate of 80 kBaud. The code used is reducing two binary informations to one quaternary symbol (2B1Q) resulting in a total of 160 kbit/s to be transmitted. 144 kbit/s are user data (B1 + B2 + D), 16 kbit/s are used for maintenance and synchronization information.

The NTC-Q uses two differential outputs (AOUT, BOUT) and two differential inputs (AIN, BIN) for transmission and reception. These differential signals are coupled via a hybrid and a transformer to the two-wire U-interface.

2.3.1 Modes

In NT1 applications (pin DCLSEL = '1') the U-transceiver delivers a DCL of 512 kHz.

If pin DCLSEL=AUA= '0' the U-transceiver delivers a DCL of 1.536 MHz. Depending on pin ICS the S-transceiver is then mapped to IOM channel 0 or 1. The U-transceiver always remains in channel 0. If the S-transveiver is mapped to channel 1 the U-transceiver can be accessed via the Monitor channel. For a description of the access to the U-transceiver's overhead bits and local functions please refer to the data sheet of the PEB 8191 (INTC-Q).

2.3.2 U-Frame Structure

Each basic frame consists of 18 bits for the (inverted) synchronization word; 6 overheads bits are allocated for system functions, and 216 bits transfer the userdata of 2B + D-channel (i.e. userdata of 12 IOM-frames is packed into one basic U-frame).

Data is grouped together into U-superframes of 12 ms. The beginning of a new superframe is marked with an inverted synchronization word (ISW). Each superframe consists of eight basic frames (1.5 ms) which begin with a standard synchronization word (SW) and contain 222 bits of information (**table 1**).

Table 1 U-Frame Structure

		Framing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118	118	119	119	120	120
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOCa1	EOCa2	EOCa3	ACT/ ACT	1	1
	2	SW	2B + D	EOC d/m	EOCi1	EOCi2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOCi3	EOCi4	EOCi5	1/ PS2	CRC1	CRC2
	4	SW	2B + D	EOCi6	EOCi7	EOCi8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOCa1	EOCa2	EOCa3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOC d/m	EOCi1	EOCi2	1	CRC7	CRC8
	7	SW	2B + D	EOCi3	EOCi4	EOCi5	UOA / SAI	CRC9	CRC10
	8	SW	2B + D	EOCi6	EOCi7	EOCi8	AIB / NIB	CRC11	CRC12
2,3…									
						LT- to NT dir. >	/	< NT- to LT dir.	

– ISW Inverted Synchronization Word (quad): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quad): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel

a = address bit
d/m = data / message bit
i = information (data / message)

– ACT Activation bit — ACT = (1) –> Layer 2 ready for communication
– DEA Deactivation bit — DEA = (0) –> LT informs NT that it will turn off
– CSO Cold Start Only — CSO = (1) –> NT-activation with cold start only
– UOA U-Only Activation — UOA = (0) –> U-only activated
– SAI S-Activity Indicator — SAI = (0) –> S-interface is deactivated
– FEBE Far-end Block Error — FEBE = (0) –> Far-end block error occurred
– PS1 Power Status Primary Source — PS1 = (1) –> Primary power supply ok
– PS2 Power Status Secondary Source — PS2 = (1) –> Secondary power supply ok
– NTM NT-Test Mode — NTM = (0) –> NT busy in test mode
– AIB Alarm Indication Bit — AIB = (0) –> Interruption (according to ANSI)
– NIB Network Indication Bit — NIB = (1) –> no function (reserved for network use)

2.3.2.1 Scrambler / Descrambler

A scrambling/descrambling algorithm according to ANSI T1.601 ensures that no sequences of permanent binary 0s or 1s are transmitted. Scrambling and descrambling are controlled fully automatically by the NTC-Q. Hence, no influence can be taken by the user.

2.3.2.2 Cyclic Redundancy Check

The cyclic redundancy check provides a possibility to verify the correct transmission of data. The checksum of a transmitted U-superframe is calculated from the bits in the D-channel, both B-channels, and the M4 bits according to the CRC polynominal

$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The check digits (CRC bits CRC1, CRC2, ..., CRC12) generated are transmitted at position M5 and M6 in the U-superframe. At the receiving side this value is compared with the value calculated from the received superframe.

In case these values are not identical a CRC-error will be indicated to both sides of the U-interface. It is indicated as a NEBE (Near-end Block Error) on the side where the error is detected and as a FEBE (Far-end Block Error) on the remote side. The FEBE-bit will be placed in the next available U-superframe transmitted to the originator.

Figure 14 illustrates the CRC-process.

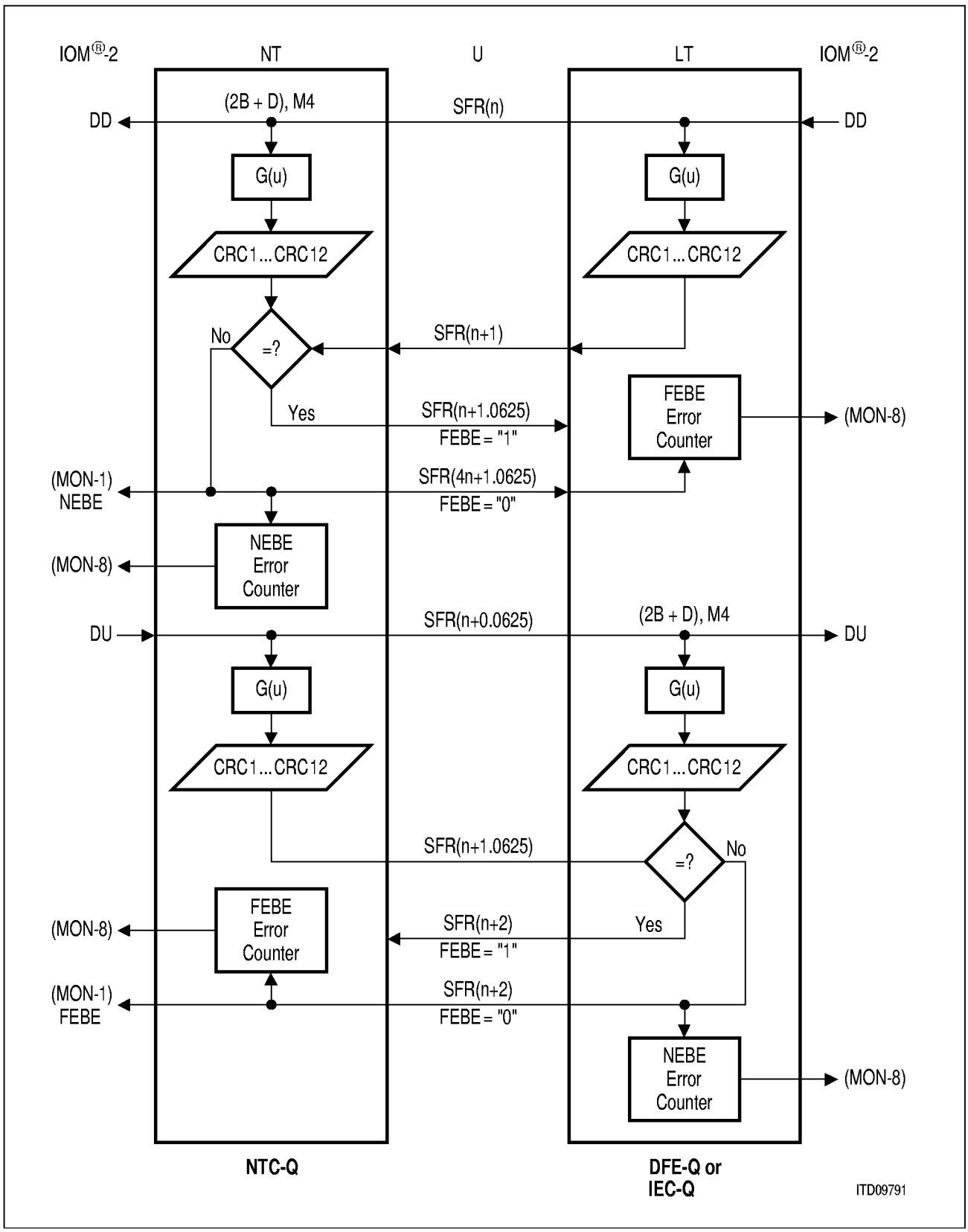


Figure 14 CRC-Process

2.3.2.3 Embedded Operations Channel (EOC)

EOC-data is inserted into the U-frame at the positions M1, M2 and M3 thereby permitting the transmission of two complete EOC-messages (2 × 12 bits) within one U-superframe.

The EOC contains an address field, a data/message indicator (d/m) and an eight-bit information field.

With the **address field** the destination of the transmitted message/data is defined. Addresses are defined for the NT, 6 repeater stations and broadcasting.

The **data/message indicator** (d/m) needs to be set to (1) to indicate that the information field contains a message. If set to (0), numerical data is transferred to the NT. Currently no numerical data transfer to or from the NT is required.

From the 256 codes possible in the **information field** 64 are reserved for non-standard applications, 64 are reserved for internal network use and eight are defined by ANSI/ ETSI for diagnostic and loop-back functions. All remaining 120 free codes are available for future standardization.

Table 2 EOC-Codes

EOC							
Address			**d/m**	**Information (hex)**	**Direction**	**Message**	**Function**
a1	**a2**	**a3**	**d/m**	**i1 - i8**			
0	0	0	x			NT	
1	1	1	x			Broadcast	
0 1	0 1	1 0	x			Repeater stations No. 1 – No. 6	
			0			Data	
			1			Message	
			1	50	NT <---- LT	LBBD	Close complete Loop
			1	51	NT <---- LT	LB1	Close Loop B1
			1	52	NT <---- LT	LB2	Close Loop B2
			1	53	NT <---- LT	RCC	Request Corrupt CRC
			1	54	NT <---- LT	NCC	Notify of corrupt CRC
			1	FF	NT <---- LT	RTN	Return to normal
			1	00	NT <---> LT	H	Hold

Table 2 EOC-Codes (cont'd)

EOC					
Address	**d/m**	**Information (hex)**	**Direction**	**Message**	**Function**
a1 a2 a3	**d/m**	**i1 - i8**			
	1	AA	NT ----> LT	UTC	Unable to comply
	1	XX	NT ----> LT	ACK	Acknowledge

2.3.3 EOC-Processor

An EOC-processor on the chip is responsible for the correct insertion and extraction of EOC-data on the U-interface. Transparent EOC mode as known from the IEC-Q is not available in the NTC-Q. Access to the EOC is only possible when a superframe is transmitted. This is the case in the U-transceiver states 'Synchronized', 'Wait for ACT', 'Transparent', 'Error S/T' and 'Pend. Deac. U'. In all other states the EOC-bits on the U-interface are clamped to high.

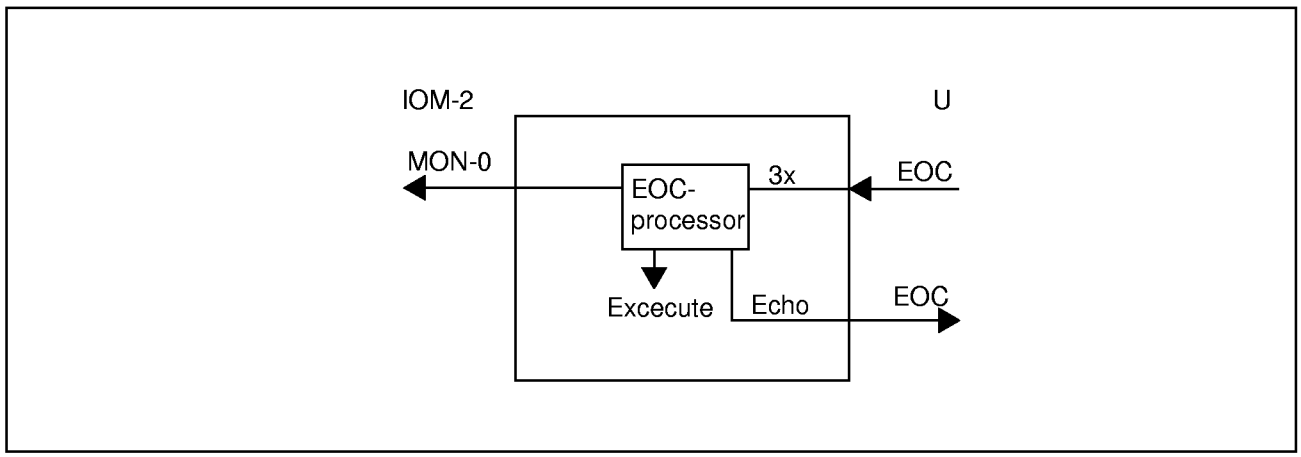


Figure 15 EOC-Processor

EOC Comand Handling

Acknowledgment: All received EOC-frames are echoed back to the exchange immediately without triple-last-look. If an address other than (000_B) or (111_B) is received, a HOLD message with address 000_B is returned. However, there is an exception: The NTC-Q will send a 'UTC' after three consecutive receptions of d/m = (0) or after an undefined command.

Latching: All detected EOC-commands are latched, i.e. they are valid as long as they are not disabled with the EOC 'RTN' command or a deactivation.

Transfer to IOM: With the triple-last-look criteria fulfilled the new EOC-command will be passed to IOM-2 with one single MON-0-message, independently of the address used and the status of the d/m indicator. MON-0-commands from IOM will be ignored.

Execution: The EOC-commands listed in **table 3** will be executed automatically by the PEB 8091 if they were addressed correctly (000_B or 111_B) and the d/m bit was set to message (1). The execution of a command is performed only after the "triple-last-look" criterion is met.

Table 3 Executed EOC Commands

EOC-code i1 - i8 (Hex)	Direction		Function
	D	U	
50	LBBD		**Close complete loop-back #2 (B1, B2, D).** The U-transceiver does not close the complete loop-back immediately after receipt of this code. Instead it issues the C/I-command AIL (in "Transparent" state) or ARL in the states "Error S/T" and "Synchronized". This triggers the S-transceiver to close the loop-back. Please refer also to **table 4** for more details.
51	LB1		**Closes B1 loop-back #2** in NT. All B1-channel data will be looped back within the U-transceiver.
52	LB2		**Closes B2 loop-back #2** in NT. All B2-channel data will be looped back within the U-transceiver.
53	RCC		**Request corrupt CRC.** Upon receipt the NTC-Q transmits corrupted (= inverted) CRCs upstream. This allows to test the near end block error counter on the LT-side. The far end block error counter at the NT-side is disabled and NT-error indications (MON-1) are suppressed.

Table 3 Executed EOC Commands (cont'd)

EOC-code i1 - i8 (Hex)	Direction D	Direction U	Function
54	NCC		**Notify of corrupt CRC.** Upon receipt of NCC the near end block error counter is disabled and error indications are suppressed. This prevents wrong error counts while corrupted CRCs are sent.
FF	RTN		**Return to normal.** With this command all previously sent EOC-commands will be released. The EOC-processor is reset to its initial state (FF_H).

Loop 2 in ETSI and ANSI

The procedure for closing the complete loop in the NT (also refered to as Loop 2) is not identical in ANSI and ETSI standards. Conformance to either the ETSI or the ANSI standard is selected via pin AL2 (**table 4**).

Table 4 Complete Loop #2

Pin AL2	Standard	Downstream act-bit	Upstream act-bit
1	ETSI ETR 080	Complete loop is closed when the received act-bit is ONE.	When the loop is closed the transmitted act-bit is ONE.
0	ANSI T.601	Complete loop is closed independently of the received act-bit.	The transmitted act-bit mirrors back the received act-bit.

2.3.4 State Machine Notation

The state machine includes all information necessary for the user to understand and predict the activation/deactivation status of the U-transceiver. The information contained in a state bubble is:

State name, **U-signal** transmitted, **Single Bits** (Overhead bits) transmitted, **C/I-indication** transmitted on the C/I-channel, **Transition criteria** and **Timers**.

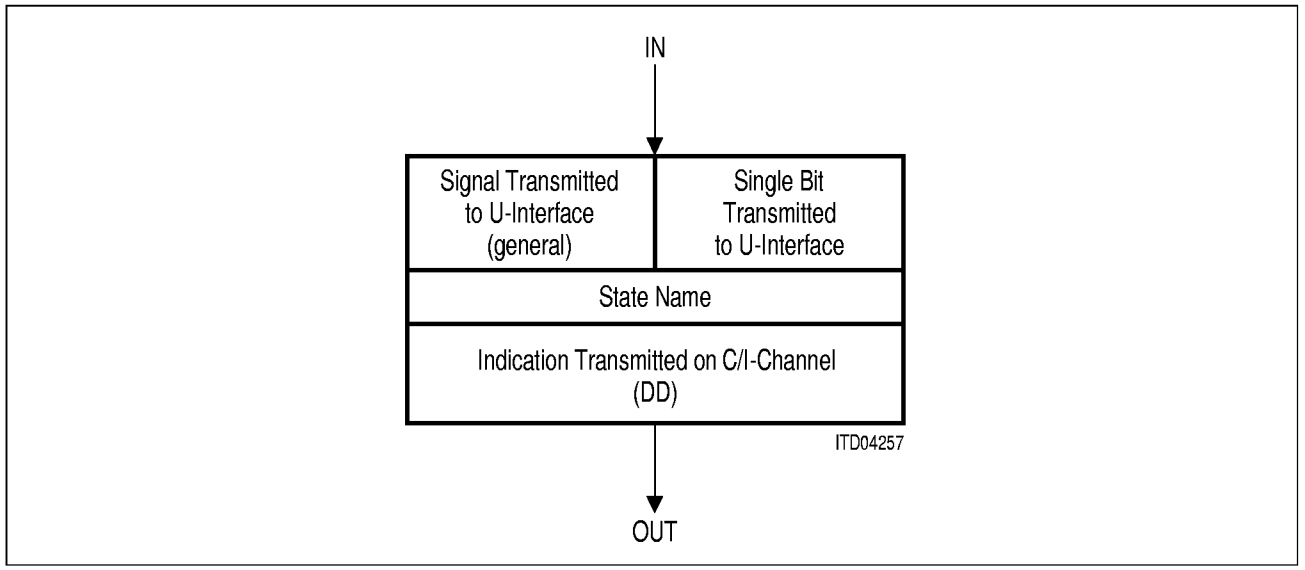


Figure 16 State Diagram Notation U-Transceiver

The following example explains the use of the state diagram by an extract of the NT-state diagram. The state explained is the “EC-Training” state.

Example:

The state may be entered by either of two methods:

–from state “Alerting” after time T11 has expired.
–from state “EC-Training 1” after the C/I command “DI” has been received.

The following information is transmitted:

–SN1 is sent on the U-interface.
–No overhead bits are sent
–C/I message “DC” is issued on the IOM-2 interface.

The state is be left at occurrence of one of the following events:

–Leave for state “EQ-Training” after LSEC has been detected.
–Leave for state “EQ-Training” after timer T12 has expired.

Combinations of transition criteria are possible. Logical “AND” is indicated by “&” (TN & DC), logical “OR” is written “or” and for a negation “/” is used. The start of a timer is indicated with “TxS” (“x” being equivalent to the timer number). Timers are always started when entering the new state. The action resulting after a timer has expired is indicated by the path labelled “TxE”.

2.3.5 State Machine

This chapter describes the behavior of the U-transceiver.

2.3.5.1 Cold and Warm Starts

Two types of start-up procedures are supported by the U-transceiver: cold starts and warm starts.

Cold starts are performed after a reset and require all echo and equalizer coefficients to be recalculated. This procedure typically is completed after 1-7 seconds depending on the line characteristics. Cold starts are recommended for activations where the line characteristics have changed considerably since the last deactivation.

A warm start procedure uses the coefficient set saved during the last deactivation. It is therefore completed much faster (maximum 300 ms). Warm starts are however restricted to activations where the line characteristics do not change significantly between two activations.

Regarding the path in the transition diagram, cold starts have in particular that the U-transceiver has entered the state ’Test’ (e.g. due to a reset) prior to an activation. The activation procedure itself is then identical in both cases. Therefore, the following sections apply to both warm and cold starts.

2.3.5.2 NT Mode State Diagram

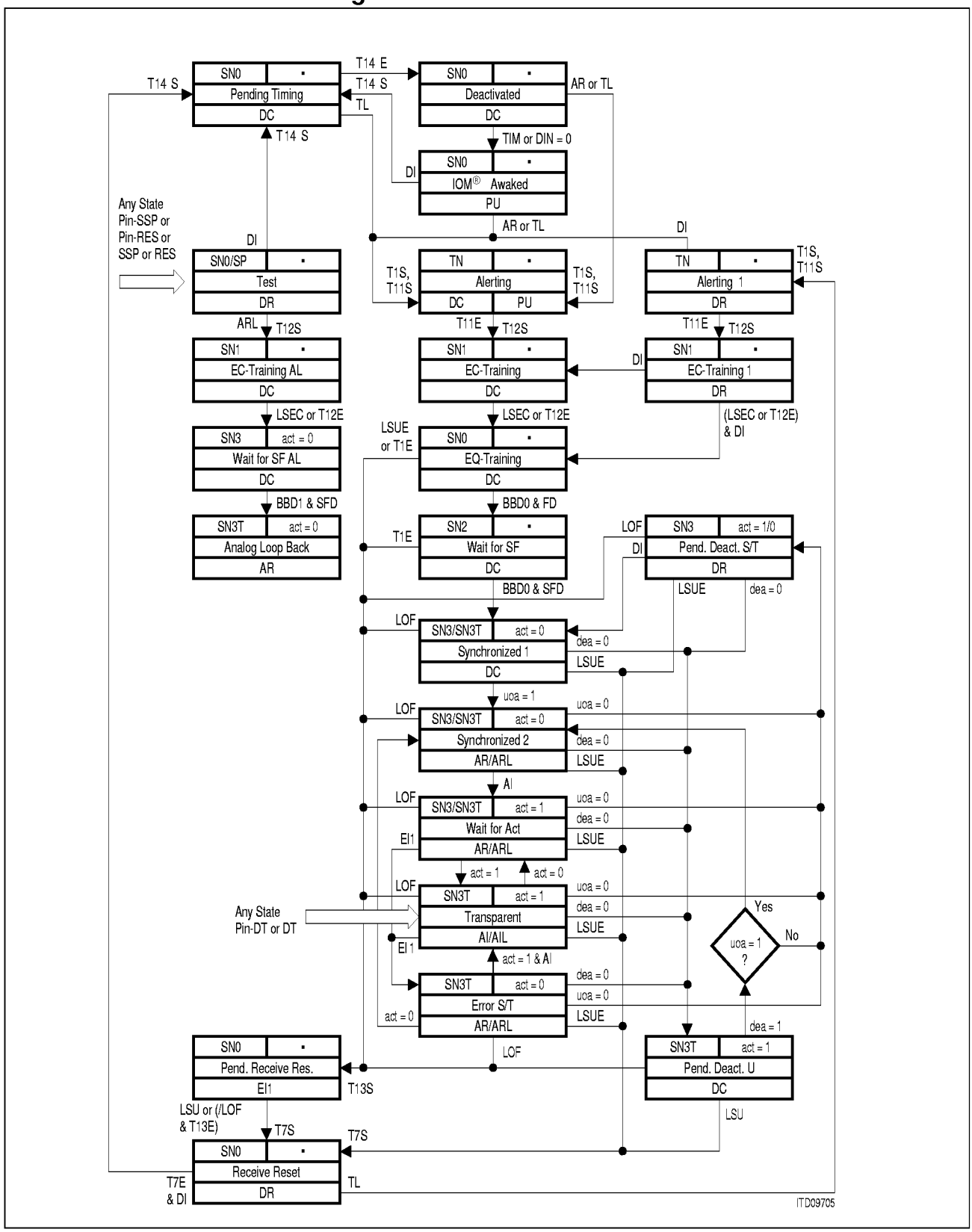


Figure 17 State Transition Diagram

2.3.5.3 Inputs to the U-Transceiver

C/I-Commands

AI Activation Indication
The S-transceiver issues this indication to announce that the S-receiver is synchronized. The U-transceiver informs the LT side by setting the “ACT” bit to “1”.

AR Activation Request
INFO1 has been received by the S-transceiver. The U-transceiver is requested to start the activation process by sending the wake-up signal TN.

ARL Activation Request Local Loop-back
The U-transceiver is requested to operate an analog loop-back (close to the U-interface) and to begin the start-up sequence by sending SN1 (without starting timer T1). This command may be issued only after the U-transceiver has been reset by making use of the C/I-channel code RES or a hardware reset. This assures that the EC- and EQ-coefficient updating algorithms converge correctly. The ARL-command has to be issued continuously as long as the loop-back is required.

DI Deactivation Indication
This indication is used during a deactivation procedure to inform the U-transceiver that timing signals are needed no longer and that the U-transceiver may enter the deactivated (power-down) state.

DIN = 0 Binary “0” polarity on DIN
This asynchronous signal requests the U-transceiver to provide IOM clocks. Hereafter, binary “0s” in the C/I-channel (code TIM “0000” or any other code different from DI “1111”) keep the IOM-2 interface active.

DT Data Through
This unconditional command is used for test purposes only and forces the U-transceiver into a state equivalent to the “Transparent” state. The far-end transceiver is assumed to be in the same condition.

EI1 Error Indication 1
The S-transceiver indicates an error condition on its receive side (loss of frame alignment or loss of incoming signal). The U-transceiver informs the LT-side by setting the ACT-bit to “0” thus indicating that transparency has been lost.

RES Reset
Unconditional command which resets the whole U-transceiver; especially the EC- and EQ-coefficients are set to zero.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs.
The chip is in the “Test” state, the receiver will not be reset.

TIM Timing
The U-transceiver is requested to continue providing timing signals and not to leave the “Power-up” state.

Pins

Pin-Res Pin-Reset
Corresponds to a low-level at pin $\overline{\text{RES}}$ or a power-on reset. The function of this pin is the same as of the C/I-code RES. C/I-message DR will be issued.

Pin-SSP Pin-Send Single Pulses
Corresponds to a low-level at pins $\overline{\text{TM}}$/TM2 and a high-level at pins TM0/TM1 (refer to page 66). The function of this pin is the same as of the C/I-code SSP. C/I-message DR will be issued.

Pin-DT Pin-Data Through
Corresponds to a low-level at pins $\overline{\text{TM}}$/TM1 and a high-level at pins TM0/TM2 (refer to page 66). The function of this pin is the same as of the C/I-code DT. C/I-message DR will be issued.

U-Interface Events

The signals SLx, TL and SP received on the U-interface are defined in **table 12** on **page 69.**

ACT ACT-bit received from LT-side.

- ACT = 1 requests the U-transceiver to transmit transparently in both directions. As transparency in receive direction (U-interface to IOM) is already performed when the receiver is synchronized, the receipt of ACT = 1 establishes transparency in transmit direction (IOM to U-interface), too. In the case of loop-backs, however, transparency in both directions of transmission is established when the receiver is synchronized.
- ACT = 0 indicates that the LT-side has lost transparency.

DEA DEA-bit received from the LT-side

- DEA = 0 informs the U-transceiver that a deactivation procedure has been started by the LT-side.
- DEA = 1 reflects the case when DEA = 0 was detected by faults due to e.g. transmission errors and allows the U-transceiver to recover from this situation (see state 'Pend. Deact. U').

UOA UOA-bit received from network side

- UOA = 0 informs the U-transceiver that only the U-interface is to be activated. The S/T-interface must remain deactivated.
- UOA = 1 enables the S/T-interface to activate.

LOF Loss of Framing on the U-interface

This condition is fulfilled if framing is lost for 576 ms. 576 ms are the upper limit. If the correlation between synchronization word and the input signal is not optimal, LOF may be issued earlier.

LSEC Loss of Signal level behind the Echo Canceler
Internal signal which indicates that the echo canceler has converged.

LSU Loss of Signal level on the U-interface
This signal indicates that a loss of signal level for a duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the NT waits for a response (no signal level) from the LT-side, i.e. after a deactivation has been announced (receipt of DEA = 0), after the NT has lost framing, and after timer T1 has elapsed.

LSUE Loss of Signal level on the U-interface
After a loss of signal has been noticed, a 588 ms timer is started. When it has elapsed, the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the NT is not prepared to lose signal level i.e. the LT has stopped transmission because of loss of framing, an unsuccessful activation, or the transmission line is interrupted.
Note that 588 ms represent a minimum value; the actual loss of signal might have occurred earlier, e.g. when a long loop is cut at the NT-side and the echo coefficients need to be readjusted to the new parameters. Only after the adjusted coefficients cancel the echo completely, the loss of signal is detected and the timer can be started (if the long loop is cut at the remote end, the coefficients are still correct and loss of signal will be detected immediately).

SFD Superframe (ISW) Detected on U-interface

FD Frame (SW) Detected on U-interface

TL Wake-up signal received from the LT
The U-transceiver is requested to start an activation procedure. The TL-criterion is fulfilled when 12 consecutive periods of the 10-kHz wake-up tone were detected.
When in the “Pending Timing” state and automatic activation after reset is selected (Pin AUA=1), a recognition of TL is assumed every time the “Pending Timing” state has been entered from the “Test” state (caused by C/I code DI). This behavior allows the U-transceiver to initiate one single activation attempt after having been reseted.

BBD0/1 Binary “0s” or “1s” detected in the B- and D-channels
This internal signal indicates that for 6-12 ms, a continuous stream of binary “0s” or “1s” has been detected. It is used as a criterion that the receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD0 corresponds to the signal SL2 in the case of normal activation and BBD1 corresponds to the internally received signal SN3 in case of an analog loop back.

Timers

The start of timers is indicated by TxS, the expiry by TxE. The following **table 5** shows which timers are used by the U-transceiver:

Table 5 Timers

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T7	40	Hold time	Receive reset
T11	9	TN-transmission	Alerting
T12	5500	Supervisor EC-converge	EC-training
T13	15000	Frame synchronization	Pend. receive reset
T14	0.5	Hold time	Pend. timing

2.3.5.4 Outputs of the U-Transceiver

Signals and indications are issued on IOM-2 (C/I-indications) and on the U-interface (predefined U-signals).

C/I Indications

AI Activation Indication
The U-transceiver has established transparency of transmission in the direction IOM to U-interface. The S-transceiver is requested to send INFO4 and to achieve transparency of transmission in the direction IOM to S/T-interface.

AIL Activation Indication Loop-back
The U-transceiver has detected ACT = 1 while loop-back 2 is still established. The S-transceiver is requested to send INFO4 (if a transparent loop-back 2 is to be implemented) and to keep loop-back 2 active.

AR Activation Request
The U-receiver has synchronized on the incoming signal. The S-transceiver is requested to start the activation procedure on the S/T-interface by sending INFO2.

ARL Activation Request Loop-back
The U-transceiver has detected a loop-back 2 command in the EOC-channel and has established transparency of transmission in the direction IOM to U-interface. The S-transceiver is requested to send INFO2 (if a transparent loop-back 2 is to be implemented) and to operate loop-back 2.

DC Deactivation Confirmation
Idle code on the IOM-2 interface. The U-transceiver stays in the power-down mode unless an activation procedure has been started from the LT-side. The U-interface may be activated but the S/T-interface has to remain deactivated.

DR Deactivation Request
The U-transceiver has detected a deactivation request command from the LT-side for a complete deactivation or a S/T only deactivation. The S-transceiver is requested to start the deactivation procedure on the S/T-interface by sending INFO0.

EI1 Error Indication 1
The U-transceiver has entered a failure condition caused by loss of framing on the U-interface or expiry of timer T1.

MLT Metallic Loop Termination
The ANSI T1.601 maintenance controller has detected a valid pulse stream on pin MTI and has set the U-transceiver in the proper state. Indication MLT is issued in 4 consecutive IOM frames. Then the C/I-code of the actual U-transceiver state is issued again.

PU Power Up
The U-transceiver provides IOM-2 clocks.

Signals on U-Interface

The signals SNx, TN and SP transmitted on the U-interface are defined in **Table 12 on page 69**.
The polarity of the transmitted ACT-bit is as follows:

a = 0/1 corresponds to ACT-bit set to binary “0/1”

The polarity of the issued SAI-bit depends on the received C/I-channel code: DI and TIM leads to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating any activity on the S/T-interface.

2.3.5.5 NT-States

The following states are used:

Alerting

The wake-up signal TN is transmitted for a period of T11 either in response to a received wake-up signal TL or to start an activation procedure on the LT-side.

Alerting 1

“Alerting 1” state is entered when a wake-up tone was received in the “Receive Reset” state and the deactivation procedure on the NT-side was not yet finished. The transmission of wake-up tone TN is started.

Analog Loop-Back

Upon detection of binary “1s” for a period of 6–12 ms and of the superframe indication, the “Analog loop-back” state is entered and transparency is achieved in both directions of transmission. This state can be left by making use of any unconditional command. Only the C/I-channel code RES should be used, however. This assures that the EC- and EQ-coefficients are set to zero and that for a subsequent normal activation procedure the receiver updating algorithms converge correctly.

Deactivated

The 'Deactivated' state is a power-down state. If there are no pending Monitor channel messages from the U-transceiver, i.e. all Monitor channel messages have been acknowledged, the IOM-clocks are turned off. No signal is sent on the U-interface.
The U-transceiver waits for a wake-up signal TL from the LT-side to start an activation procedure. To enter state 'IOM Awake' a wake-up signal (DIN = 0) is required if the IOM-clocks are disabled. The wake-up signal is provided by the S-transceiver after an activation from a terminal on the S-bus. If the IOM-clocks were active in state 'Deactivated' C/I-code TIM is sufficient for a transition to state 'IOM Awake'.

EC Training

The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The "EC-training" state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

EC-Training 1

The "EC-Training 1" state is entered if transmission of signal SN1 has to be started and the deactivation procedure on the NT-side is not yet finished.

EC-Training AL

This state is entered in the case of an analog loop-back. The signal SN1 is transmitted on the U-interface to allow the NT-receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The "EC-training" state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

EQ-Training

The receiver waits for signal SL1 or SL2 to be able to update the AGC, to recover the timing phase, to detect the synch-word (SW), and to update the EQ-coefficients. The "EQ-training" state is left upon detection of binary "0s" in the B- and D-channels for a period of 6–12 ms corresponding to the detection of SL2.

Error S/T

Loss of framing or loss of incoming signal has been detected on the S/T-interface (EI1). The LT-side is informed by setting the ACT-bit to "0" (loss of transparency on the NT-side). The following codes are issued on the C/I-channel:

- Normal activation or single-channel loop-back: AR
- Loop-back 2: ARL

IOM®-2 Awaked

Timing signals are delivered on the IOM-2 interface. The U-transceiver enters the “Deactivated” state again upon detection of the C/I-channel code DI (idle code).

Pending Deactivation of S/T

The U-transceiver has received the UOA-bit at zero after a complete activation of the S/T-interface. The U-transceiver deactivates the S/T-interface by issuing DR in the C/I-channel. The value of the ACT-bit depends on its value in the previous state.

Pending Deactivation of U-Interface

The U-transceiver waits for the receive signal level to be turned off (LSU) to enter the “Receiver Reset” state and start the deactivation procedure.

Pending Receive Reset

The “Pending Receive Reset” state is entered upon detection of loss of framing on the U-interface or expiry of timer T1. This failure condition is signalled to the LT-side by turning off the transmit level (SN0). The U-transceiver then waits for a response (no signal level LSU) from the LT-side to enter the “Receive Reset” state.

Pending Timing

The “Pending timing“ state assures that the C/I-channel code DC is issued four times before the timing signals on the IOM-2 interface are turned off.
In case pin AUA=1 is selected the recognition of the LT wake-up tone TL is assumed everytime the “Pending Timing” state has been entered from the “Test” state. This function guarantees that the NT starts one single activation attempt after having been resetted. After the assumed TL recognition in this state the activation will proceed normally.

Receive Reset

The “Receive Reset” state is entered upon detection of a deactivation request from the LT-side, after a failure condition on the U-interface (loss of signal level LSUE), or following the “Pending Reset” state upon expiry of timer T1 or loss of framing. No signal is transmitted on the U-interface, especially no wake-up signal TN, and the S-transceiver or microcontroller is requested to start the deactivation procedure on the NT-side (DR). Timer T7 assures that no activation procedure is started from the NT-side for a minimum period of T7. This gives the LT a chance to activate the NT.
The state is left only after completion of the deactivation procedure on the NT-side (receipt of the C/I-channel code DI), unless a wake-up tone is received from the LT-side.

Synchronized 1

When reaching this state the U-transceiver informs the LT-side by sending the superframe indication (inverted synch.-word). The loop-back commands decoded by the EOC-processor control the output of the transmit signals:

- Normal ACT and UOA = 0: SN3
- Any loop-back and UOA = 0 (no loop-back): SN3T

The value of the issued SAI-bit depends on the received C/I-channel code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity on the S/T-interface. The U-transceiver waits for the receipt of UOA = 1 to enter the “Synchronized 2” state.

Synchronized 2

In this state the U-transceiver has received UOA = 1. This is a request to activate the S/T-reference point. The loop-back commands detected by the EOC-processor control the output of indications and transmit signals:

- Normal activation and UOA = (1): SN3 and AR
- Single channel loop-back and UOA = (1): SN3T and AR
- Loop-back 2 (LBBD): SN3T and ARL

The value of the issued SAI-bit depends on the received C/I-channel code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity on the S/T-interface. The U-transceiver waits for the receipt of the C/I-channel code AI to enter the “Wait for ACT” state.

Test

The “Test” mode is entered when the unconditional commands RES, SSP, Pin-RES or Pin-SSP are used. It is left when normal U-transceiver operation is selected via pinstrapping of $\overline{TM}$ and TM0-2 (table on page 66) and the C/I-channel codes DI or ARL are received.

The following signals are transmitted on the U-interface:

- No signal level (SN0) when the C/I-channel code RES is applied or a hardware reset is activated.
- Single pulses (SP) when the C/I-channel code SSP is applied or $\overline{TM}$=TM2=0 & TM0=TM1=1.

Transparent

This state is entered upon the detection of ACT = 1 received from the LT-side and corresponds to the fully active state. In the case of a normal activation in both directions of transmission the the following codes are output:

– Normal activation or single-channel loop-back: AI
– Loop-back 2: AIL

Wait for ACT

Upon the receipt of AI, the ACT-bit is set to “1” and the NT waits for a response (ACT = 1) from the LT-side. The output of indications and transmit signals is as defined for the “Synchronized” state.

Wait for SF

Upon detection of SL2, the signal SN2 is sent on the U-interface and the receiver waits for detection of the superframe indication. Timer T1 is then stopped and the “Synchronized” state is entered.

Wait for SF AL

This state is entered in the case of an analog loop-back and allows the receiver to update the AGC, to recover the timing phase, and to update the EQ-coefficients. Signal SN3 is sent instead of signal SN2 in the “Wait-for-SF” state.

2.3.6 C/I Codes

Both commands and indications depend on the data direction. **Table 6** presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM frames (Double last-look criterion). Indications are strictly state orientated. Refer to the state diagrams in the previous sections for commands and indications applicable in various states.

Table 6 U-Transceiver C/I Codes

Code	NT Mode	
	IN	OUT
0000	TIM	DR
0001	RES	–
0010	–	–
0011	–	–
0100	EI1	EI1
0101	SSP	–
0110	DT	MLT
0111	–	PU
1000	AR	AR
1001	–	–
1010	ARL	ARL
1011	–	–
1100	AI	AI
1101	–	–
1110	–	AIL
1111	DI	DC

AI	Activation Indication	EI1	Error Indication 1
AR	Activation Request	MLT	Metallic Loop Termination
ARL	Activation Request Local Loop	PU	Power-Up
DC	Deactivation Confirmation	RES	Reset
DI	Deactivation Indication	SSP	Send-Single-Pulses test mode
DR	Deactivation Request	TIM	Timing request
DT	Data-Through test mode		

2.3.7 Loop-Back #2

Loop-back #2 is specified by the national PTTs in order to facilitate the location of defect systems. Loop-back #2 commands are recognized and executed automatically by the NTC-Q.

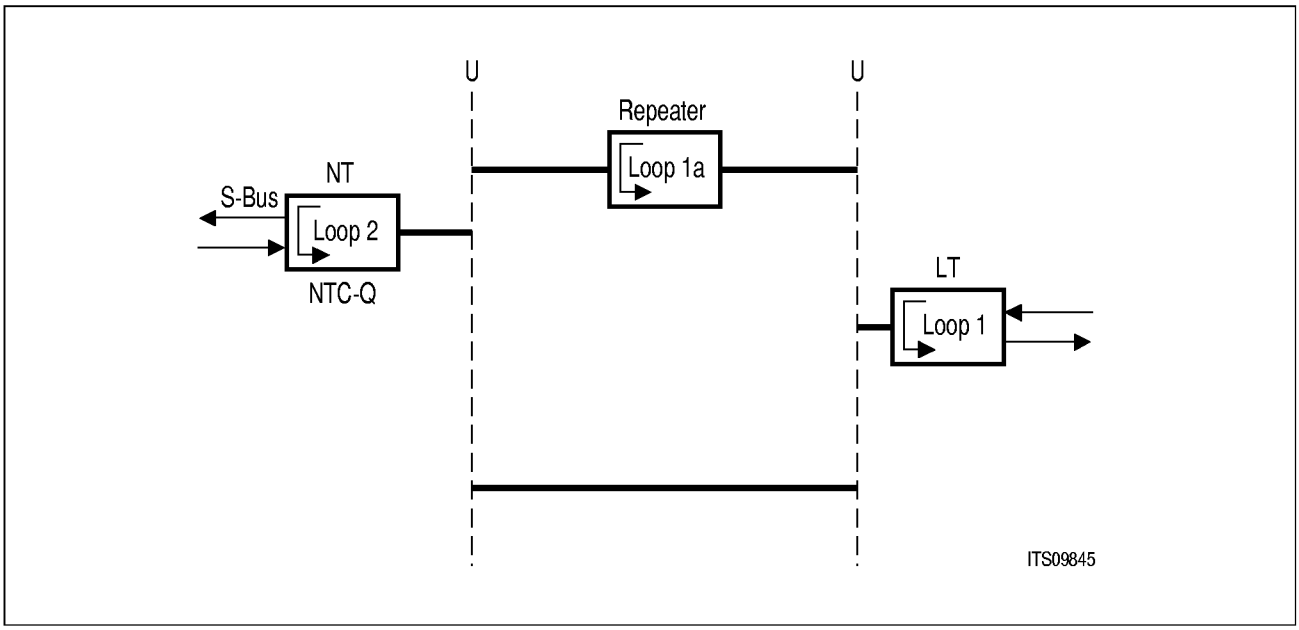


Figure 18 Test Loop-Backs

Loop-back #2 is controlled by the exchange using the EOC commands LBBD, LB1 and LB2. The loop-back is transparent which means that all bits that are looped back are also passed on to the S-bus. All loop-backs are opened when the EOC command RTN is sent by the LT.

Complete loop-back

The complete loop-back (LBBD) comprises both B-channels and the D-channel. It is closed in the NTC-Q as close to the S-transceiver as possible. The U-transceiver passes the request on to the IOM-2 interface. This is achieved by issuing the C/I-code AIL in the “Transparent” state or C/I = ARL in states different than “Transparent”. Please refer to page 33 for details on how to set pin AL2 regarding the differences between ETSI and ANSI standards.

Single-channel loop-back (B1/B2)

Single-channel loop-backs (LB1, LB2) are always performed directly in the U-transceiver. The B1-channel is closed with the EOC-command LB1. LB2 causes the channel B2 to loop-back. Because these functions are latched, both channels may be looped back simultaneously by sending first the command to close one channel followed by the command for the remaining channel.

2.3.8 Analog Line Port

The analog part of the U-transceiver consists of three main building blocks:

– The analog-to-digital converter in the receive path
– The digital-to-analog converter in the transmit path
– The output buffer in the transmit path

Furthermore it contains some special functions. These are:

– Analog test loop-back
– Level detect function

Analog-to-Digital Converter

The ADC is a sigma-delta modulator of second order using a clock rate of 15.36-MHz.

The peak input signal measured between AIN and BIN must be below 4 Vpp. In case the signal input is too low (long range), the received signal is amplified internally by 6 dB. The maximum signal to noise ratio is achieved with 1.3 Vpp (long range) and 2.6 Vpp (short range) input signal voltage.

Digital-to-Analog Converter

The output pulse is shaped by a special DAC. The DAC was optimized for excellent matching between positive and negative pulses and high linearity. It uses a fully differential capacitor approach. The staircase-like output signal of the DAC drives the output buffers. The shape of a DAC-output signal is shown in **figure 19**, the peak amplitude is normalized to one. This signal is fed to an RC-lowpass of first order with a corner frequency of 1 MHz ± 50%.

The duration of each pulse is 24 steps, with T0 = 0.78 µs per step. On the other hand, the pulse rate is 80-kHz or one pulse per 16 steps. Thus, the subsequent pulses are overlapping for a duration of 8 steps.

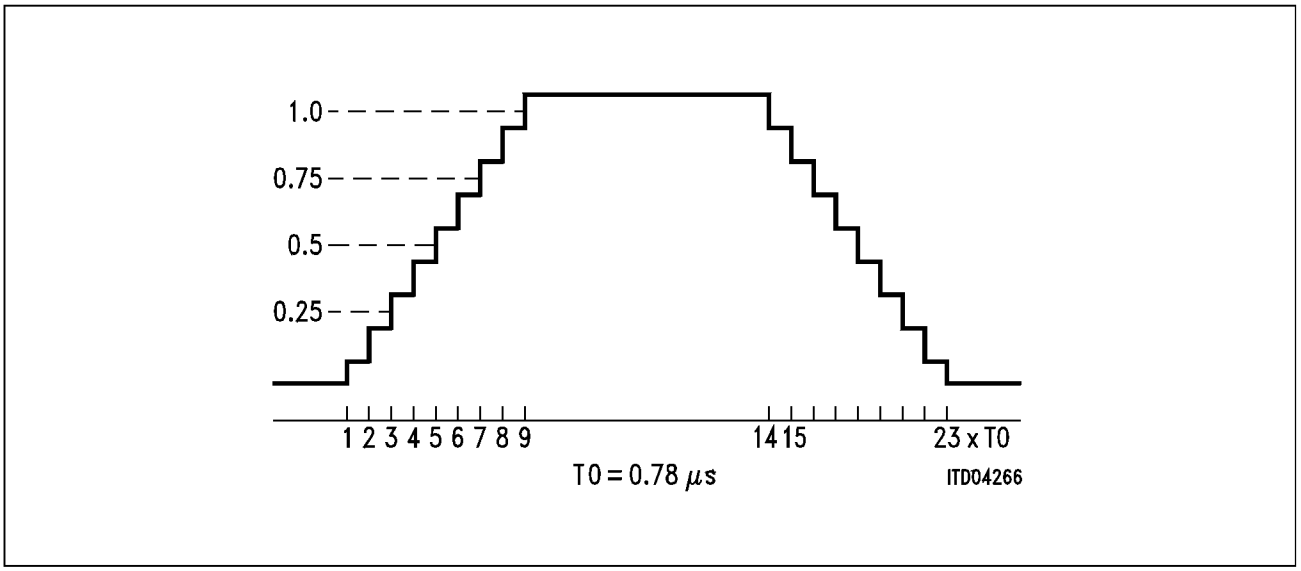


Figure 19 DAC-Output for a Single Pulse

Output Stage

The output stage consists of two identical buffers, operated in a differential mode. This concept allows an output-voltage swing of 6.4 Vpp at the output pins of the U-transceiver. The buffers are optimized for:

– High output swing
– High linearity
– Low quiescent current to minimize power consumption

The output jitter produced by the transmitter (with jitter-free input signals) is below 0.02 UIpp (Unit intervall = 12.5 µs, peak-peak) measured with a high-pass filter of 30-Hz cutoff frequency. Without the filter the cutoff frequency is below 0.1 UIpp.

Analog Loop-Back Function

The loop-back C/I command ARL activates an internal, analog loop-back. This loop-back is closed near the U-interface. All signals received on AIN / BIN will neither be evaluated nor recognized after reaching the “Synchronized” state.

Level Detect

The level detect circuit evaluates the differential signal between AIN and BIN. The differential threshold level is between 4 mV and 28 mV. The DC-level (common mode level) may be between 0 V and 3 V. Level detect is not effected by the range setting.

Pulse Shape

The pulse mask for a single positive pulse measured between AOUT and BOUT at a load of 98 Ω is given in the following figure.

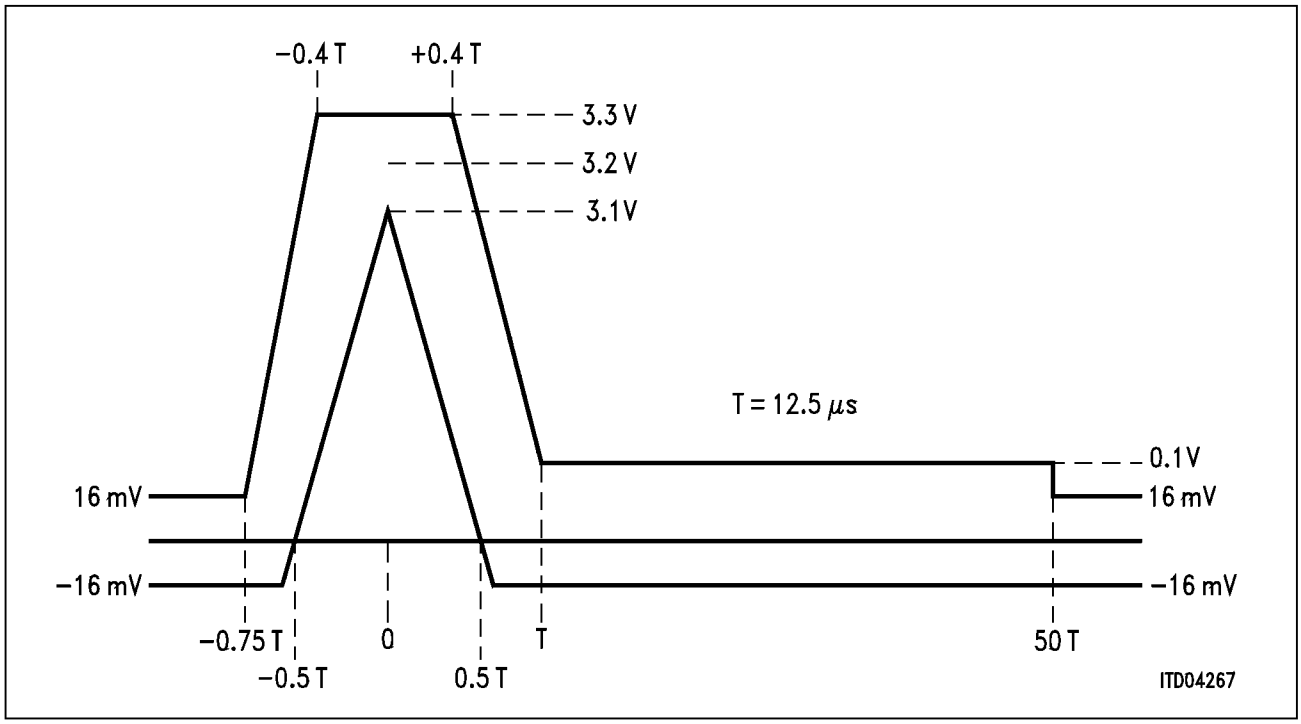


Figure 20 Pulse Mask for a Single Positive Pulse

Hybrid

Please refer to page 80 for the external circuitry of the U-transceiver.

2.3.9 Metallic Loop Termination

For North American applications a maintenance controller according to ANSI T1.601 section 6.5 is implemented. The maintenance pulse stream from the U-interface Metallic Loop Termination circuit (MLT) is fed to pin MTI, usually via an optocoupler. It is digitally filtered for 20ms and decoded by the maintenance controller according to **table 7**. The NTC-Q automatically sets the U-transceiver in the proper state and issues C/I code MLT ('0110') for 4 consecutive IOM-frames.

A test mode is valid for 75 seconds. If during the 75 seconds a valid pulse sequence is detected the 75 s timer starts again. After expiry of the 75 s timer the U-transceiver goes back to normal operation.

Table 7 ANSI Maintenance Controller States

Number of counted pulses	ANSI maintenance controller state	U-transceiver State Machine
<= 5	ignored	no impact
6	Quiet Mode	transition to state 'Test'
7	ignored	no impact
8	Insertion Loss Measurement	transition to state 'Transparent'
9	ignored	no impact
10	normal operation	back to normal operation
>= 10	ignored	no impact

Figure 21 shows an example for a pulse stream selecting Quiet Mode.

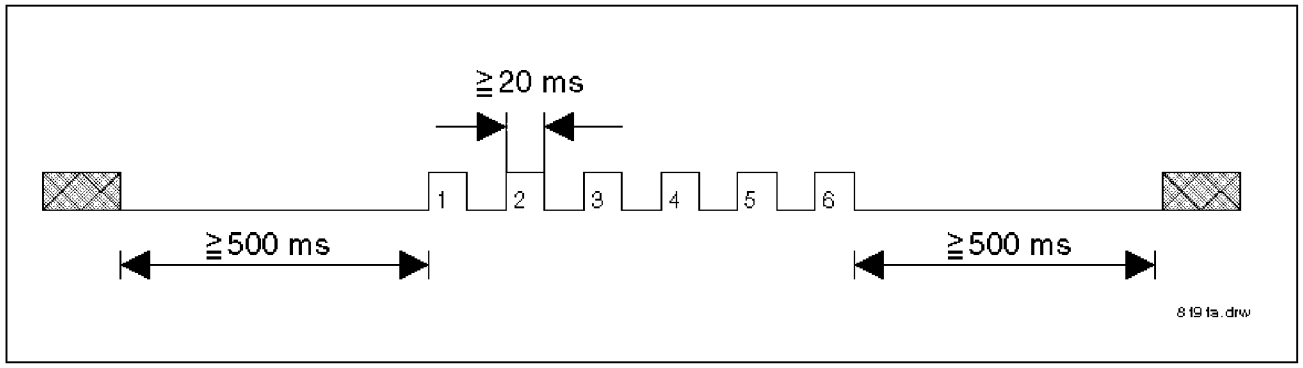


Figure 21 Pulse Stream Selecting Quiet Mode

2.4 S-Transceiver

Transmission over the S/T-interface is performed at a rate of 192 kbit/s. Pseudo-ternary coding with 100 % pulse width is used. 144 kbit/s are used for user data (B1+B2+D), 48 kbit/s are used for framing and maintenance information. The NTC-Q uses two symmetrical, differential outputs (SX1, SX2) and two symmetrical, differential inputs (SR1, SR2). These signals are coupled via external circuitry (page 81) and two transformers onto the 4 wire S-interface. The nominal pulse amplitude on the S-interface is 750 mV (zero-peak).

2.4.1 Modes

In NT1 applications (pin DCLSEL = '1', DCL=512 kHz) the S-transceiver is in NT mode.

However, if pin DCLSEL = '0' (DCL=1.536 MHz) the S-transceiver is in LT-S mode. Depending on pin ICS the S-transceiver is then mapped to IOM channel 0 or 1. If mapped to channel 1 the internal registers of the S-transceiver can be accessed via the Monitor channel. For a description of the S-transceiver's internal registers and S/Q channel access please refer to the data sheet of the PEB 8191 (INTC-Q) or the PEB 2081 (SBCX) User's Manual. For a description of the LT-S mode state machine please refer to page 136 of the SBCX User's Manual.

Common functions in all operating modes are:

- line transceiver functions for the S/T interface according to the electrical specifications of ITU I.430 and ETSI ETS 300 012;
- conversion of the frame structure between IOM and S/T interface;
- conversion from/to binary to/from pseudo-ternary code;
- level detect.
- receive timing recovery for point-to-point, passive bus and extended passive bus configuration;
- S/T timing generation using IOM timing synchronous to system;
- D-channel echo bit generation by handling of the global echo bit;
- activation/deactivation procedures, triggered by primitives received over the IOM C/I channel or by INFO's received from the line;
- execution of test loops.

The wiring configurations in user premises, in which the NTC-Q can be used are illustrated in **figure 22**.

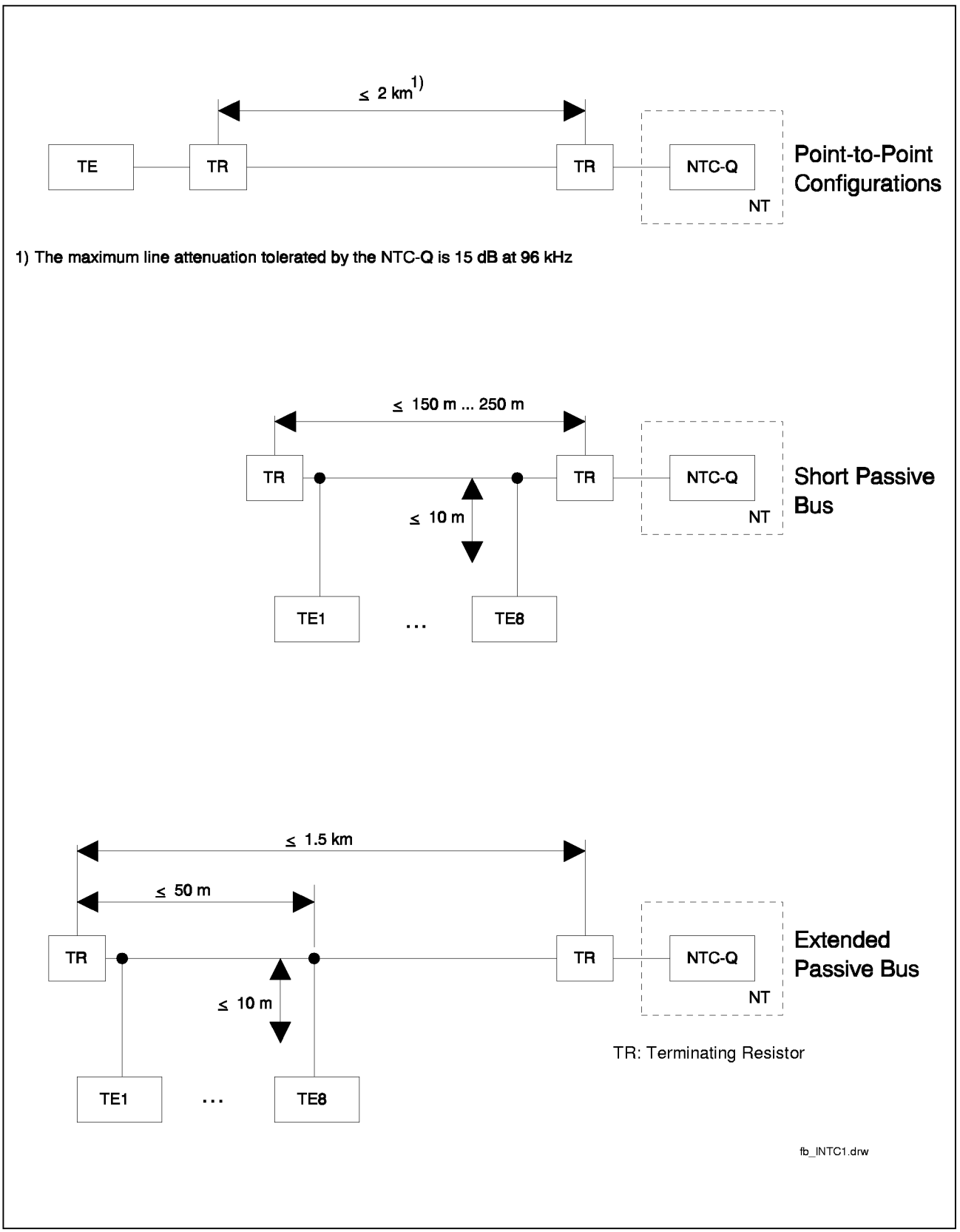


Figure 22 Wiring Configurations in User Premises

2.4.2 S/T-Interface Coding

The following figure illustrates the code used. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with a single exception: the first binary ZERO following the framing balance bit is of the same polarity as the framing-balancing bit (required code violation).

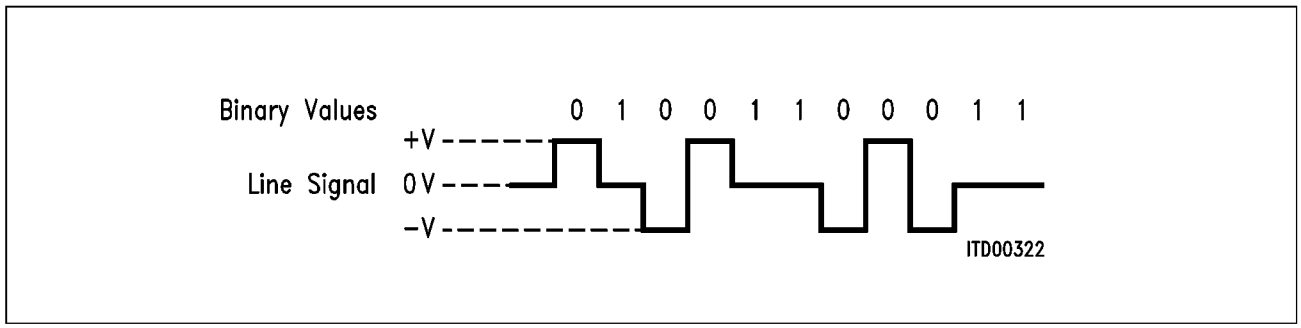


Figure 23 S/T -Interface Line Code (without code violation)

A standard S/T frame consists of 48 bits. In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

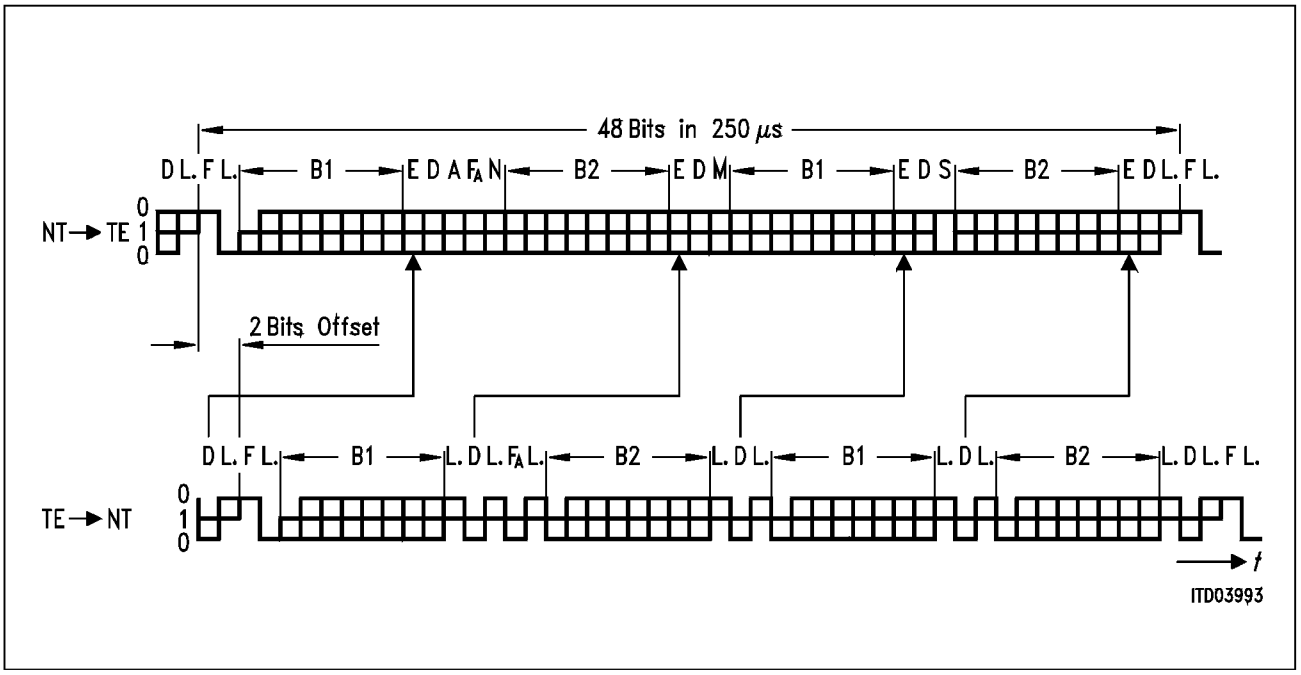


Figure 24 Frame Structure at Reference Points S and T (ITU I.430)

–F	Framing Bit	F = (0b) → identifies new frame (always positive pulse)
–L.	D.C. Balancing Bit	L. = (0b) → number of binary ZEROs sent after the last L. bit was odd
–D	D-Channel Data Bit	Signalling data specified by user
–E	D-Channel Echo Bit	E = D → no D-channel collision. ZEROs overwrite ONEs
–F_A	Auxiliary Framing Bit	See section 6.3 in ITU I.430
–N		N = $\overline{F_A}$
–B1	B1-Channel Data Bit	User data
–B2	B2-Channel Data Bit	User data
–A	Activation Bit	A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
–S	S-Channel Data Bit	S_1 or S_2 channel data
–M	Multiframing Bit	M = (1b) → Start of new multi-frame

2.4.3 State Machine Notation

The state machines include all the information necessary for the user to understand and predict the behavior of the S-transceiver. The information contained in a state bubble is:

State (state name, based on ITU I.430), i_x (S/T signal transmitted), i_r (S/T signal received), ***Ind.*** (C/I code transmitted) and ***Cmd.*** (C/I code received). Received S/T signals and C/I codes are transition criterias.

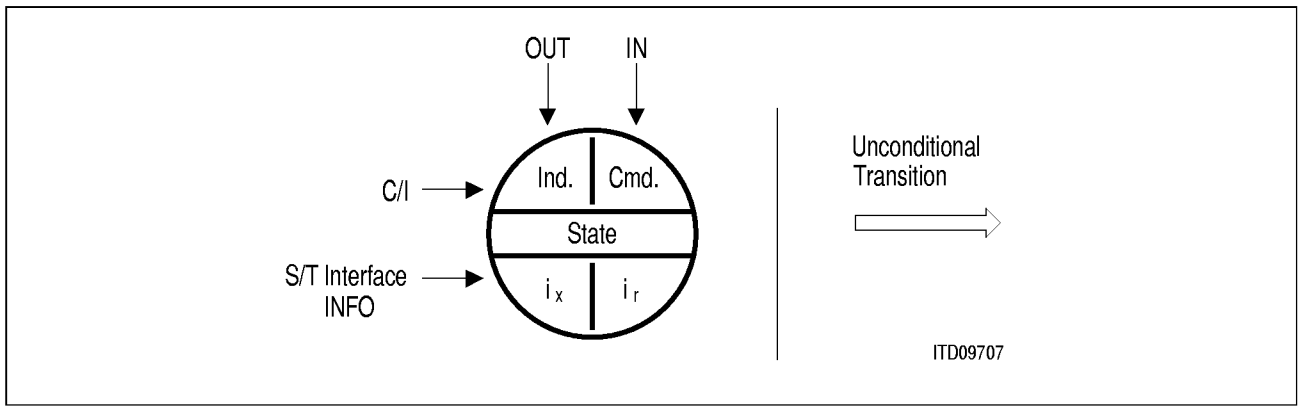


Figure 25 State Diagram Notation S-Transceiver

The following example illustrates the use of a state diagram with an extract of the NT state diagram (**page 58**). The explained state is “G1 $\overline{i0}$ Detected”.

Example:

The state may be entered:

–from state “Deactivated” after $\overline{i0}$ has been received.

The following S/T signal and C/I code are transmitted:

–INFO 0 (no signal) is sent on the S/T-interface.
–C/I message “AR” is issued on the IOM-2 interface.

The state is be left at occurrence of one of the following events:

–Leave for the state “G2 Pend. Act” after “ARD” code has been received on IOM-2.
–Leave for the state “G4 Pend. Deact.” in case C/I = DR is received.

Combinations of multiple conditions are possible as well. A “&” stands for a logical AND combination. An “or” indicates a logical OR combination. Negated arguments are overlined (e.g. $\overline{X}$).

2.4.4 State Machine NT Mode

2.4.4.1 NT Mode State Diagram

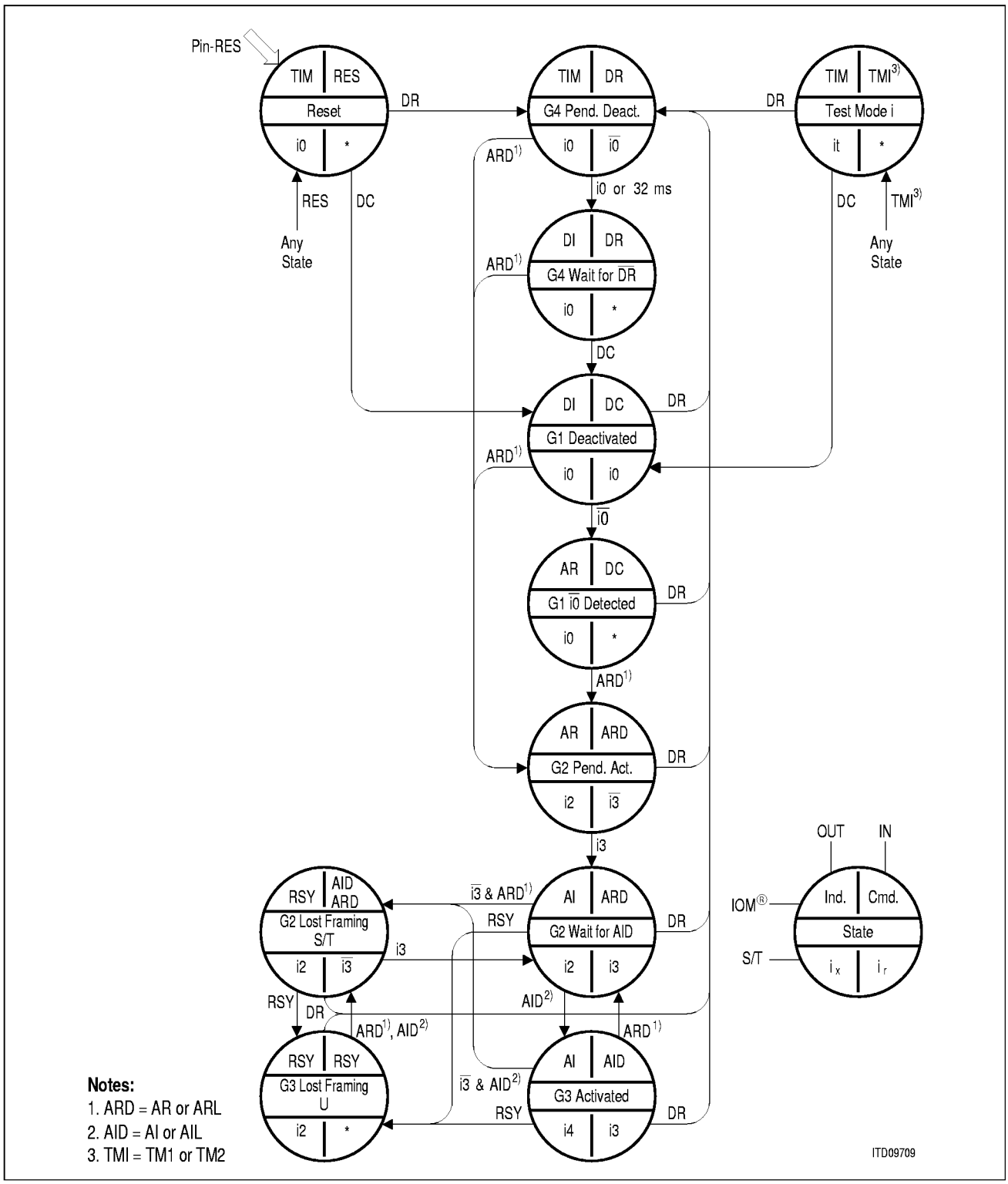


Figure 26 NT Mode State Diagram

2.4.4.2 Inputs to the S-Transceiver in NT Mode

The transition criteria used by the S-transceiver are described in the following sections. They are grouped into:

–C/I commands
–Pin states
–Events on the S/T-interface.

C/I Commands

AR Activation Request. This command is used to start an exchange initiated activation.

ARL Activation request loop. The S-transceiver is requested to operate an analog loop-back close to the S/T-interface.

AI Activation Indication. Confirms that the U-interface is fully transparent, D-channel data transfer is allowed.

AIL Activation Indication loop. Command to close the analog loop on the S-interface.

DC Deactivation Confirmation. Transfers the S-transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled).

DR Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. Unconditional command.

RES Reset of state machine. Transmission of Info 0. No reaction to incoming infos. RES is an unconditional command.

RSY Resynchronizing. The U-interface has not obtained or lost synchronization. INFO 2 is transmitted consequently by the S-transceiver.

TM1 Test Mode 1. Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. TM1 is an unconditional command.

TM2 Test Mode 2. Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is an unconditional command.

Pin States

Pin-$\overline{\text{RES}}$ Pin-Reset. Corresponds to a low level at pin $\overline{\text{RES}}$ or a power-on reset. The function of this pin is identical to the C/I code RES concerning the state machine.

Pin-TM1 Selected if pins $\overline{\text{TM}}$=TM0=0 and TM1=TM2=1. Transfers the S-transceiver into the “Test mode i” state. Here a 2-kHz signal of alternating pulses is transmitted on the S/T-interface.

Pin-TM2 Selected if pins $\overline{\text{TM}}$=TM0=TM2=0 and TM1=1.Transfers the S-transceiver into “Test Mode i” state. Here a signal consisting of continuous binary ZEROs is sent at the rate of 96 kHz.

S/T-Interface Events

i0 INFO 0 detected

$\overline{\text{i0}}$ Level detected (any signal different from I0)

i3 INFO 3 detected

$\overline{\text{i3}}$ Any INFO other than INFO 3.

2.4.4.3 Outputs of the S-Transceiver in NT Mode

The following signals and indications are issued on the IOM-2 and S/T-interface.

C/I Indications

TIM Timing. S-transceiver requires clock pulses.

RSY Resynchronizing. Receiver is not synchronous.

AR Activate request. $\overline{\text{INFO 0}}$ or command AR received.

AI Activate indication. Synchronous receiver.

DI Deactivation Indication. Timer (32 ms) expired or INFO 0 received after received C/I code DR.

S/T-Interface Signals

The signals transmitted on the S-interface are defined in **Table 11 on page 68.**

i0 INFO 0

i2 INFO 2

i4 INFO 4

it Pseudo ternary pulses at 2-kHz frequency (TM1).
Pseudo ternary pulses at 96-kHz frequency (TM2).

2.4.4.4 States NT Mode

G1 Deactivated

The S-transceiver is not transmitting. No signal is detected on the S/T-interface, and no activation command is received in C/I channel. DI is output in the normal deactivated state, and TIM is output as a first step when an activation is requested from the S/T-interface ($\overline{i0}$).

G1 $\overline{I0}$ Detected

An $\overline{\text{INFO 0}}$ is detected on the S/T-interface, translated to an “Activation Request” indication in the C/I channel. The S-transceiver is waiting for an AR command, which normally indicates that the transmission line upstream (the two-wire U interface) is synchronized.

G2 Pending Activation

As a result of the ARD command INFO 2 is sent on the S/T-interface. INFO 3 is not yet received.

G2 wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the S-transceiver waits for a “switch-through” command AID from the device upstream.

G3 Activated

INFO 4 is sent on the S/T-interface as a result of the “switch through” command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

G2 Lost Framing S/T

This state is reached when the S-transceiver has lost synchronism in the state ’G3 activated’ or ’G2 Wait for AID’.

G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the two-wire U interface, the S-transceiver transmits INFO 2.

G4 Pend. Deact.

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state “G4 wait for $\overline{DR}$”) is issued by the S-transceiver when:

– either INFO0 is received
– or an internal timer of 32 ms expires.

G4 wait for $\overline{DR}$

Final state after a deactivation request. The S-transceiver remains in this state until an C/I code DC is received.

Test Mode 1

Single alternating pulses are sent on the S/T-interface (2-kHz repetition rate).

Test Mode 2

Continuous alternating pulses are sent on the S/T-interface (96 kHz).

Reset state

A hardware or software reset (RES) forces the S-transceiver to an idle state where the analog components are disabled (transmission of INFO0) and the S/T line awake detector is inactive. Thus activation from the NT is not possible.

2.4.5 C/I Codes

Both commands and indications depend on the data direction. **Table 8** presents all defined C/I codes. A new command or indication will be recognized as valid after it has been detected in two successive IOM frames (Double last-look criterion). Indications are strictly state orientated. Refer to the state diagrams in the previous sections for commands and indications applicable in various states.

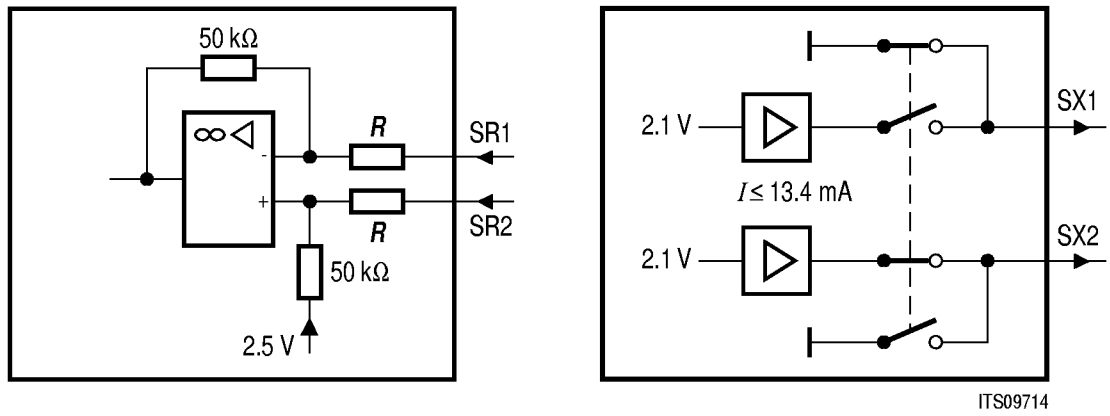
Table 8 S-Transceiver C/I Codes

Code	NT	
	IN	**OUT**
0000	DR	TIM
0001	RES	–
0010	TM1	–
0011	TM2	–
0100	RSY	RSY
0101	–	–
0110	–	–
0111	–	–
1000	AR	AR
1001	–	–
1010	ARL	–
1011	–	–
1100	AI	AI
1101	–	–
1110	AIL	–
1111	DC	DI

AI Activation Indication
AIL Activation Indication Loop
AR Activation Reques
ARL Activation Request Loop
DC Deactivation Confirmation
DI Deactivation Indication
DR Deactivation Request
RES Reset
RSY Resynchronizing
TIM Timer
TIM1 Test Mode 1 (2-kHz signal)
TM2 Test Mode 2 (96-kHz signal)

2.4.6 Analog Line Port

The equivalent circuits of the integrated receiver and transmitter stages are shown in **figure 27**.



R = 40 kΩ if transformer ratio is 2:1
R = 20 kΩ if transformer ratio is 1:1

Figure 27 Receiver and Transmitter Stages

The S-bus receiver is designed as a threshold detector with adaptively switched threshold levels. Pin SR1 delivers 2.5 V as an output, which is the virtual ground of the input signal on pin SR2. The S-bus receiver is symmetrical, which allows for a simple external circuitry and printed circuit board layout to meet the I.430 receiver input impedance specification.

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as two current limited voltage sources. A voltage of 2.1 V is delivered between SX1-SX2, which yields a current of 7.5 mA over 280 Ω.

S/T-Interface Circuitry

Please refer to page 81 for the external circuitry of the S-transceiver.

2.4.7 Timing Recovery

The transmit PLL (XPLL) synchronizes a 192 kHz transmit bit clock to the IOM-2 clock FSC (8 kHz).

– In a point-to-point or extended bus configuration the Receive PLL (RPLL) recovers bit timing from the detector´s output signal and provides a synchronous 1536-kHz clock (adaptive timing recovery from the receive data stream on the S-interface). Divided by eight this clock is used as 192-kHz receive data clock (PP).
– In a passive bus configuration, a 192-kHz receive clock (MP) generated by the transmit PLL (XPLL) is used to sample the input data (fixed timing recovery).

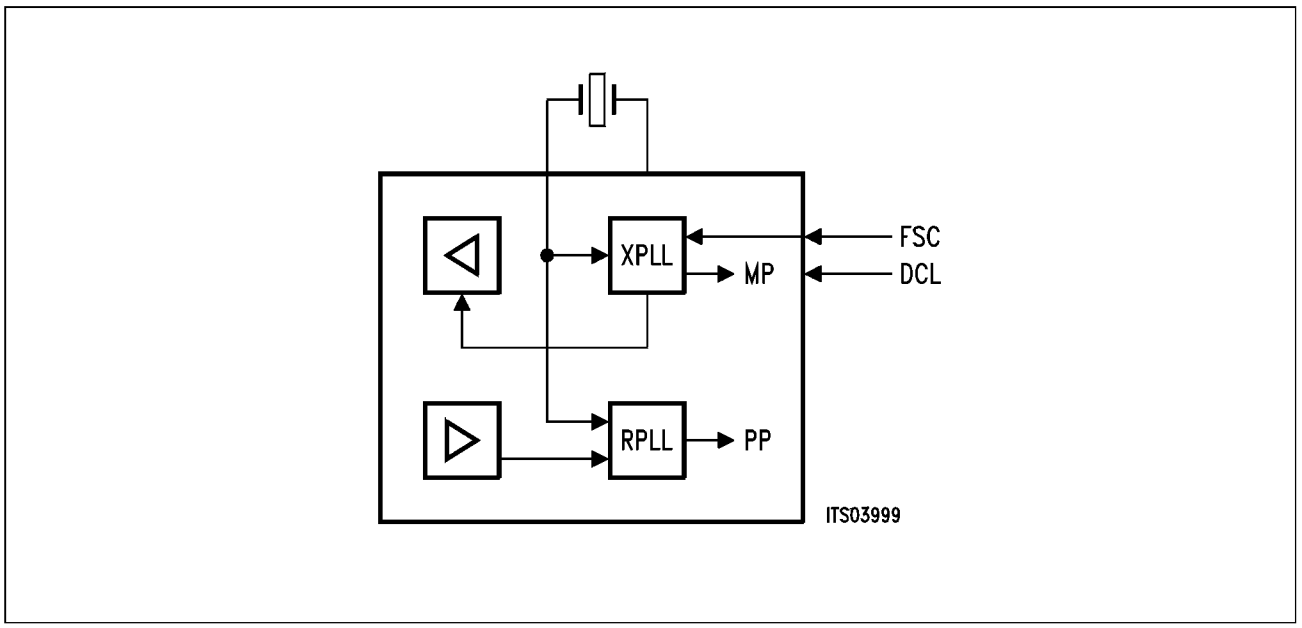


Figure 28 Clock System of the S-Transceiver

2.5 LED

An LED can be connected to pin $\overline{\text{ACT}}$ to display four different states (off, slow flashing, fast flashing, on). It displays the activation status of the U-and S-transceiver according to **table 9**.

Table 9 LED States

Pin $\overline{\text{ACT}}$	LED	U- and S-interface states
high Z	off	S- and U-interface deactivated
8Hz	8Hz	U activating or problem on U
1Hz	1Hz	U active; S activating or problem on S
GND	on	S and U activated

2.6 Reset

The NTC-Q contains a power-on reset which resets the U- and the S-transceiver. The NTC-Q can also be reset by applying an external reset impulse on pin $\overline{\text{RES}}$. The IOM-2 clocks DCL and FSC are delivered during a reset.

2.7 Test Modes

If pin $\overline{\text{TM}}$ is tied to GND the different test modes are selected via pins TM0-2 according to **table 10**.

Table 10 Test Modes

$\overline{\text{TM}}$	TM0	TM1	TM2	U-transceiver	S-transceiver
1	x[1)]	x	x	normal operation, IOM-2 interface disabled	
0	0	0	0	Quiet Mode	normal operation
0	0	0	1	reserved	
0	0	1	0	normal operation	Test Mode 2
0	0	1	1		Test Mode 1
0	1	0	0	reserved	
0	1	0	1	Data Through	normal operation
0	1	1	0	Send Single Pulses	
0	1	1	1	normal operation, IOM-2 interface active	

1) 'x' means: don't care

In **Test Mode 1** the S-transceiver transmits pseudo-ternary pulses at a rate of 2 kHz.

In **Test Mode 2** the S-transceiver transmits pseudo-ternary pulses at a rate of 96 kHz.

Send Single Pulses forces the U-transceiver to go into state 'Test' and to send single pulses. It has the same effect on the U-transceiver as C/I code SSP has. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs. Send Single Pulses is selected for the following measurements as defined in ANSI T1.601:

- Pulse Mask measurement

Data Through forces the U-transceiver into the state 'Transparent' where it transmitts signal SN3T. It has the same effect on the U-transceiver as C/I code DT has. Data Through is selected for the following measurements as defined in ANSI T1.601:

- Power Spectral-Density measurement
- Total Power measurement
- Insertion Loss measurement

Quiet Mode forces the U-transceiver into the state 'Test'. It has the same effect on the U-transceiver as C/I code RES has. Quiet Mode is selected for the following measurements as defined in ANSI T1.601:

- Quiet Mode measurement
- Return-Loss measurement

Note: Pins TM and TM0-2 can be left open in applications that do not require the test modes (internal pull-up resistors).

3 Operational Description

3.1 Layer 1 Activation/Deactivation

This chapter illustrates the interactions during activation and deactivation between the U- and the S-interface. The information presented in this section is extracted from the U- and S-transceiver state machines.

All S/T-interface signals used in the following sections as defined by ITU I.430 are explained in **table 11**. **Table 12** shows all U-interface signals as defined by ANSI.

Table 11 S/T-Interface Signals

Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal.	INFO 0	No signal.
		INFO 1	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs.
INFO 2	Frame with all bits of B, D, and D-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.		
		INFO 3	Synchronized frames with operational data on B and D-channels.
INFO 4	Frames with operational data on B, D, and D-echo channels. Bit A set to binary ONE.		

Table 12 U-Interface Signals

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
NT –> LT				
TN [1]	± 3	± 3	± 3	± 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
LT –> NT				
TL [1]	± 3	± 3	± 3	± 3
SL0	no signal	no signal	no signal	no signal
SL1	present	absent	1	1
SL2	present	present	0	normal
SL3 [2]	present	present	0	normal
SL3T	present	present	normal	normal
Test Mode				
SP [3]	no signal	no signal	± 3	no signal

Notes: [1] Alternating ± 3 symbols at 10 kHz

[2] Must be generated by the exchange

[3] Alternating ± 3 single pulses of 12.5 µs duration spaced by 1.5 ms

Complete Activation Initiated by Exchange

Figure 29 depicts the procedure if activation has been initiated by the exchange side (LT).

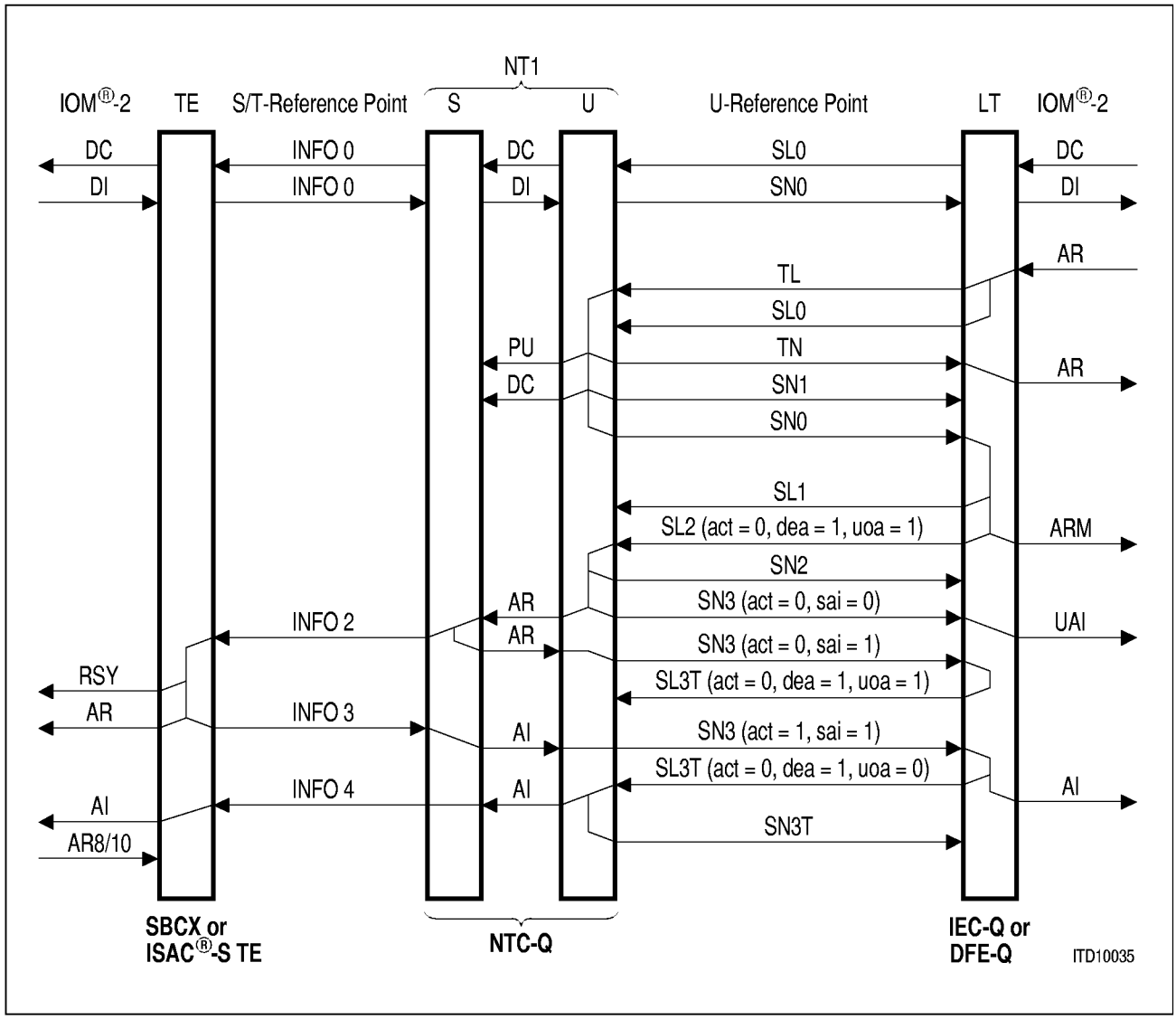


Figure 29 Complete Activation Initiated by Exchange

Complete Activation Initiated by TE

Figure 30 depicts the procedure if activation has been initiated by the terminal side (TE).

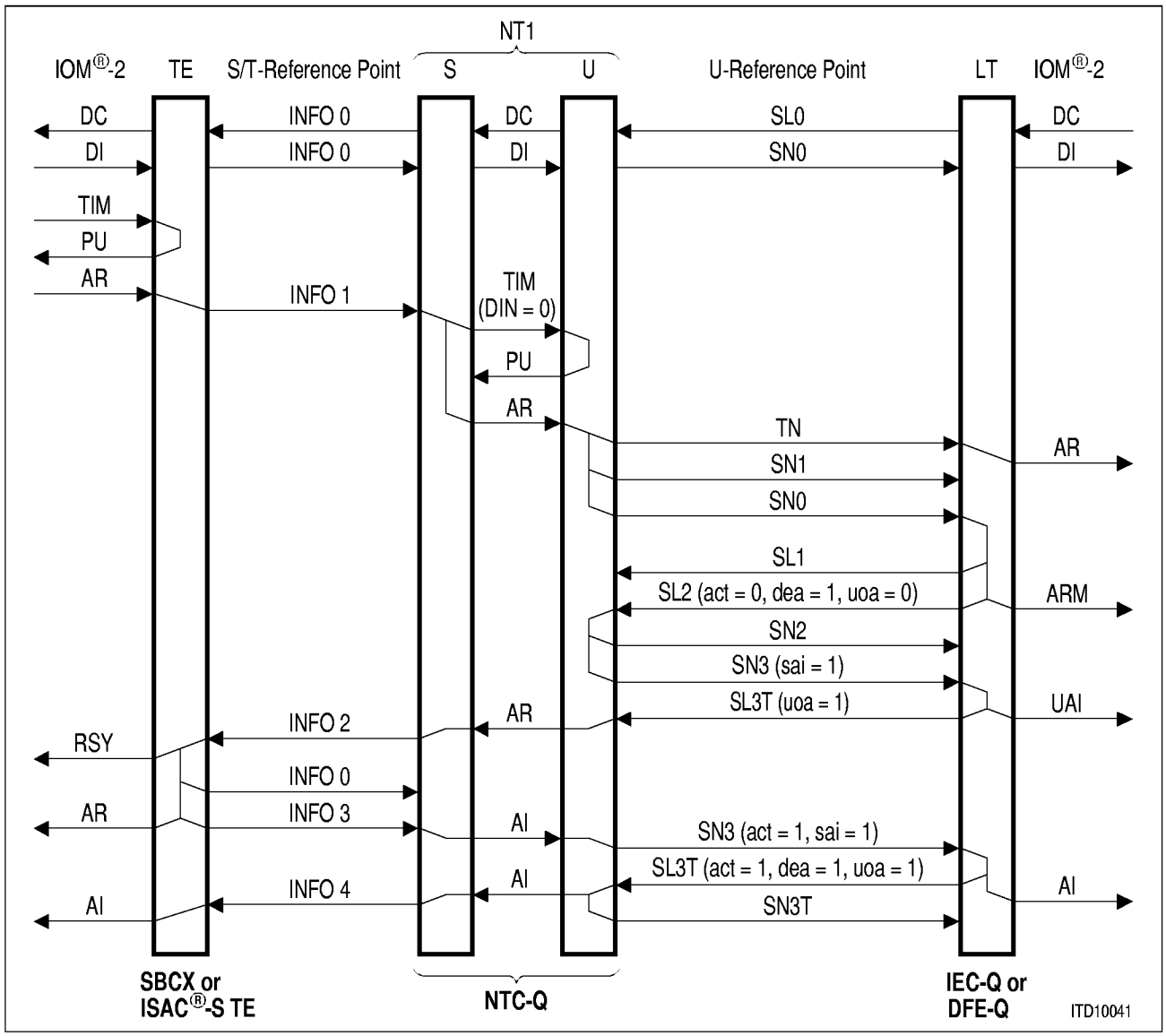


Figure 30 Complete Activation Initiated by Terminal (TE)

Complete Deactivation

Figure 31 depicts the procedure if deactivation has been initiated. Deactivation of layer 1 is always initiated by the exchange (LT)

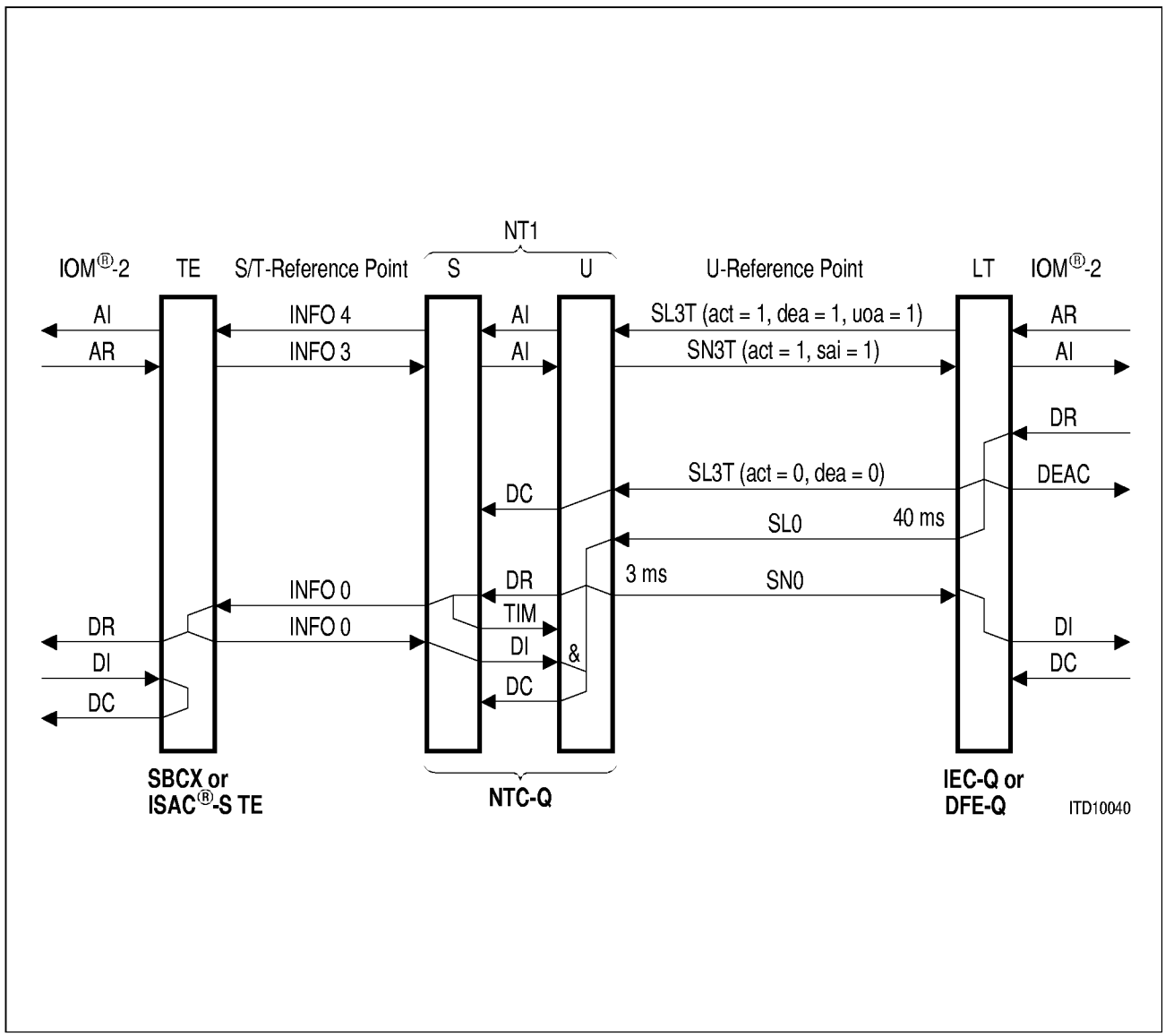


Figure 31 Complete Deactivation

Partial Activation

Figure 32 depicts the procedure if partial activation has been initiated by the exchange (LT).

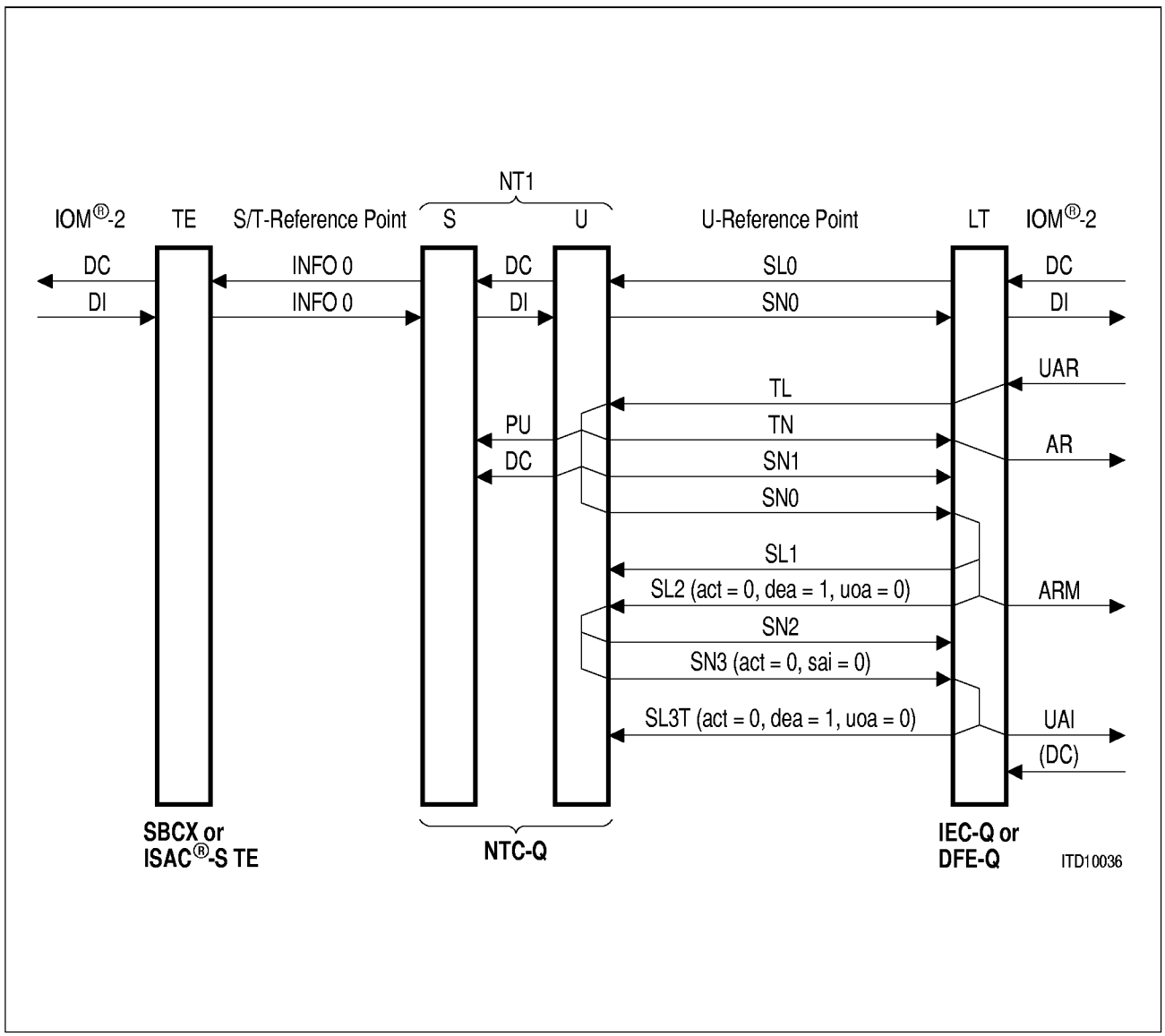


Figure 32 Partial Activation

Activation from LT with U active

Figure 33 depicts the procedure if activation has been initiated by the LT with U already being active.

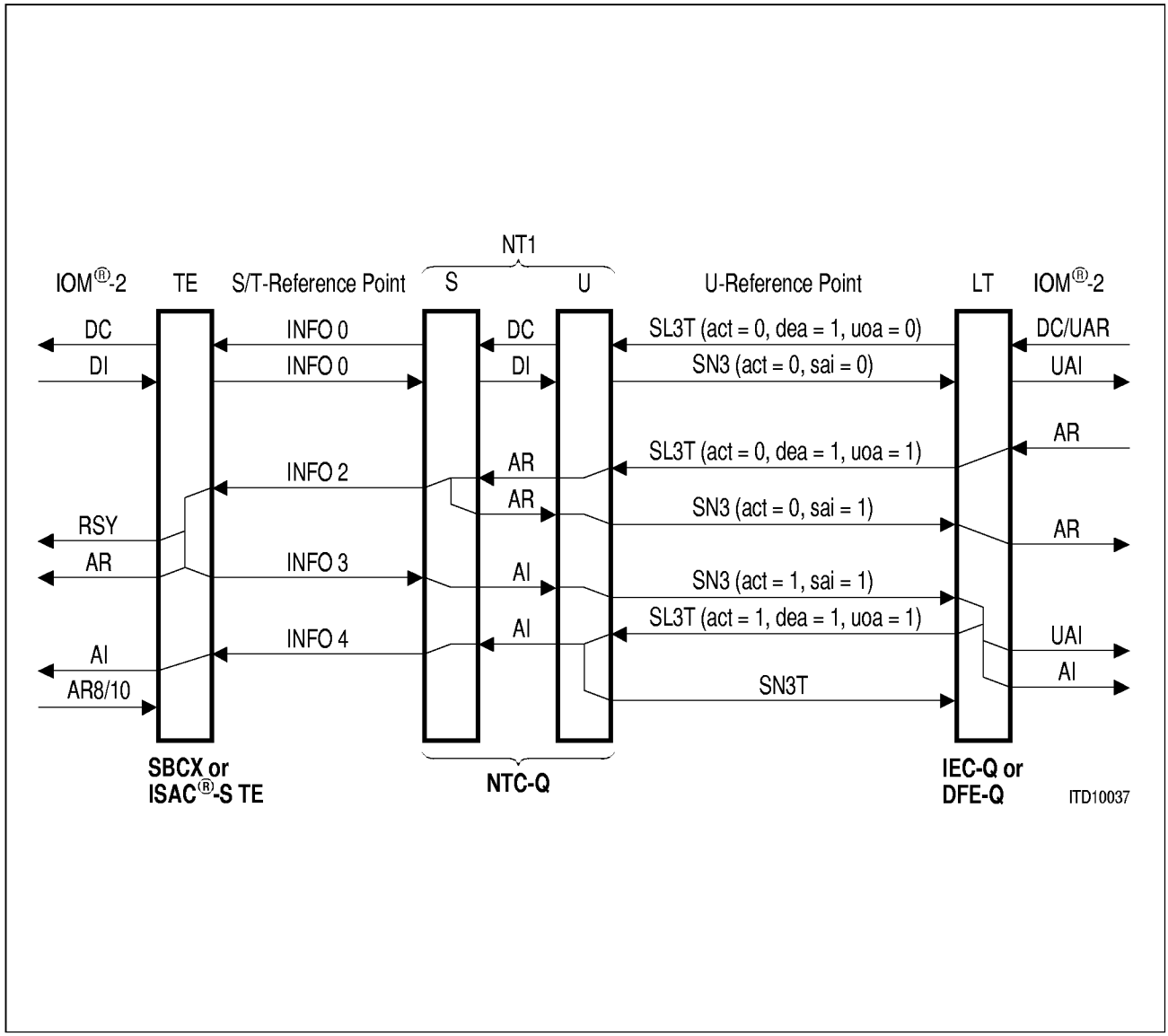


Figure 33 Activation from LT with U Active

Activation from TE with U Active

Figure 34 depicts the procedure if activation has been initiated by the TE with U already being active.

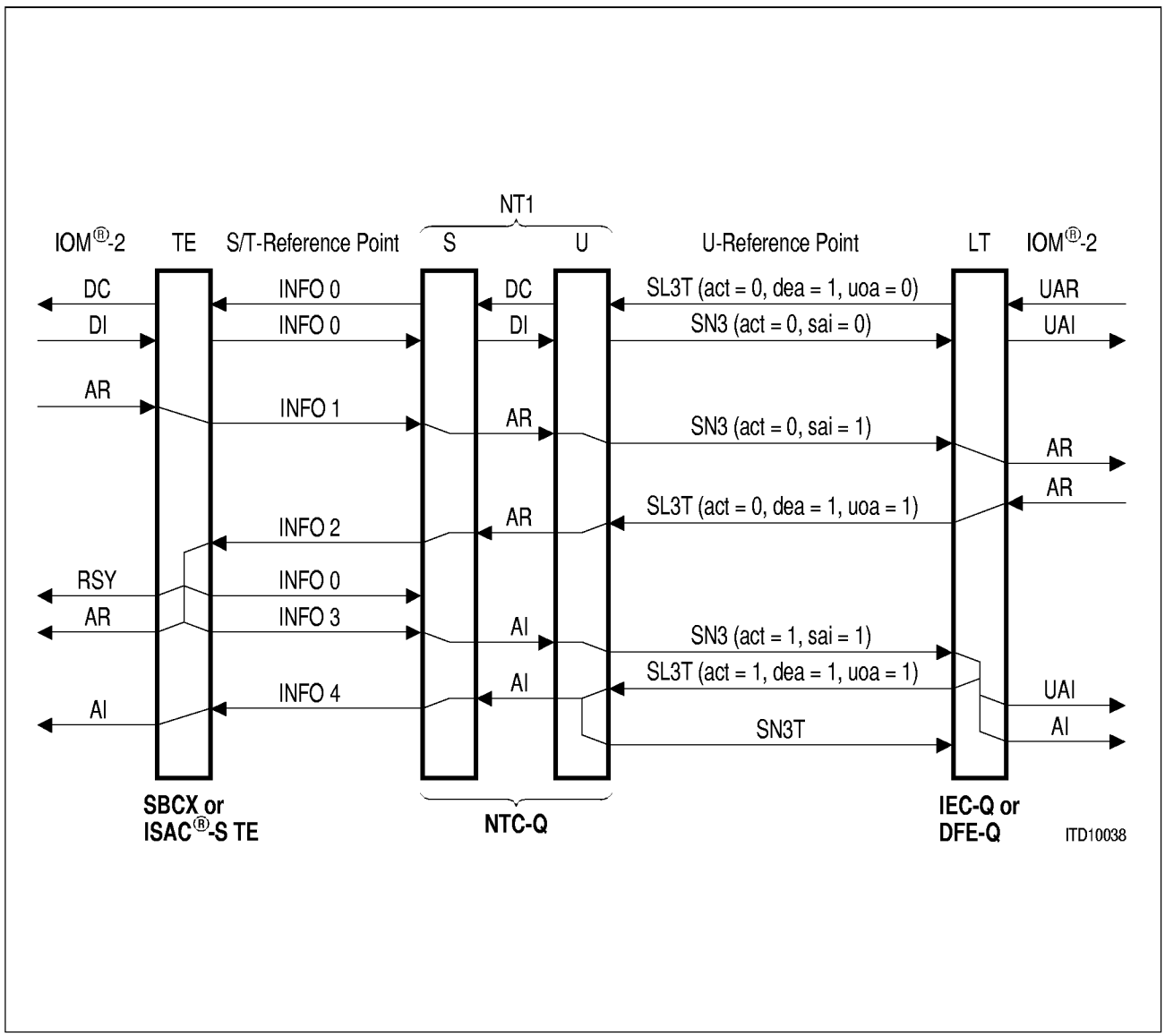


Figure 34 Activation from TE with U Active

Partial Deactivation with U Active

Figure 35 depicts the procedure if partial deactivation has been initiated, i.e. U remains active.

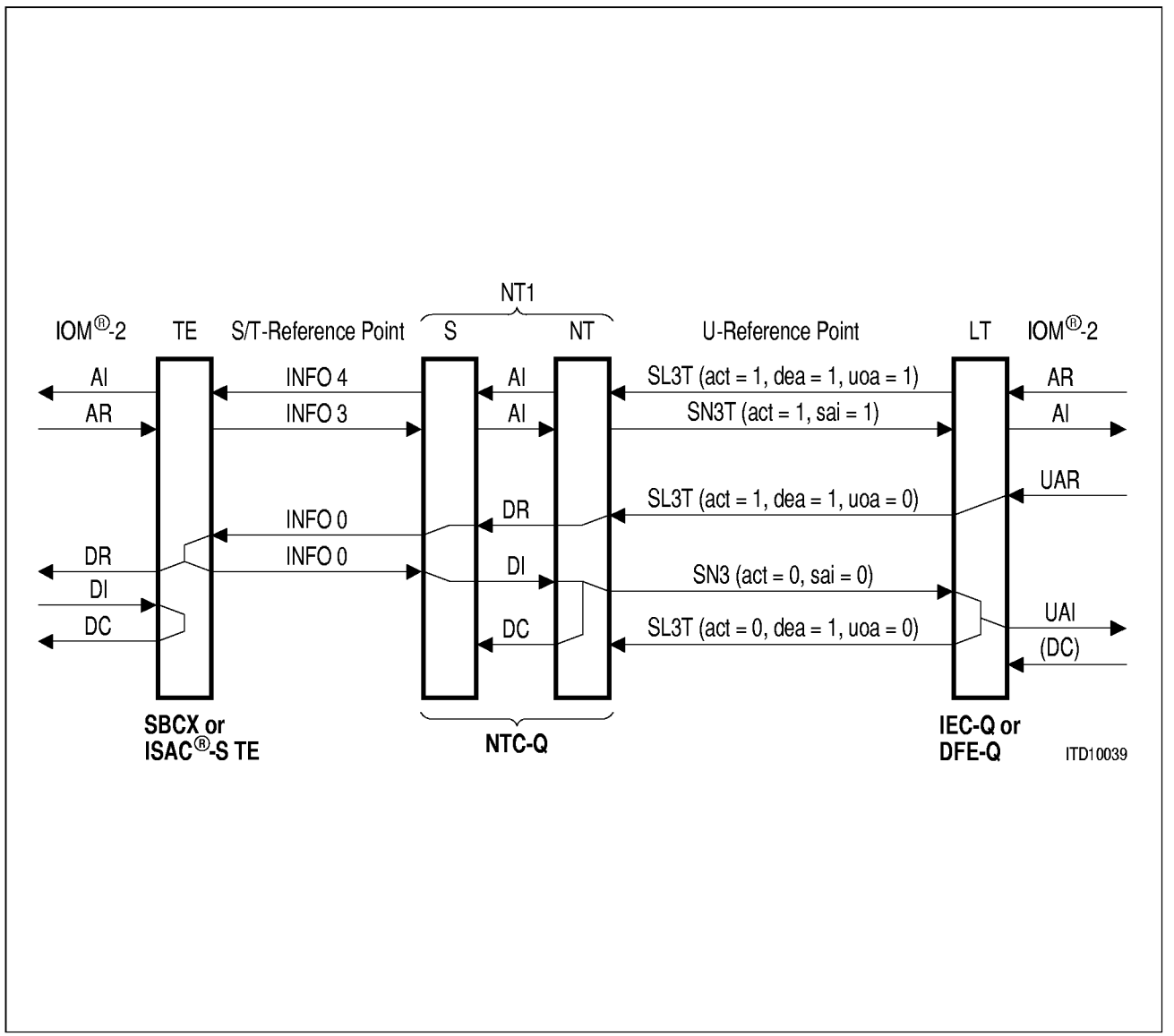


Figure 35 Partial Deactivation wit U Active

Loop 2 According to ETSI Standard

Figure 36 depicts the procedure if loop 2 is closed and opened according to ETSI ETR 080. Pin AL2 is set to '1'

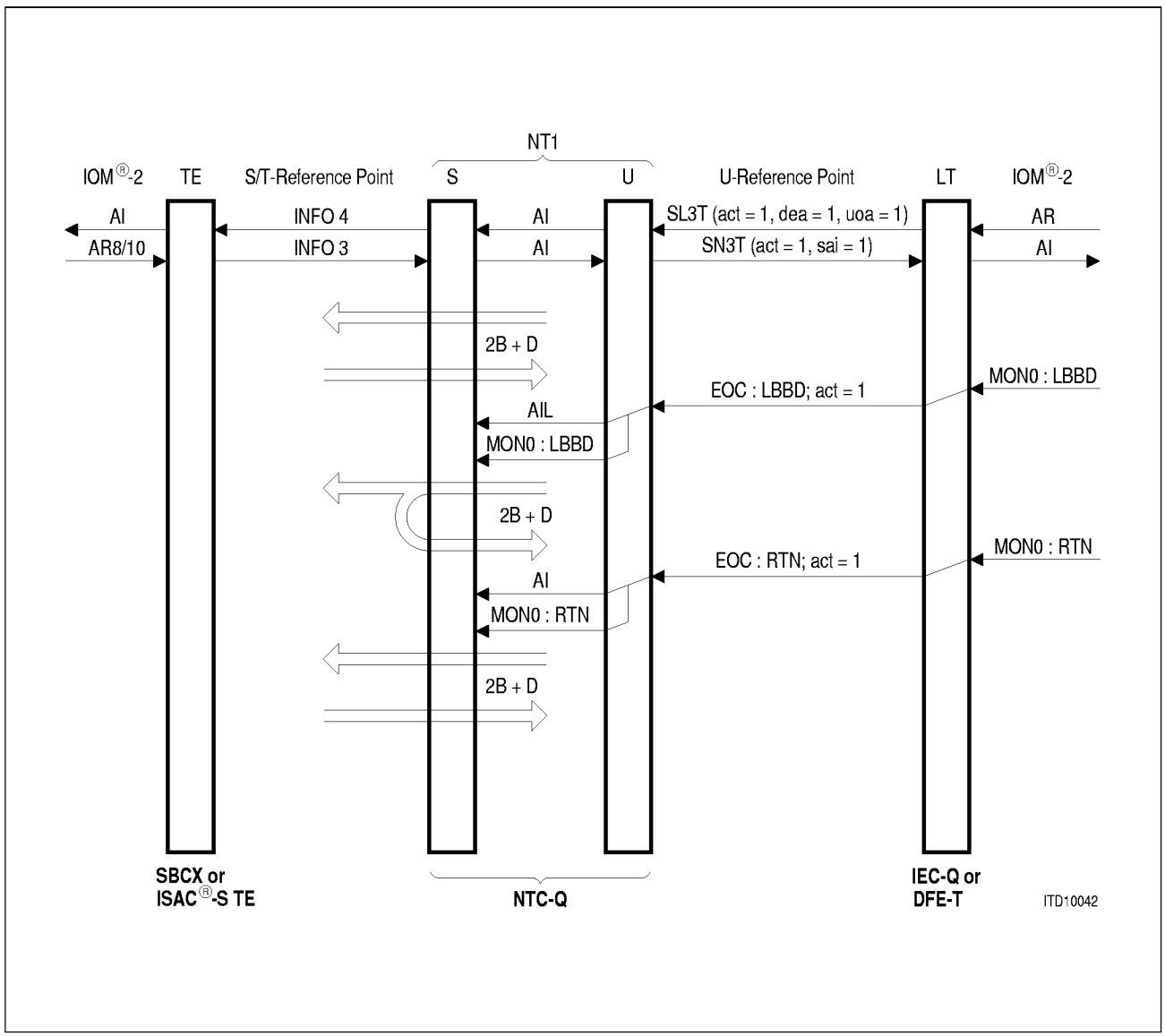


Figure 36 Loop 2 According to ETSI Standard

Loop 2 According to ANSI Standard

Figure 37 depicts the procedure if loop 2 is closed and opened according to ANSI T1.601. Pin AL2 is set to '0'.

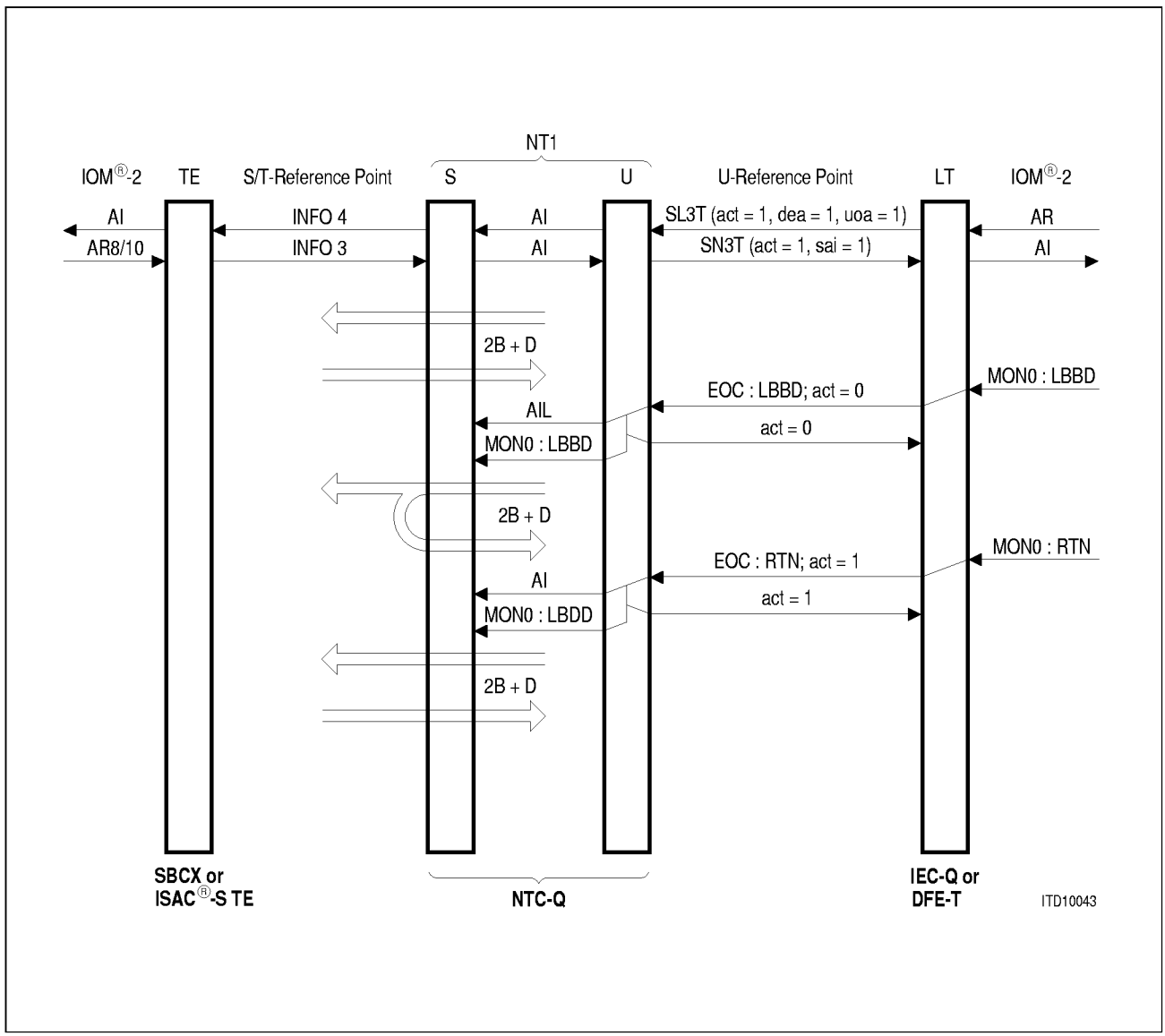


Figure 37 Loop 2 According to ANSI Standard

3.2 External Circuitry

3.2.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.

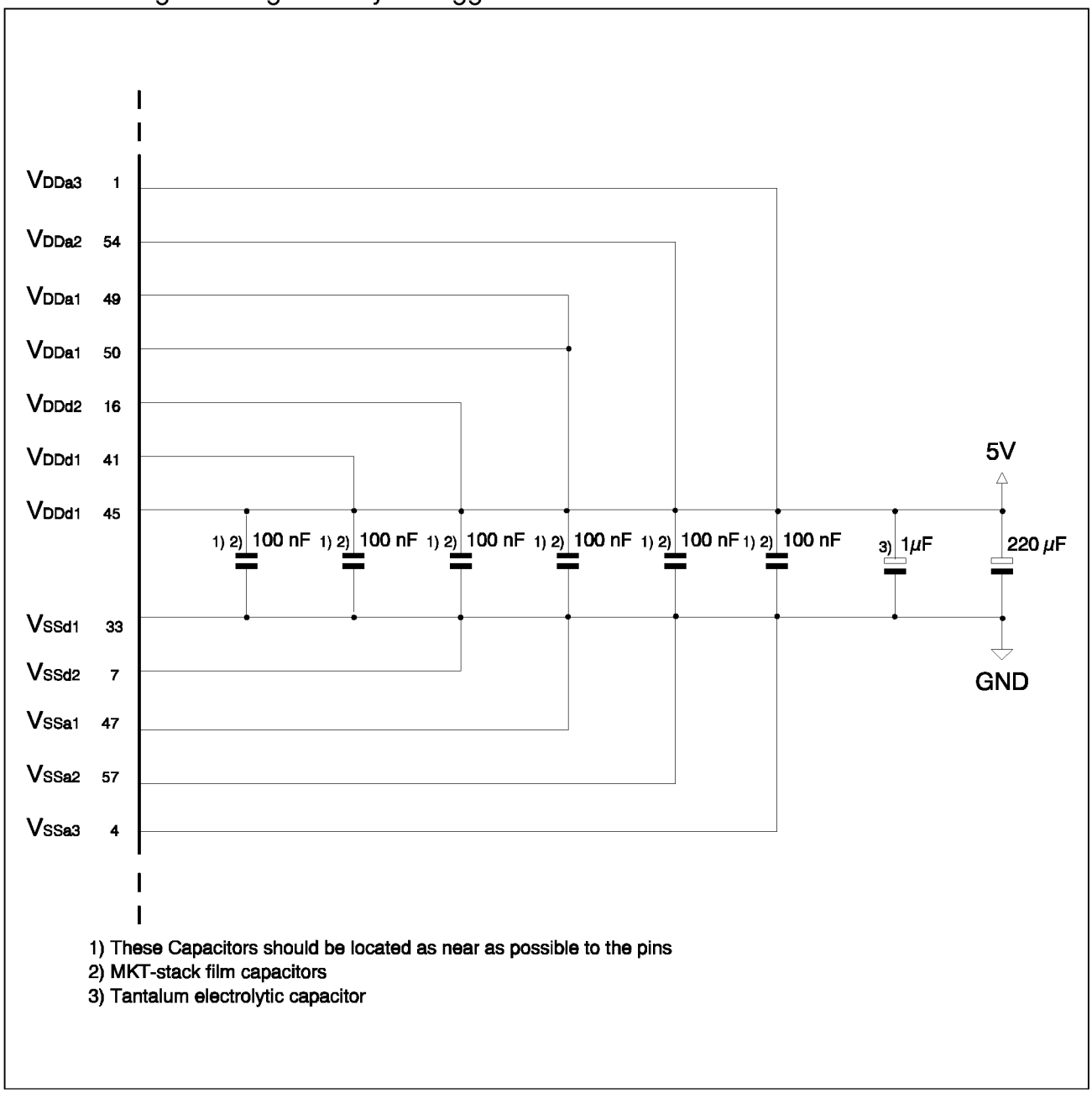


Figure 38 Power Supply Blocking

3.2.2 U-Interface

The hybrid suggested for the NTC-Q in **figure 39** is identical to the hybrid recommended for the PEB 2091 IEC-Q.

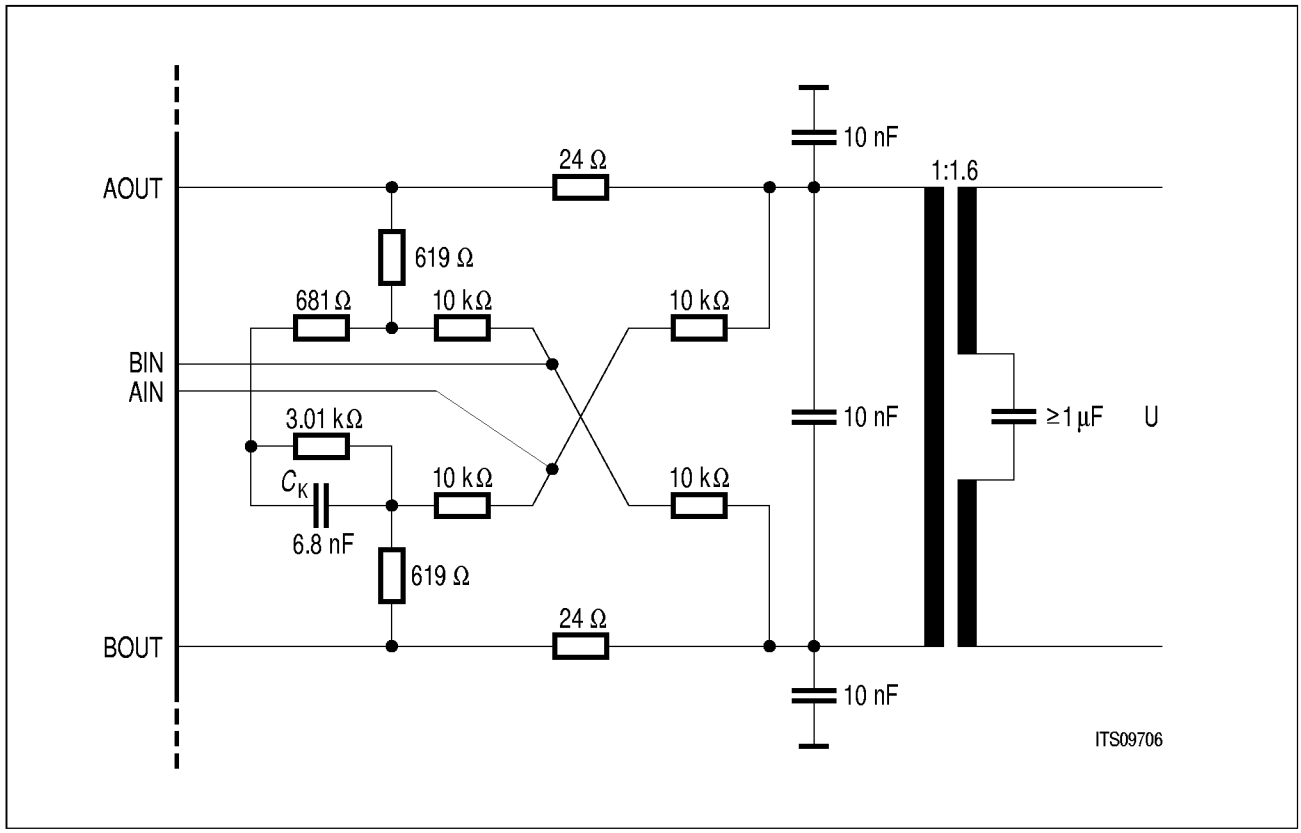


Figure 39 U-Interface Hybrid Circuit

Note: To achieve optimum performance all capacitors of the hybrid should be MKT. Ceramic capacitors are not recommended.

The recommended tolerances are:

Rs: 1%.
6.8nF: 5%
10nF: 10-20%

3.2.3 S-Interface

In order to comply to the physical requirements of ITU recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the S-transceiver needs some additional circuitry.

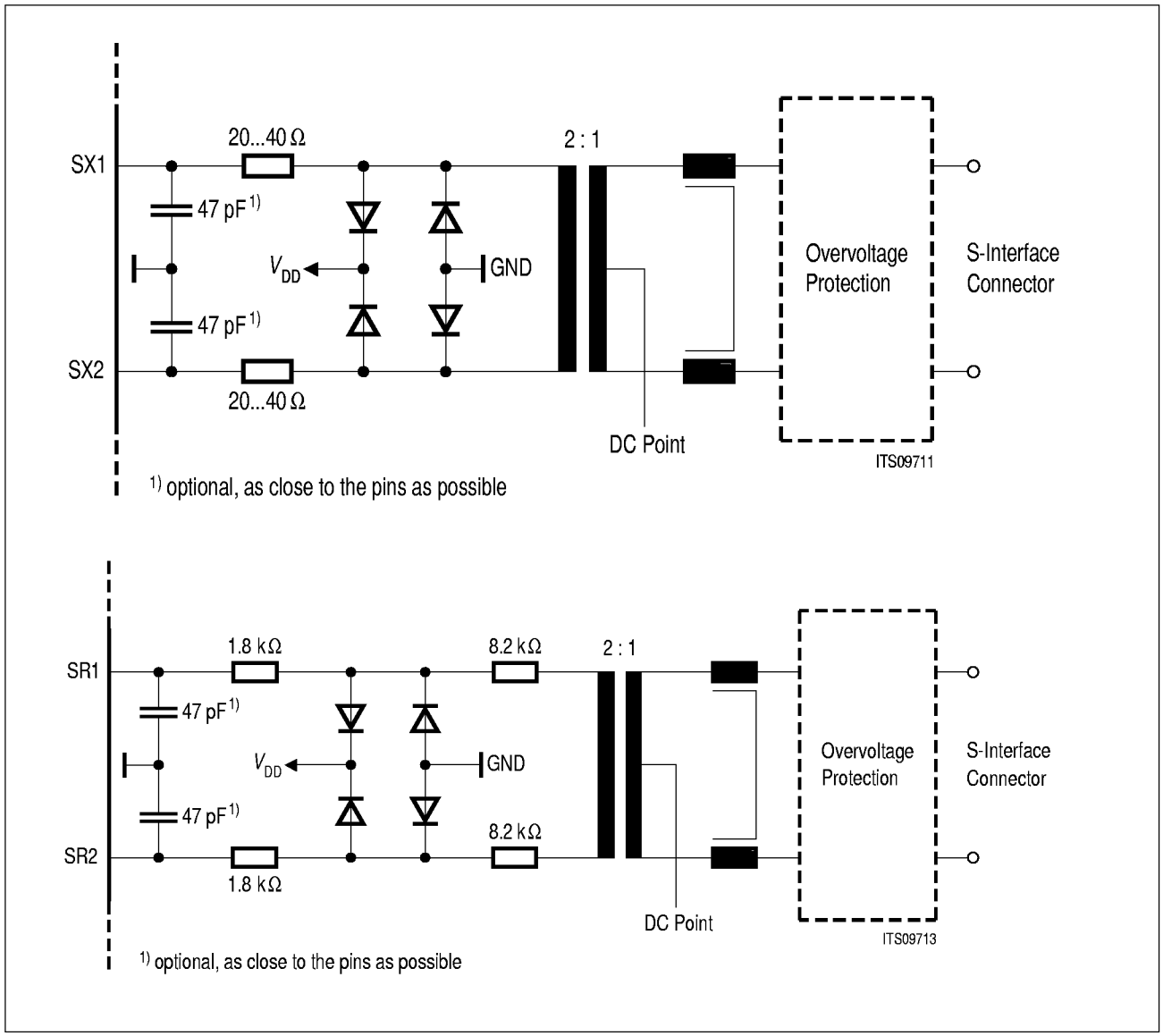


Figure 40 S-Interface External Circuitry

The transmitter requires external resistors (20 … 40 Ω) in order to adjust the output voltage to the pulse mask (nominal 750 mV according to ITU I.430, to be tested with the test mode “TM1”) on the one hand and in order to meet the output impedance of minimum 20 Ω on the other hand.

The receiver of the S-transceiver is symmetrical. 10 kΩ overall resistance are recommended in each receive path. Although it is possible to place two single 10 kΩ resistors, either between transformer and diode circuit or between chip and diode circuit,

it is preferable to split the resistance into two resistors for each line. This allows to place a high resistance between the transformer and the diode protection circuit (required to pass 96 kHz input impedance test of ITU I.430). The remaining resistance (1.8 kΩ) protects the S-transceiver itself from input current peaks.

3.2.4 Oscillator Circuit

Figure 41 illustrates the recommended oscillator circuit.

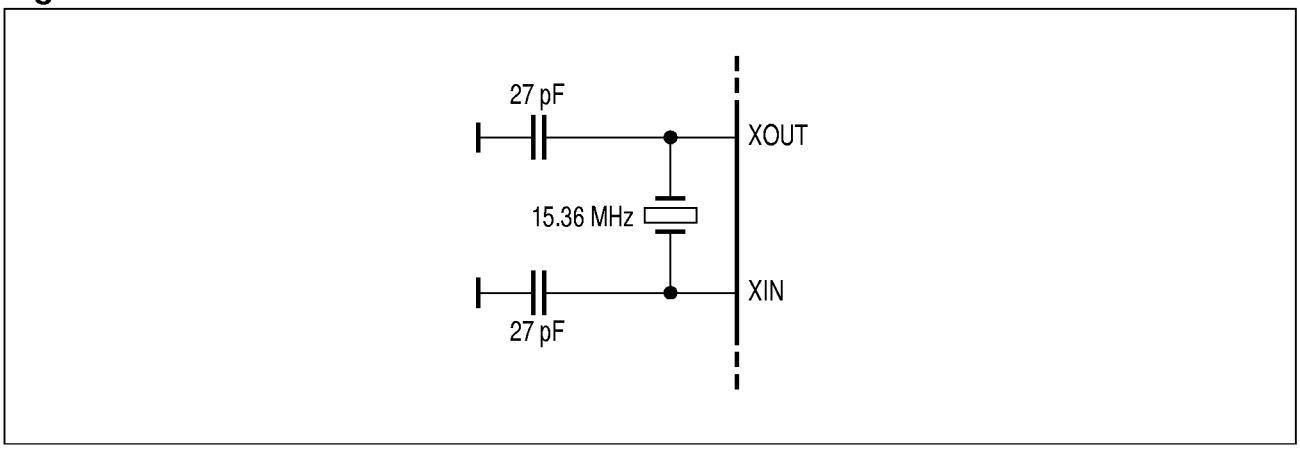


Figure 41 Crystal Oscillator

Crystal Parameters

Frequency:	15.36 MHz
Load capacitance:	20 pF +/- 0.3pF
Frequency tolerance:	60 ppm
Resonance resistance:	20 Ω
Max. shunt capacitance:	7 pF
Oszillator mode:	fundamental

Note: Typical values for the capacitances connected to the crystal are 22 ... 33 pF.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEB PEF	T_A T_A	0 to 70 – 40 to 85	°C °C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on V_{DD}	V_{DD}	6	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	1000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993. Stress tests vs. Pin 4 (VSSa3) withstand voltages ≤850 V.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse as outlined in the following figure.

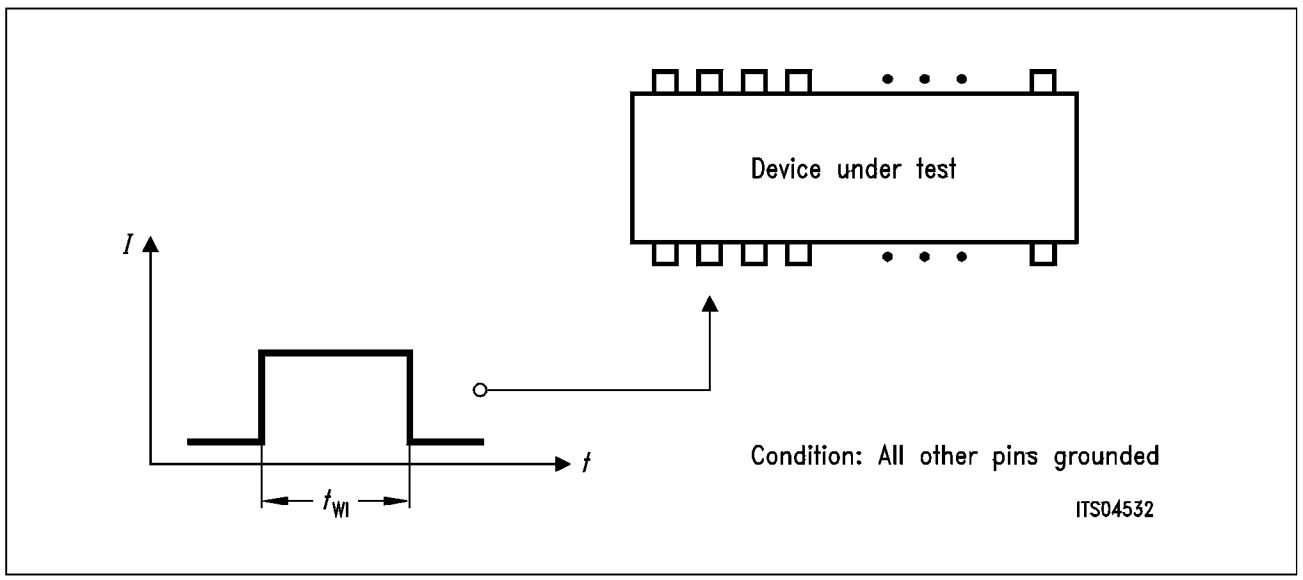


Figure 42 Test Condition for Maximum Input Current

S-Transmitter Input Current

The destruction limits for negative input signals ($R_i \geq 2\ \Omega$) and for positive input signals ($R_i \geq 200\ \Omega$) are given in **Figure 43**.

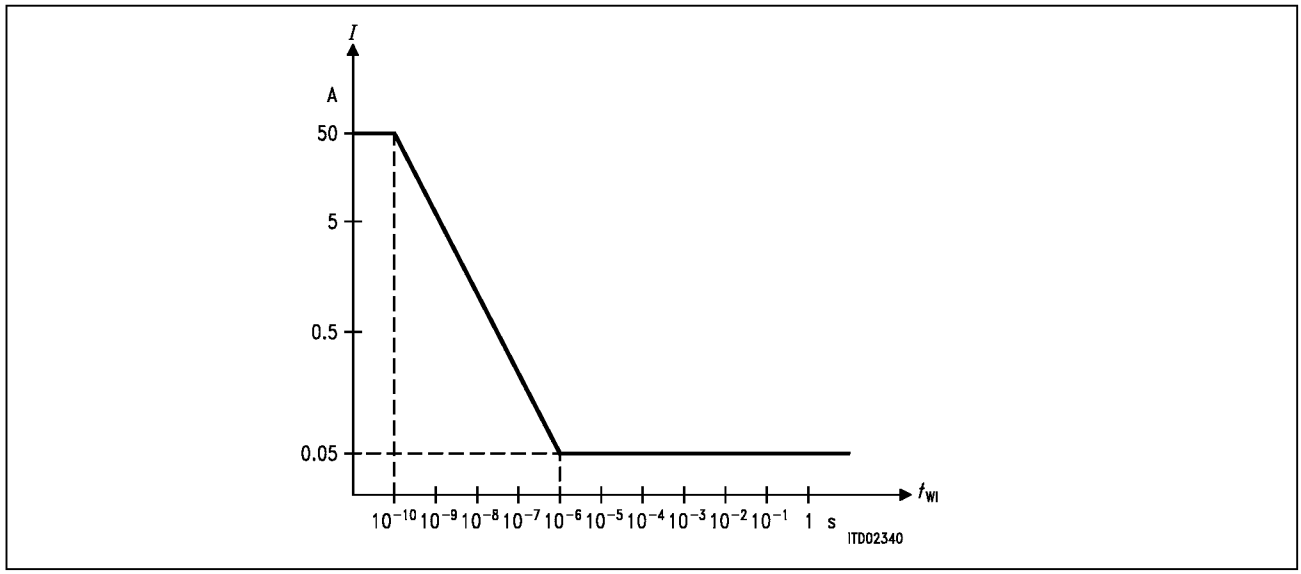


Figure 43 S-Transmitter Input Current

S-Receiver Input Current

The destruction limits ($R_i \geq 300\ \Omega$) are given in **Figure 44**.

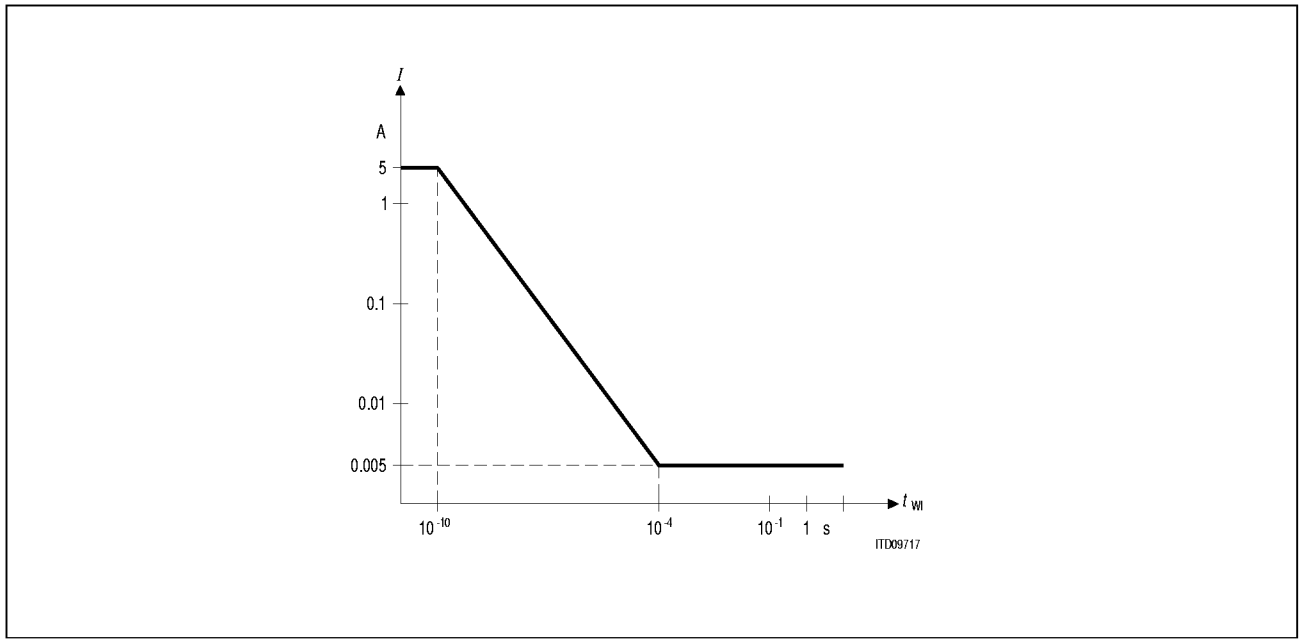


Figure 44 S-Receiver Input Current

U-Transceiver Input Current

The destruction limits for AOUT, BOUT, AIN and BIN are given in **Figure 45**.

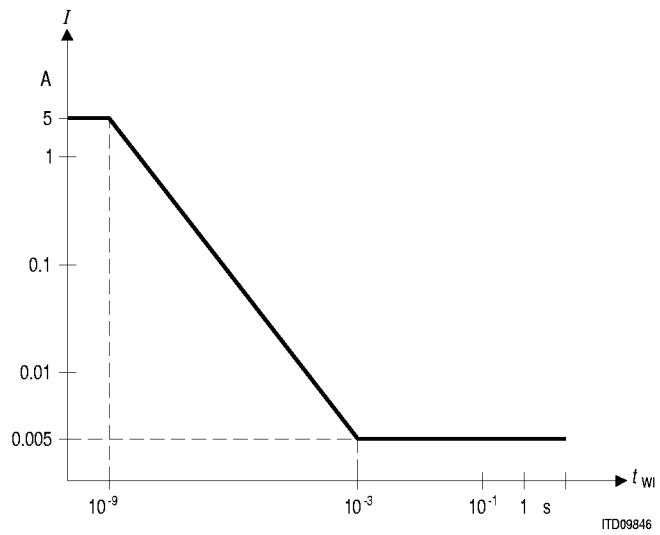


Figure 45 U-Transceiver Input Current

4.2 Power Consumption

Power Consumption

Parameter	Limit Values			Unit	Test Condition
	min.	typ.	max.		
Operational Power Down		300 28	360 50	mW mW	VDD=5V, VSS=0V. Inputs at VSS/VDD, No output loads except SX1,2 (280 Ω[1)]) and AOUT,BOUT (98 Ω[2)]), 50% bin. zeros no LED connected, IOM-2 disabled, pin MTI open

1) 280 Ω between pins SX1 and SX2 correspond to 50 Ω (2 x TR) on the S-bus.

2) 98 Ω between pins AOUT and BOUT correspond to 135 Ω line impedance of the U-interface.

*Note: Please refer to **chapter 6** on **page 95** for more information concerning the power consumption in typical applications.*

4.3 DC Characteristics

Pin	Parameter	Symbol	Limit Values		Unit	Test Condition
			min.	max.		
All except SR1, 2	Input low voltage	V_{IL}	– 0.4	0.8	V	
	Input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
All except DD, DU; SX1, SX2; A/BOUT	Output low voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
DD, DU; $\overline{ACT}$	Output low voltage	V_{OL1}		0.45	V	I_{OL} = 7 mA
All except DD, DU; SX1, 2, A/BOUT	Output high voltage	V_{OH1}	2.4		V	I_{OH1} = 400 µA
			V_{DD} – 0.5		V	I_{OH1} = 100 µA
DD, DU	Output high voltage (push-pull)	V_{OH2}	3.5		V	I_{OH2} = 6 mA
All pins except SX1, 2; SR1,2; AIN, BIN, XIN	Input leakage current	I_{LI}		1	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Output leakage current	I_{LO}		1	µA	0 V ≤ V_{OUT} ≤ V_{DD}
	Input leakage current internal pull-up	I_{LIPU}		100	µA	0 V ≤ V_{IN} ≤ V_{DD}
	Input leakage current internal pull-down	I_{LIPD}		100	µA	0 V ≤ V_{IN} ≤ V_{DD}
XIN	Input leakage current	I_L		40	µA	0 V ≤ V_{IN} ≤ V_{DD}
AIN, BIN	Input leakage current	I_L		70	µA	0 V ≤ V_{IN} ≤ V_{DD}
SX1, SX2	Absolute value of output pulse amplitude (V_{SX2} – V_{SX1})	V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω[1)] R_L = 400 Ω[1)]
SX1, SX2	S-Transmitter output current	I_X	7.5	13.4	mA	R_L = 5.6 Ω[1)]
SX1, SX2	S-Transmitter output impedance	Z_X	10 0		kΩ Ω	inactive or during binary one (V_{DD} = 0 … 5 V) during binary zero R_L = 50 Ω
SR1, SR2	S-Receiver input impedance	Z_R	10 100		kΩ Ω	V_{DD} = 5 V V_{DD} = 0 V

U-Transceiver Characteristics

	Limit Values			Unit
	min.	typ.	max.	
Receive Path				
Signal / (noise + total harmonic distortion)[1]	60	65		dB
DC-level at AD-output	45	50	55	%[4]
Threshold of level detect	4	20	28	mV
Input impedance AIN/BIN	50			kΩ
Transmit Path				
Signal / (noise + total harmonic distortion) [2]	65	70		dB
Output DC-level	2.05	2.375	2.6	dB
Offset between AOUT and BOUT			35.5	mV
Signal amplitude [3]	3.10	3.20	3.30	V
Output impedance AOUT/BOUT: Power-up Power-down		 2 6	 4 12	 Ω Ω

Note:
1) Test conditions: 1.3 Vpp antisemetric sine wave as input on AIN/BIN with long range (low, critical range).
2) Interpretation and test conditions: The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 65 dB below the signal for an evenly distributed but otherwise random sequence of + 3, + 1, – 1, – 3.
3) The signal amplitude measured over a period of 1 min. varies less than 1%.
4) The percentage of the "1"-values in the PDM-signal.

Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; f_C = 1 MHz

Pin	Parameter	Symbol	Limit Values		Unit
			min.	max.	
All pins except SX1,2, XIN, XOUT	Pin capacitance	C_{IO}		7	pF
SX1,2	Output capacitance against V_{SS}	C_{OUT}		10	pF
XIN, XOUT	Pin capacitance	C_{IO}		5	pF

Supply voltages

$VDD_D1\text{-}2 = +5\ V \pm 0.25\ V$
$VDD_A1\text{-}3 = +5\ V \pm 0.25\ V$

The maximum sinusoidal ripple on $VDD_A1\text{-}3$ is specified in the following figure:

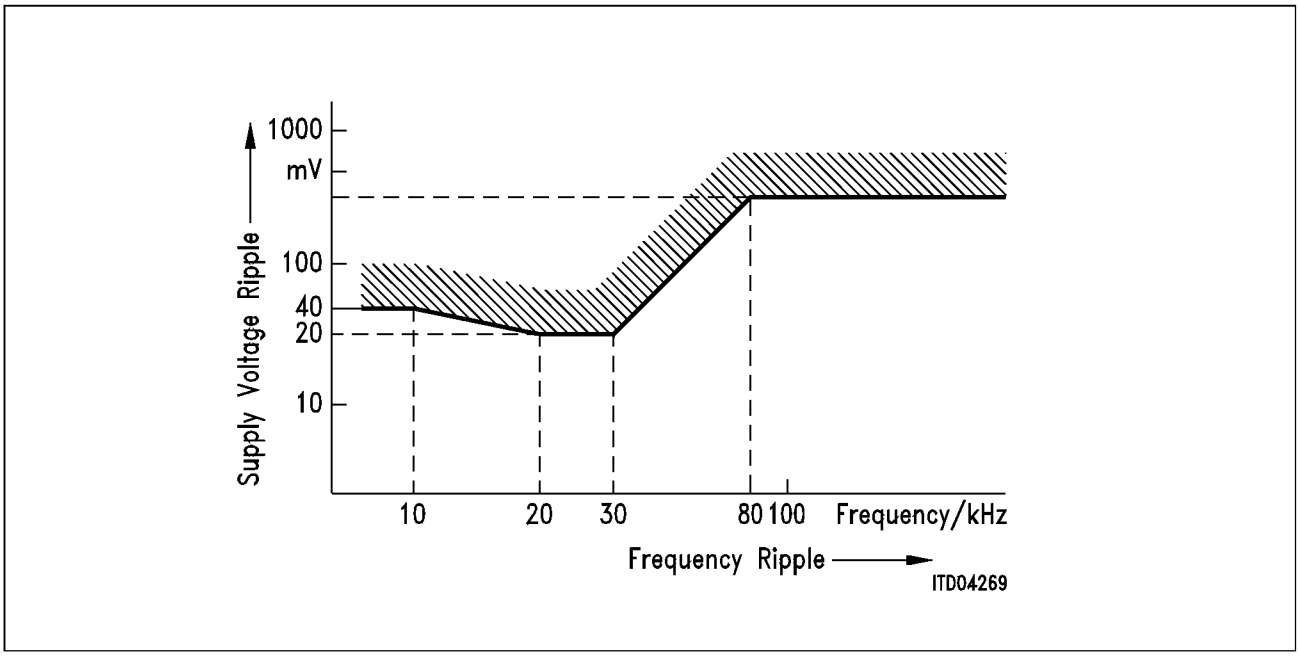


Figure 46 Maximum Sinusoidal Ripple on Supply Voltage

4.4 AC Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **figure 47.**

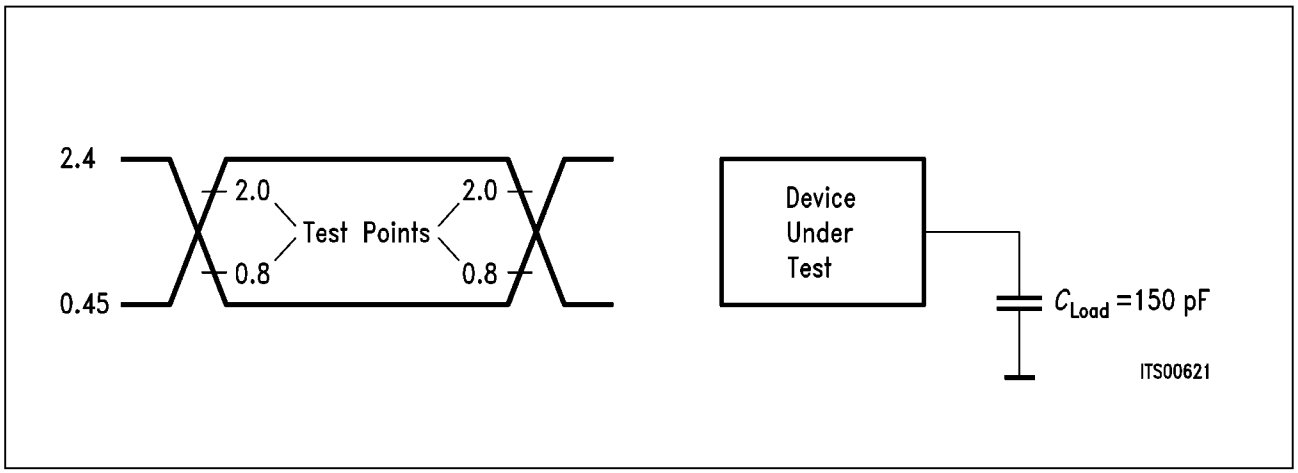


Figure 47 Input/Output Waveform for AC Tests

IOM®-2 Interface Timing

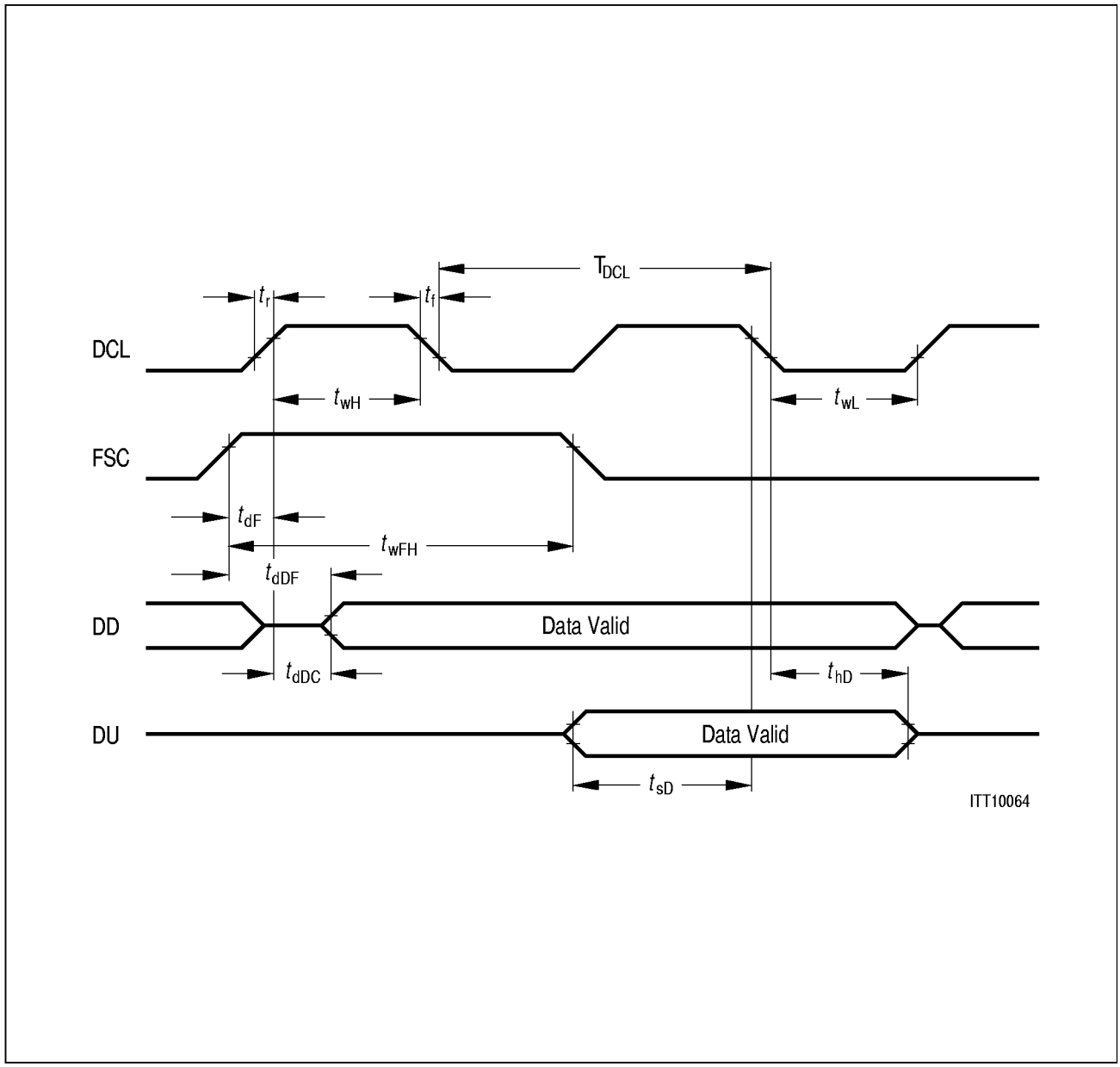


Figure 48 IOM®-2 Timing

Table 13 IOM®-2

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Data clock rise/fall	DCL	t_R, t_F			30	ns	C_L = 25 pF
Clock period [1]		T_{DCL}	1875	1953	2035	ns	C_L = 25 pF
Pulse width [1] high/low		t_{wH} t_{wL}	850	960	1105	ns	
Clock period [2]		T_{DCL}	565	651	735	ns	C_L = 25 pF
Pulse width [2] high/low		t_{wH} t_{wL}	200	310	420	ns	
Frame width high	FSC	t_{wFH}		$2 \times T_{DCL}$			C_L = 25 pF
Frame synch. rise/ fall		t_R, t_F			30	ns	C_L = 25 pF
Frame advance		t_{dF}	0	65	130	ns	C_L = 25 pF
Data out	DD	t_F			200	ns	C_L = 150 pF (R = 1 kΩ to V_{DD}, open drain)
Data out		t_R, t_F			150	ns	C_L = 150 pF (tristate)
Data delay clock [3]		t_{dDC}			100	ns	C_L = 150 pF
Data delay frame [3]		t_{dDF}			150	ns	C_L = 150 pF
Data sample delay	DU	t_{sD}	t_{wH} + 20			ns	
Data hold		t_{hD}	50			ns	

Notes:

[1] 256 kbit/s (DCL = 512 kHz)

[2] 768 kbit/s (DCL = 1.523 MHz)

[3] The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference.

Reset Timing

Table 14 Reset Timing Characteristics

Parameter	Symbol	Limit Values	Unit	Test Conditions
		min.		
Power-on Reset Active low state	t_{RST}	67	ms	
Reset at pin $\overline{RES}$ Active low state	t_{RST}	4 DCL periods		

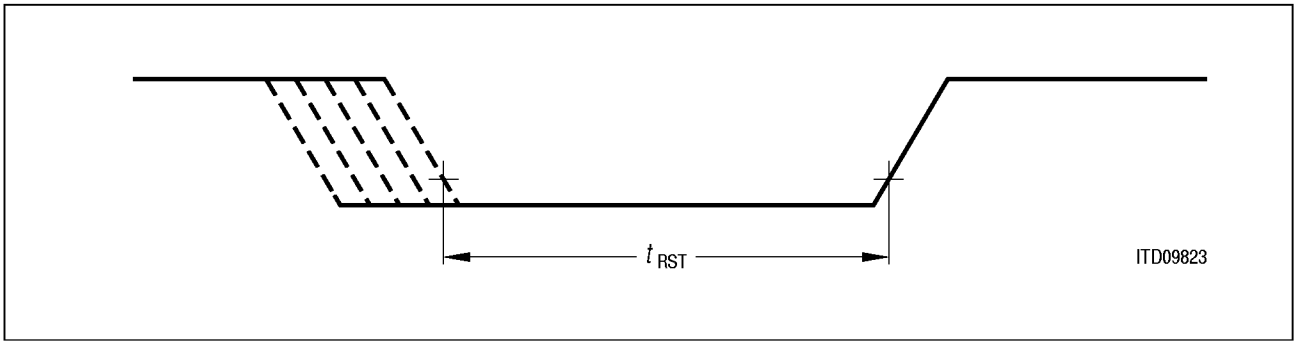
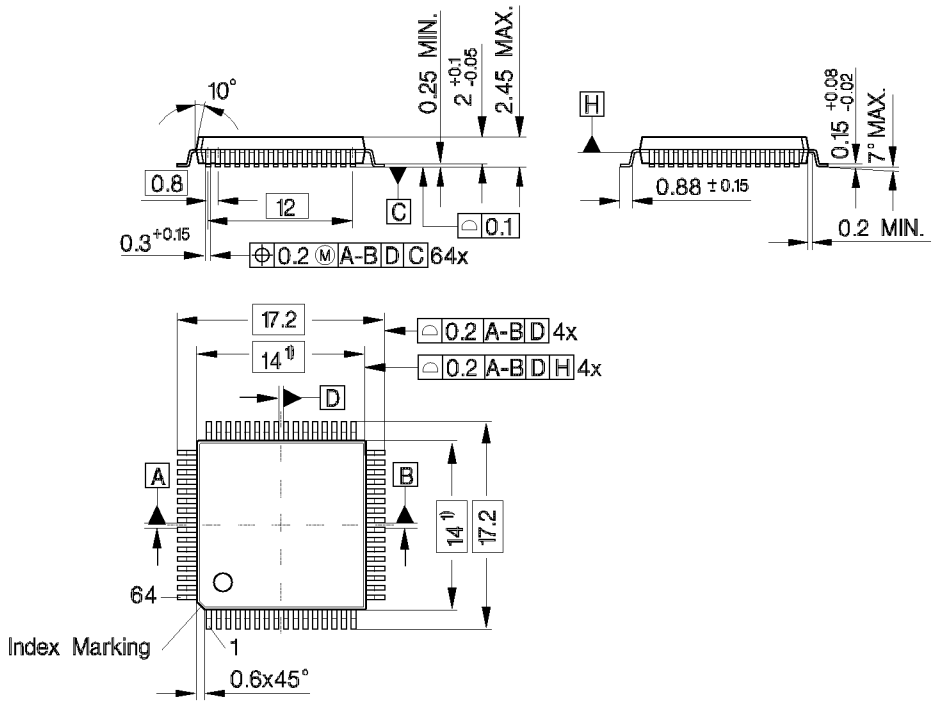


Figure 49 Reset Timing

5 Package Outlines

Plastic Package, P-MQFP-64
(Metric Quad Flat Package)

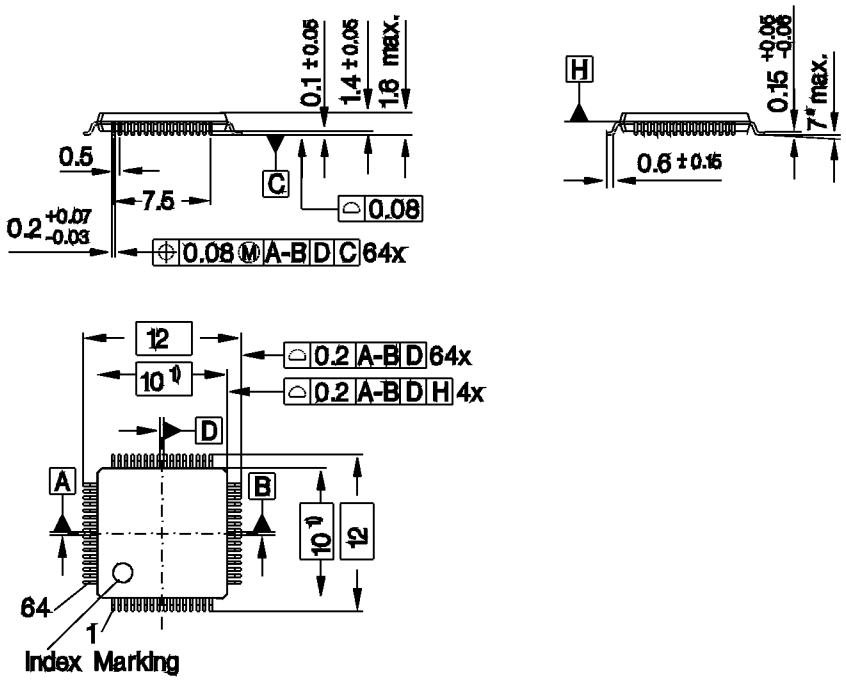


1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-TQFP-64
(Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.
SMD = Surface Mounted Device

Dimensions in mm

6 Power Consumption in the Application

Table 15 shows the typical power consumption of the NTC-Q in an NT1 application. It can be seen how different test conditions such as the loop length of the U-line and the data pattern influence the power consumption of the device.

The lab measurements were done with specific, arbitrarily selected devices on the NT1 Evaluation Board SIPB81910. All measurements were performed at room temperature.

Table 15 Power Consumption in a Typical Application

U-Loop	Load on S/T Interface	Data Pattern	V_{DD}	IOM-interface enabled	Power Consumption in mW
15kft[1)]	50 Ω	50% Zeros	5.0V	no	285
ANSI Loop 0[2)]	50 Ω	50% Zeros	5.0V	no	325
ANSI Loop 1[3)]	50 Ω	50% Zero	5.0V	no	291
135 Ω	50 Ω	100% Zeros	5.0V	no	310
15kft	50 Ω	**100 % Ones**	5.0V	no	278
15kft	50 Ω	**100 % Zeros**	5.0V	no	294
15kft	50 Ω	50% Zeros	**4.75V**	no	276
15kft	50 Ω	50% Zeros	**5.25V**	no	297
15kft	50 Ω	50% Zeros	5.0V	**yes[4)]**	287

1) 15kft of 26AWG) cable are approximately 4.5km on 0.4mm cable

2) 0kft cable

3) 16.5kft 26AWG cable plus 1.5kft 24AWG cable. Equals approximately 5.4km cable

4) No output load

7 External Component Sourcing

The following tables contain transformers and crystals recommended by different manufacturers for use with Siemens ICs. No manufacturer can be recommended over another.

Until date of print transformers marked with *) have been tested at Siemens Semiconductors and have shown positive test results.

This list is not complete. It contains a few examples of devices offered by different manufacturers. Most manufacturers offer a variety of components with different parameters. For latest information please contact the manufacturers directly or visit their web pages where available.

Note: There may also exist other manufacturers than those included in the list.

Table 16 U-Transformer Information

Part Number	Comments	Contacts (Phone)	Fax
APC			www.apcisdn.com
APC42954	2kV, RM8, PTH	EU: +44 1634 2905-88 SEA: +852 2410-2731 US: (201) 368 17-50	-91 -2518 -04
APC42963S	2kV, RM6, SMD		
APC13112	incl. hybrid and MLT		
PulseEngineering			www.pulse.com
T4002	2kV, SMD	EU: +44 14834-28877 SEA: +886 78-213141 US: (619) 674 8100	-16011 -419707 -8262
PE-68669	3kV, reinforced		
PE-68670	3kV, Low bit error rate		
S+MComponents			www.siemens.de/pr
V409	2kV, RM6, SMD	EU: +49 89 6362 4265 SEA: +65 744-7768 US: (908)-906 4300	 -6992 -632 2830
V832	2kV, RM8, PTH		
W144	4kV, RM8, PTH		
SchottCorporation			
		US: (615)-889-8800	

Table 16 U-Transformer Information (cont'd)

Part Number	Comments	Contacts (Phone)	Fax
Vacuumschmelze			www.vaccorp.com
T60403 -M6290-X054 *)	2kV	EU: +49 6181 382673 SEA: +65 8404 880 US: (405) 943 9651	
-M6290-X058 *)	2kV/4kV; Low bit error rate		
-M6276-X...	2kV; SMD		
TDK			
		EU: +49 2192 487-0	
Valor			www.valorinc.com
		EU: +44 1727-8248-75 SEA: +852 2 953-1000 US: (619) 537-2500	-98 -1333 -2525
Vogt			www.vogt-electronic.com
544 03 006 00	2kV, PTH	EU: +49 8591 17-0 SEA: +86 21 6251-2227 US: (914) 921-6900	-240 -4489 -6381

Table 17 S-Transformer Information

Part Number	Comments	Contacts (Phone)	Fax
APC			www.apcisdn.com
APC2040 S		see table 16	
APC1020 S			
APC9018 D			
PulseEngineering			www.pulse.com
PE-68975*)	2kV	see table 16	
PE-64995	3kV		
PE-65795	3kV, Low bit error rate		
S+MComponents			www.siemens.de/pr
V373	1.5kV, RM5, SMD	see table 16	
V475	0.5kV, RM5, PTH		
V568	2.0kV, R10, SMD		
SchottCorporation			
		see table 16	
Vacuumschmelze			www.vaccorp.com
T60403 -L4025-X021*)		see table 16	
-L4097-X011*)			
-L5051-X006*)			
TDK			
		see table 16	
Valor			www.valorinc.com
PT 5001		see table 16	
PT 5069			
ST 5069			

Table 17 S-Transformer Information (cont'd)

Part Number	Comments	Contacts (Phone)	Fax
Vogt			www.vogt-electronic.com
543 21 002 00*)		see table 16	
543 21 004 00*)			
543 20 006 00	2kV		

Table 18 Crystal Information

Part Number	Comments	Contacts (Phone)	Fax
FrischerElectronic			
		EU: +49 9131-33007	
KVG			
		EU: +49 7263 648-0	
NDK			
		J: (03)-460-2111 US: (408) 255-0831	
Saronix			
		US: (415) 856-6900	
Tele Quarz			
		EU: +49 7268 8010	

8 Differences between NTC-Q and IEC-Q NTE / SBCX

The NTC-Q incorporates the devices PSB 21910 (IEC-Q NTE) and PEB 2081 (SBCX). **Table 19** shows the major differences between these devices and the NTC-Q. If you are already familiar with the IEC-Q NTE and SBCX this table may help you to quickly get an understanding of the NTC-Q.

Table 19 New Functions in NTC-Q

Feature	refer to page
Additional Control Pins (CSO, AL2, SRA)	14
Metalic Loop Termination	52
Activation Status LED	65
New Test Mode arrangement	66

9 Glossary

A/D	Analog-to digital
ADC	Analog-to digital converter
AGC	Automatic gain control
AIN	Differential U-interface input
ANSI	American National Standardization Institute
ARCOFI	Audio ringing codec filter
AOUT	Differential U-interface output
B	64-kbit/s voice and data transmission channel
BCL	Bit clock
BIN	Differential U-interface input
BOUT	Differential U-interface output
C/I	Command/Indicate (channel)
CCITT	Comité Consultatif International des Téléphones et Télégraph
CCRC	Corrupted CRC
CRC	Cyclic redundancy check
D	16-kbit/s data and control transmission channel
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DCL	Data clock
DD	Data downstream
DT	Data through test mode
DU	Data upstream
EC	Echo canceller
EOC	Embedded operations channel
EOM	End of message
ETSI	European Telephone Standards Institute
FEBE	Far-end block error
FIFO	First-in first-out (memory)
FSC	Frame synchronizing clock
GND	Ground
HDLC	High-level data link control
ICC	ISDN-communications controller
IEC-Q	ISDN-echo cancellation circuit conforming to 2B1Q-transmission code
IOM-2	ISDN-oriented modular 2nd generation
INFO	U- and S-interface signal as specified by ANSI/ETSI
ISDN	Integrated services digital network
ISW	Inverted synchronization word
LB	Loop back
LBBD	Loop-back of B- and D-channels
LSB	Least significant bit
LT	Line termination

MON	Monitor channel command
MSB	Most significant bit
MR	Monitor read bit
MTO	Monitor procedure timeout
MX	Monitor transmit bit
NCC	Notify of corrupt CRC
NEBE	Near-end block error
NT	Network termination
OSI	Open systems interconnection
PLL	Phase locked loop
PS	Power supply status bit
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up
RCC	Request corrupt CRC
RCI	Read Power Controller Interface
RMS	Root mean square
RP	Repeater
S/T	Two-wire pair interface
SBCX	S/T-bus interface circuit extended
SICOFI	Signal processing codec filter
SLIC	Subscriber line interface circuit
SSP	Send single pulses (test mode)
ST	Self test
SW	Synchronization word
TE	Terminal equipment
TL	Wake-up tone, LT side
TN	Wake-up tone, NT side
TP	Test pin
U	Single wire pair interface
UTC	Unable to comply
2B1Q	Transmission code requiring 80-kHz bandwidth

10 Quick Reference Guide

This chapter contains tables and figures often required when working with the PEB 8091. For additional technical information please refer to the text.

U-Transceiver NT Mode State Diagram

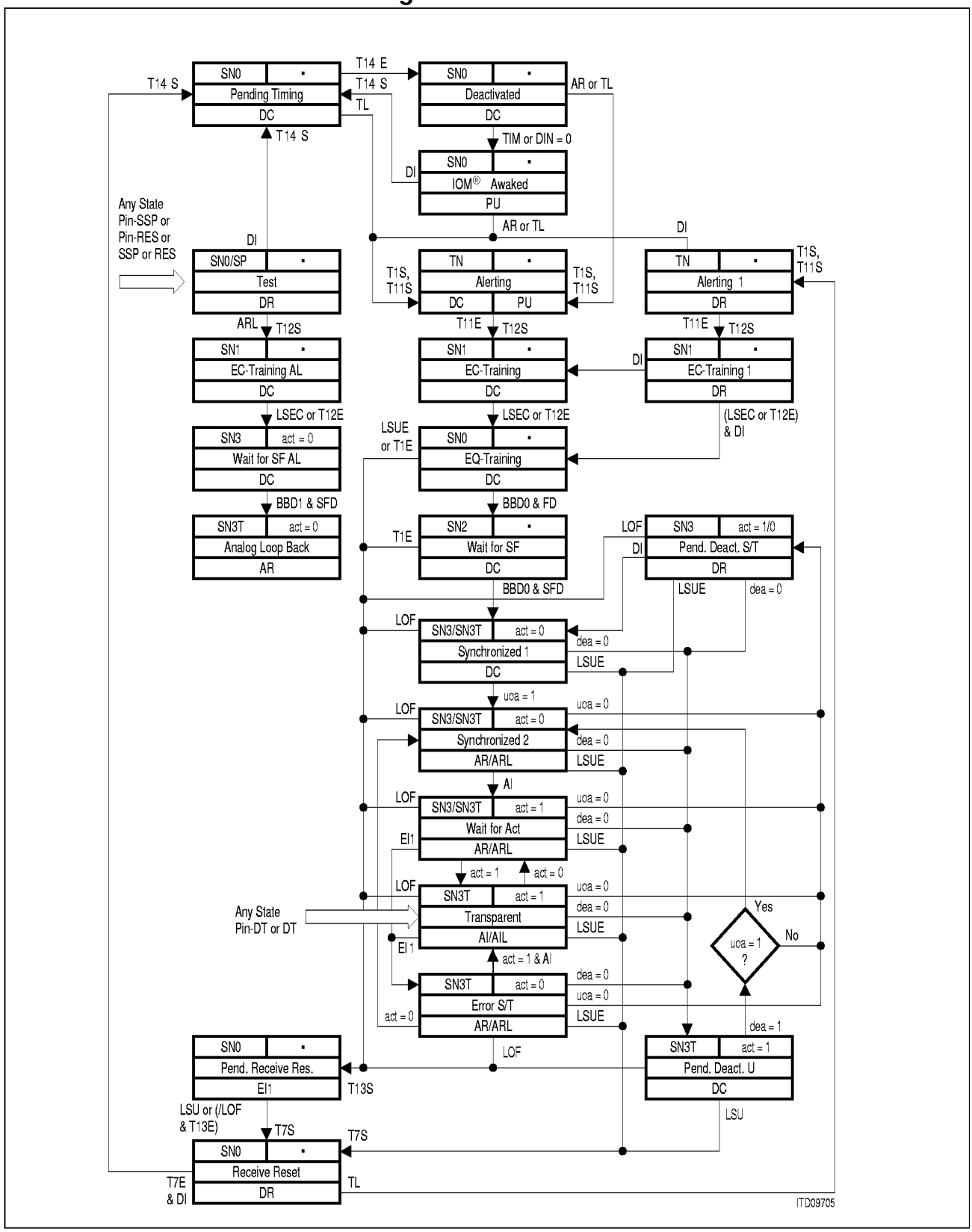


Figure 50 U-Transceiver State Diagram

Table 20 U-Transceiver C/I Codes

Code	NT-Mode	
	IN	OUT
0000	TIM	DR
0001	RES	–
0010	–	–
0011	–	–
0100	EI1	EI1
0101	SSP	–
0110	DT	MLT
0111	–	PU
1000	AR	AR
1001	–	–
1010	ARL	ARL
1011	–	–
1100	AI	AI
1101	–	–
1110	–	AIL
1111	DI	DC

AI	Activation Indication	EI1	Error Indication 1
AR	Activation Request	MLT	Metallic Loop Termination
ARL	Activation Request Local Loop	PU	Power-Up
DC	Deactivation Confirmation	RES	Reset
DI	Deactivation Indication	SSP	Send-Single-Pulses test mode
DR	Deactivation Request	TIM	Timing request
DT	Data-Through test mode		

S-Transceiver State Machine NT Mode

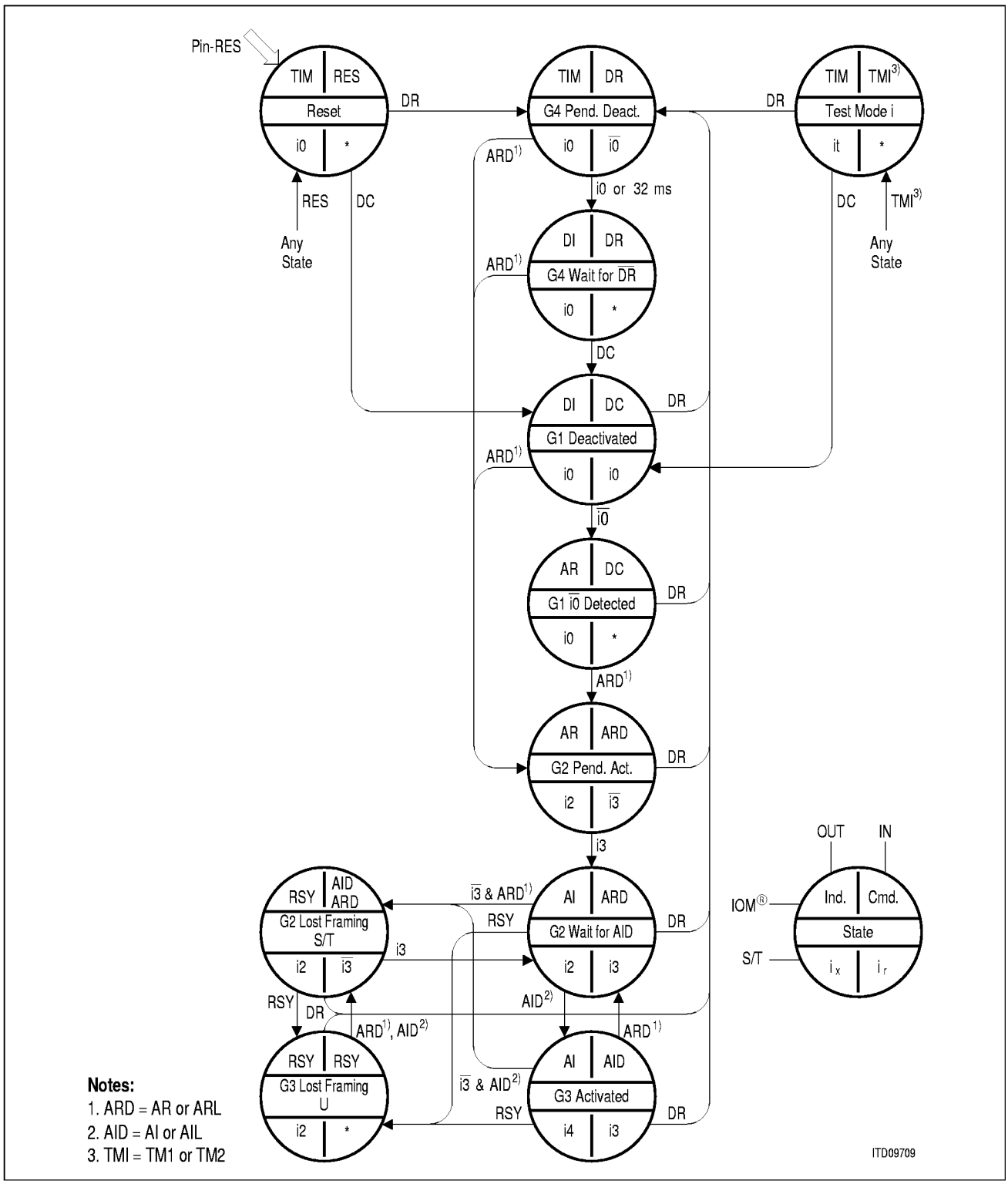


Figure 51 S-Transceiver NT Mode State Diagram

Table 21 S-Transceiver C/I Codes

Code				NT		TE	
				IN	**OUT**	**IN**	**OUT**
0	0	0	0	DR	TIM	TIM	DR
0	0	0	1	RES	–	RES	RES
0	0	1	0	TM1	–	TM1	TM1
0	0	1	1	TM2	–	TM2	TM2
0	1	0	0	RSY	RSY	–	RSY
0	1	0	1	–	–	–	–
0	1	1	0	–	–	–	–
0	1	1	1	–	–	–	PU
1	0	0	0	AR	AR	AR8	AR
1	0	0	1	–	–	AR10	–
1	0	1	0	ARL	–	ARL	ARL
1	0	1	1	–	CVR	–	CVR
1	1	0	0	AI	AI	–	AI8
1	1	0	1	–	–	–	AI10
1	1	1	0	AIL	–	–	AIL
1	1	1	1	DC	DI	DI	DC

AI Activation Indication
AI8 Activation Indication with high priority
AI10 Activation Indication with low priority
AIL Activation Indication Loop
AR Activation Request
AR8 Activation Request with high priority
AR10 Activation Request with low priority
ARL Activation Request Loop
CVR Code Violation Received
DC Deactivation Confirmation
DI Deactivation Indication
DR Deactivation Request
PU Power-Up
RES Reset
RSY Resynchronizing
TIM Timer
TIM1 Test Mode 1 (2-kHz signal)
TM2 Test Mode 2 (96-kHz signal)

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