PRELIMINARY PRODUCT SPECIFICATION

Z8604

NMOS Z8 8-BIT MICROCONTROLLER

FEATURES

- 8-bit NMOS Microcomputer, 18-pin DIP
- Low Cost
- 4.5 to 5.5 Volt Operating Range
- Low Power Consumption—600 mW (typical)
- Fast instruction pointer—1.5 microseconds at 8MHz
- 14 input/output lines
- All inputs are Schmitt triggered
- 1K byte of ROM
- Two programmable 8-bit Counter/Timers each with 6-bit programmable prescaler
- 6 vectored, priority interrupts from 5 different sources
- Clock speed 1 to 8MHz
- Watchdog/Power-On Reset Timer
- Bit Programmable RC Oscillator
- On-chip oscillator that accepts a crystal, ceramic resonator, RC or external clock drive.

GENERAL DESCRIPTION

The Z8604 microcontroller (MCU) introduces a new level of sophistication to single-chip architecture. The Z8604 is a member of the Z8 single-chip microcontroller family with 1K of ROM. The device is housed in a 18-pin DIP, and is NMOS compatible. Zilog's NMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z8604 architecture is characterized by Zilog's 8-bit microcontroller core. The MCU offers a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in many industrial, high volume, peripheral types, and advanced scientific applications.

The device applications demand powerful I/O capabilities. The MCU fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

There are two basic address spaces available to support the wide range of configurations: Program Memory and 76 bytes of General Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and input/output data communication, the Z8604 offers two on-chip counter/timers with a large number of user selectable modes (Figure 1).

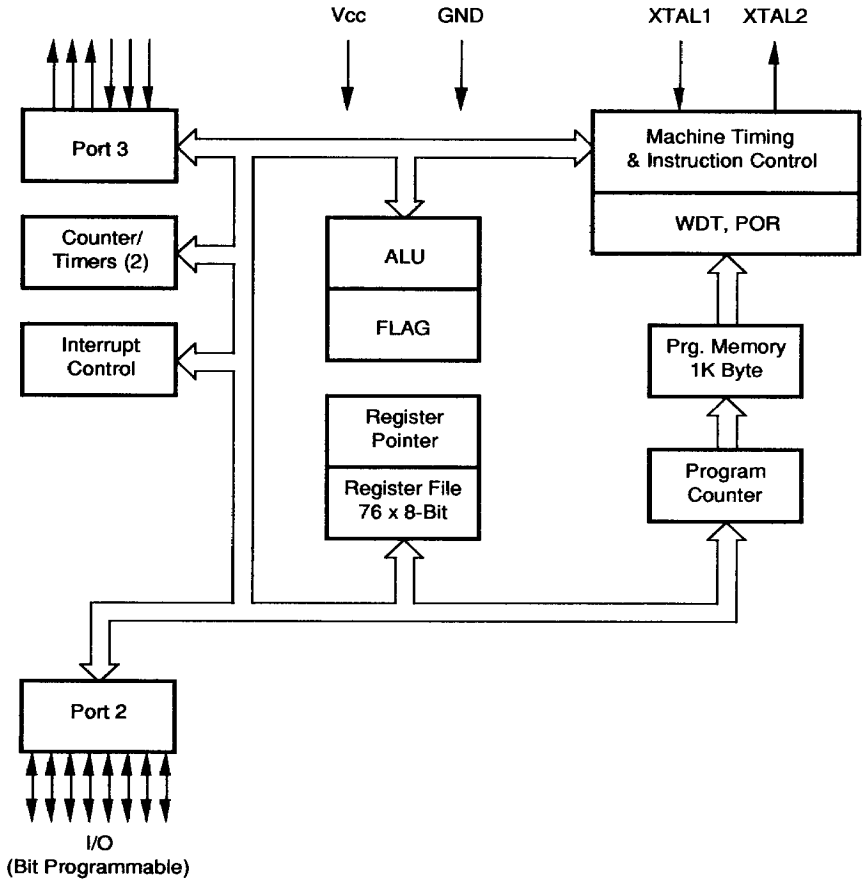


Figure 1. Functional Block Diagram

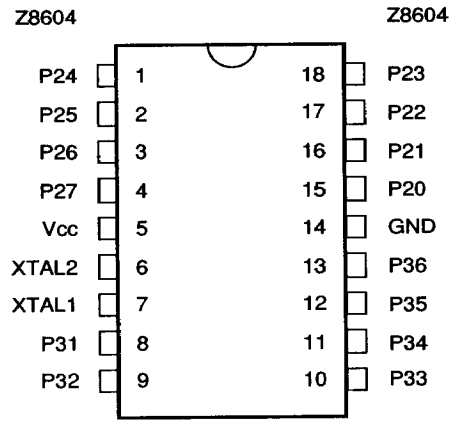


Figure 2. Pin Configuration

PIN DESCRIPTION

Table 1. Pin Description

Pin #	Symbol	Function	Direction
1-4	P24-7	Port 2 pin 4,5,6,7	In/Output
5	Vcc	Power Supply	Input
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-3	Port 3 pin 1,2,3	Fixed Input
11-13	P34-6	Port 3 pin 4,5,6	Fixed Output
14	GND	Ground, V_{SS}	Input
15-18	P20-3	Port 2 pin 0,1,2,3	In/Output

PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input).
This pin connects a parallel-resonant crystal, ceramic resonator or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output).
This pin connects a parallel-resonant crystal, ceramic resonator to the on-chip oscillator output.

Port 2 P20-P27. Port 2 is an 8-bit, bidirectional, NMOS compatible I/O port. These 8 I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt triggered. Bits programmed as outputs are globally programmed as either push-pull or open drain (Figure 3).

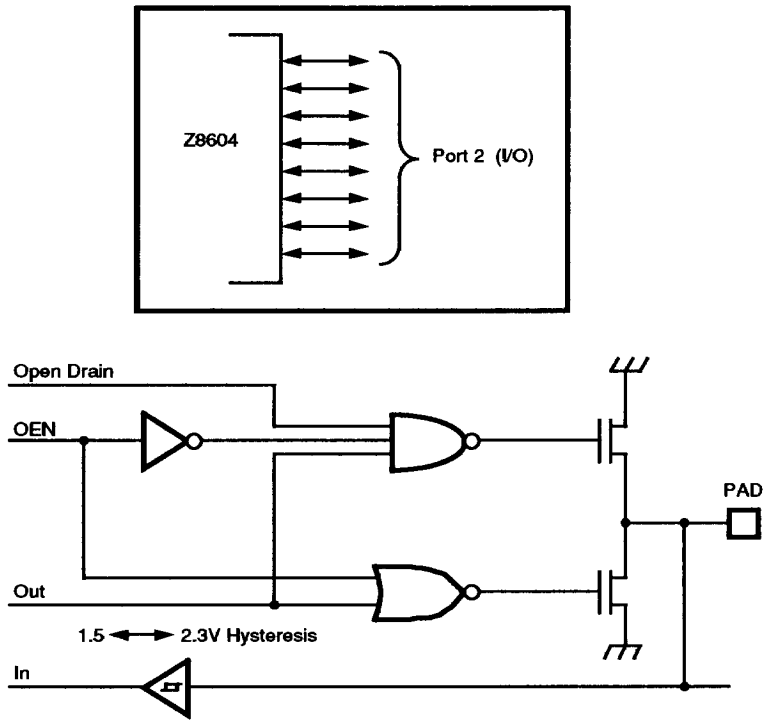


Figure 3. Port 2 Configuration

Port 3 P31-P36. Port 3 is a 6-bit port, NMOS compatible with three fixed input and three fixed output lines. These six lines consist of three fixed input (P31-P33) and three fixed output port (P34-P36) lines. Pins P31, P32 and P33 are standard Schmitt triggered NMOS inputs. Pins P34,P35,and P36 are push-pull outputs. Access to counter/timer 1 is made through P31 (Tin) and P36 (Tout) (Figure 4).

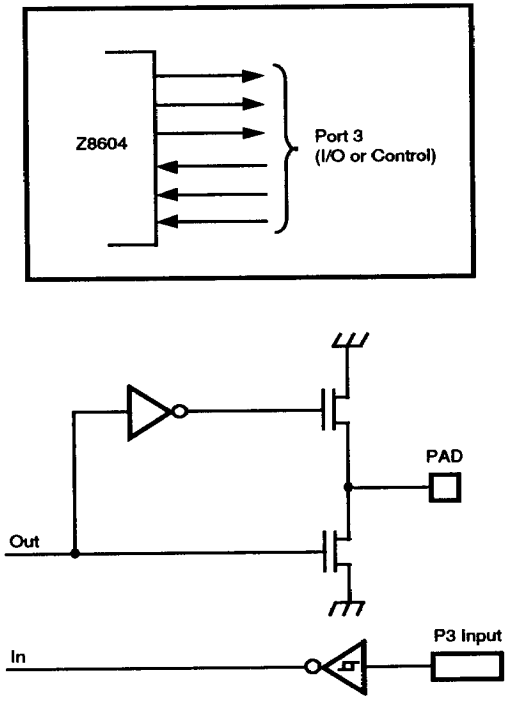


Figure 4. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z8 MCU incorporates special functions to enhance the Z8's application in industrial, scientific research and advanced technologies applications.

Reset

The device resets in one of the following conditions:

Power-On Reset
Watch-Dog Timer

Program Memory

The Z8604 can address up to 1K byte of internal program memory (Figure 5). This 1K byte Program Memory is mask programmable. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 1024 consists of on-chip mask-programmed ROM.

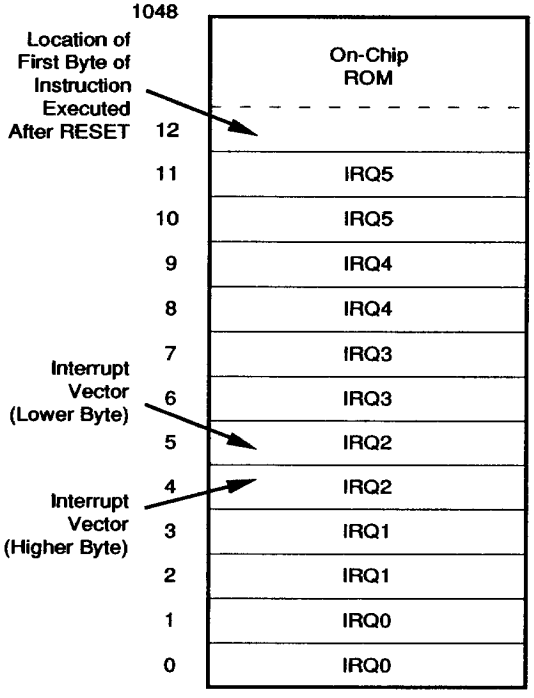


Figure 5. Program Memory Map

Register File

The Register File consists of two I/O port registers, 76 general-purpose registers and 15 control and status registers (Figure 6). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 7). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

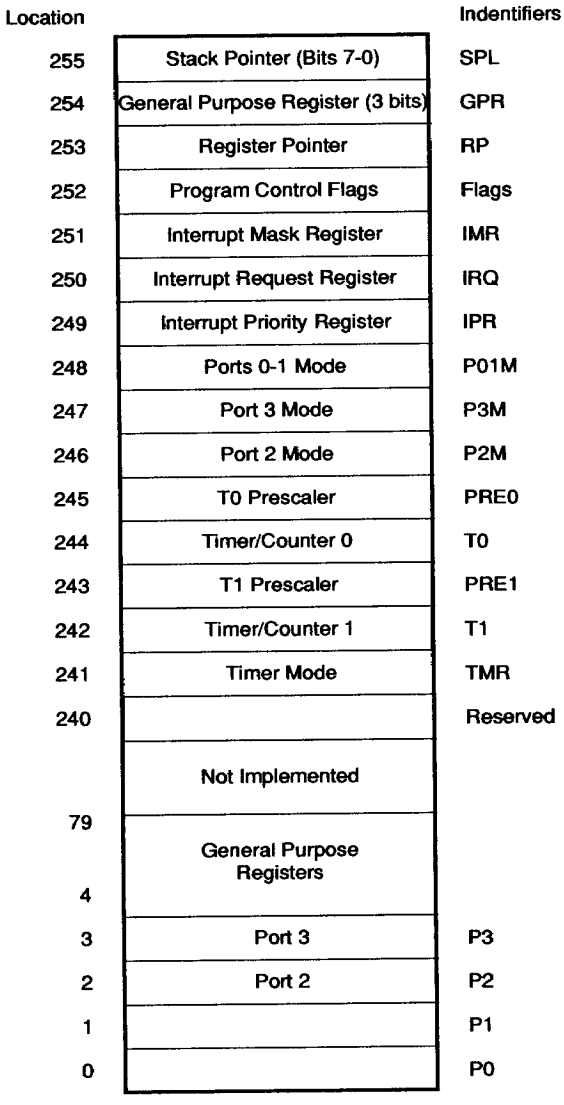


Figure 6. Register File

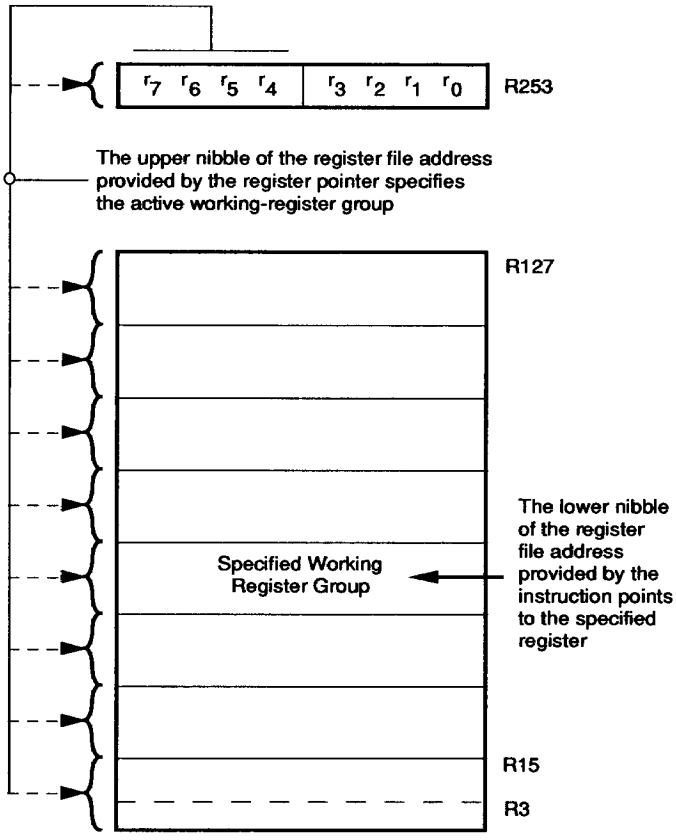


Figure 7. Register Pointer

Stack
The Z8604 has an 8-bit Stack Pointer (R255) that is used for the internal stack that resides within the 76 general purpose registers.

Table 1. Control Registers

Addr	Register	Reset Condition	D7	D6	D5	D4	D3	D2	D1	D0	Comments
F0		Not Implemented									
F1	TMR	Unchanged	0	0	0	0	0	0	0	0	
F2	Timer/CNTR1	Unchanged	U	U	U	U	U	U	U	U	
F3	PRE1	Unchanged	U	U	U	U	U	U	0	0	
F4	Timer/CNTR0	Unchanged	U	U	U	U	U	U	U	U	
F5	PRE0	Unchanged	U	U	U	U	U	U	U	0	
F6	Port 2 MDE	Unchanged	1	1	1	1	1	1	1	1	
F7	Port 3 MDE	X X X X X X X 0 D0: 0=P2 Open drain, 1=Push pull	U	U	U	U	U	U	U	0	
F8	Port 01 MDE	X X X 4 X 2 X X	U	U	U	0	U	1	U	U	Reserved
F9	IR Priority	Unchanged	U	U	U	U	U	U	U	U	
FA	IR Request	X X 5 4 3 2 1 0 D0=IRQ0=P32 Input D1=IRQ1=P33 Input D2=IRQ2=P31 Input	U	U	0	0	0	0	0	0	
		D3=IRQ3=P32 Input Inverted D4=T0 D5=T1									IRQ3 is used for positive edge detection.
FB	IR Mask	Unchanged	0	U	U	U	U	U	U	U	
FC	Flags	Unchanged	U	U	U	U	U	U	U	U	
FD	RP	RP Bank	U	U	U	U	U	U	U	U	
FE	SPH	X X X X X 2 1 0	U	U	U	U	U	U	U	U	
FF	SPL	Unchanged	U	U	U	U	U	U	U	U	

Counter/Timers

There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 8).

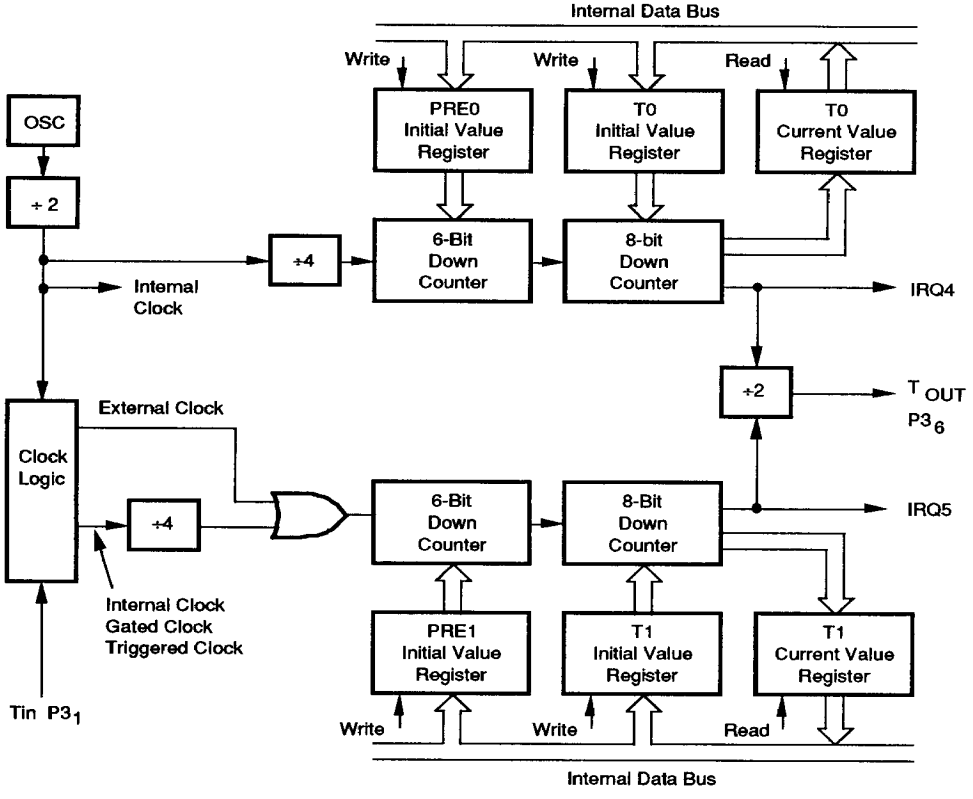


Figure 8. Counter/Timer Block Diagram

The 6-bit prescaler divides the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of count, a timer interrupt request-IRQ4 (T0) or IRQ5 (T1) is generated.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or not-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (Tout) through which T0, T1 or the internal clock are output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Interrupts

The Z8604 has six different interrupts from five different sources. The interrupts are maskable and prioritized (Figure 9). The five sources are divided as follow: three sources are claimed by Port 3 lines P31-P33, and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests, (Table 2).

Table 2. Interrupt Types, Sources and Vectors

Name	Source	Vector Location	Edge triggered	Comment
IRQ0	IRQ0	0,1	Falling	Ext (P32)
IRQ1	IRQ1	2,3	Falling	Ext (P33)
IRQ2	IRQ2, Tin	4,5	Falling	Ext (P31)
IRQ3		6,7	Rising	Ext (P32)
IRQ4	T0	8,9		Internal
IRQ5	T1	10,11		Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register. All Z8604 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled. This determines which of the interrupt requests needs services.

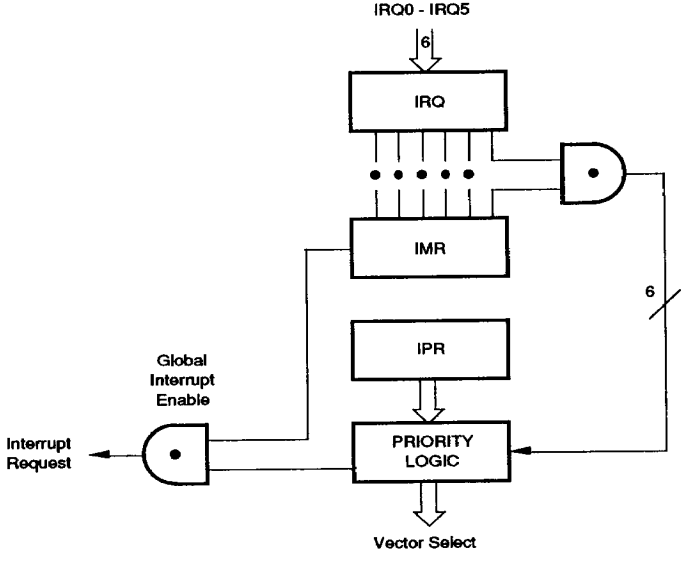


Figure 9. Interrupt Block Diagram

Clock

The Z8604 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 to 8 MHz max, with a series resistance (RS) less than or equal to 100 Ohms (Figure 10a).

The Z8604 has an on-chip bit programmable RC Oscillator. The RC oscillator uses an internal capacitor and an external resistor to determine its operation frequency. The external resisitor is connected between VCC and XTAL1. Resistor values range from 0 to 100K. By connecting XTAL1 to VCC the maximum frequency is obtained (Figure 10b).

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance is between 15pf to 25pf which depends on the manufacturer of crystal, ceramic resonator and PCB layout) from each pin to ground.

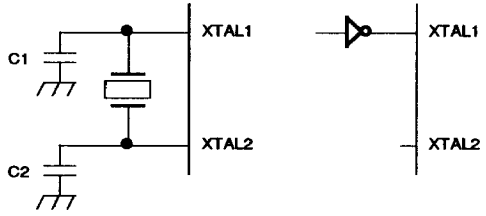


Figure 10a. Crystal Oscillator Configuration

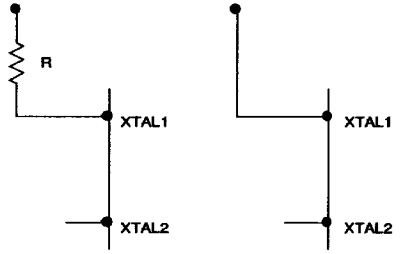


Figure 10b. RC Oscillator Configuration

Power-On Reset

A timer circuit clocked by a dedicated on-board RC oscillator and by the XTAL oscillator is used for the Power-On Reset (POR) timer function. The POR time allows Vcc and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by WDT timeout. The POR time is a nominal 40mS.

Watch Dog Timer (WDT). The WDT is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped,and must be refreshed by executing the WDT instruction every 10 ms; otherwise the Z8604 will reset itself.

WDT=5F (HEX)

Opcode WDT (5F%). The first time opcode %5F is executed, the WDT is enabled, subsequent execution clears the WDT counter. This has to be done at least every 10 ms. Otherwise, the WDT will time out and generate a reset. The generated reset is the same as a power on reset of 40 ms+18 XTALK clock cycles.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to ground. Positive current flows into the referenced pin (Figure 11).

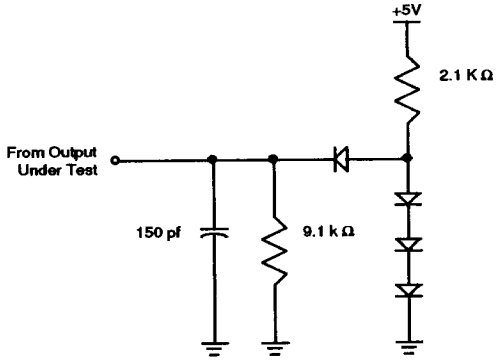


Figure 11. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
Vcc	Supply Voltage*	-0.3	+7.0	V
TSTG	Storage Temp	-65	+150	C
TA	Oper Ambient Temp	†		C

† See Ordering Information

Note (*). Voltage on all pins with respect to GND Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC}=+4.5 to +5.5V

Sym	Parameter	TA=0°C to 70°C Min	Max	Typ	Unit	Condition
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS}-0.3	8.0		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.75	V_{CC}		V	
V_{IL}	Input Low Voltage	0.3	1.5		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH}= -250 µA
V_{OL}	Output Low Voltage	0.4			V	I_{OL}= +2.0 mA
I_{IL}	Input Leakage	-10	10		µA	V_{IN}= 0V, V_{CC}
I_{OL}	Output Leakage	-10	10		µA	V_{IN}= 0V, V_{CC}
I_{CC}	Supply Current		120		mA	

REGISTER DIAGRAMS

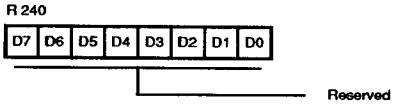


Figure 12. Reserved

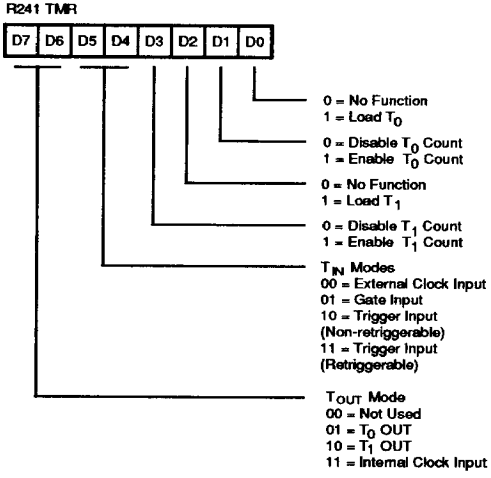


Figure 13. Timer Mode Register
(F1H; Read/Write)

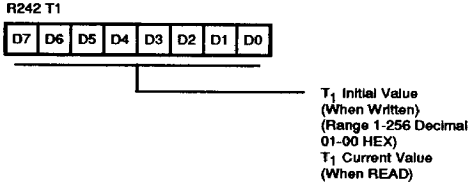


Figure 14. Counter Timer 1 Register
(F2H; Read/Write)

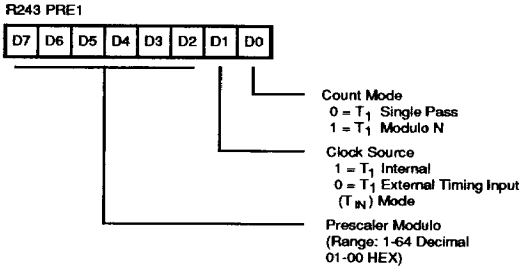


Figure 15. Prescaler 1 Register
(F3H; Write Only)

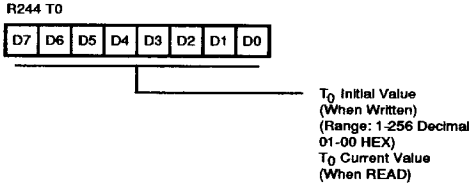


Figure 16. Counter/Timer 0 Register
(F4H; Read/Write)

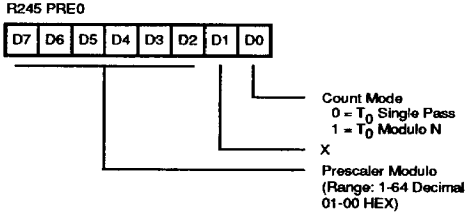


Figure 17. Prescaler 0 Register
(F5H; Write Only)

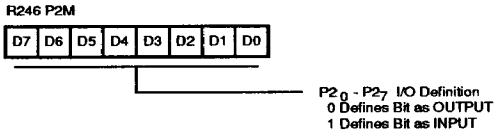


Figure 18. Port 2 Mode Register
(F6H; Write Only)

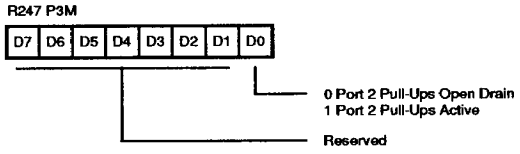


Figure 19. Port 3 Mode Register
(F7H; Write Only)

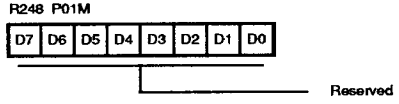


Figure 20. Port 0 and 1 Mode Register

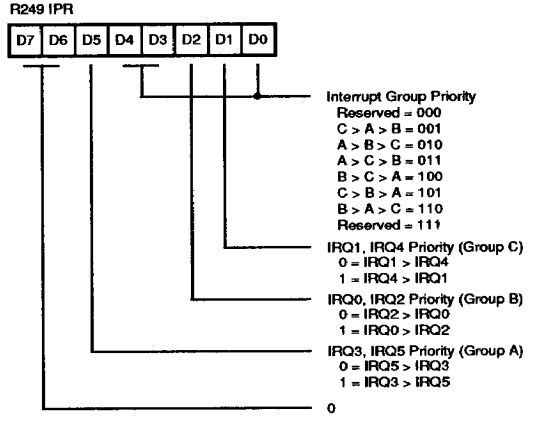


Figure 21. Interrupt Priority Register
(F9H; Write Only)

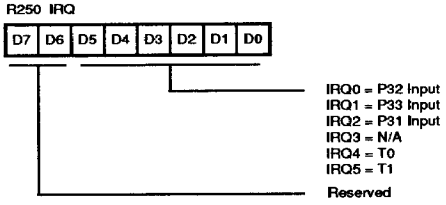


Figure 22. Interrupt Req Register
(FAH; Read/Write)

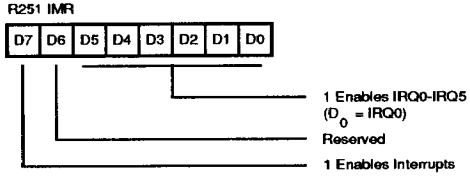


Figure 23. Interrupt Mask Register
(FBH; Read/Write)

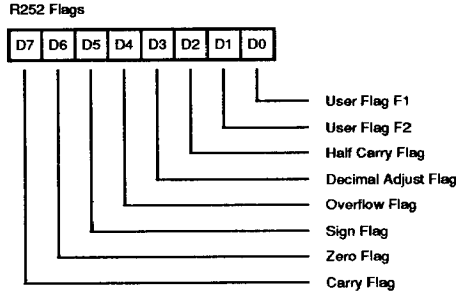


Figure 24. Flag Register
(FCH; Read/Write)

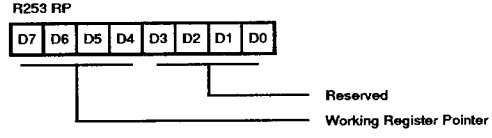


Figure 25. Register Pointer
(FDH; Read/Write)

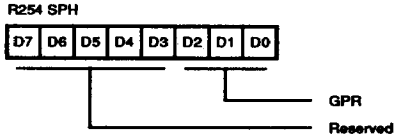


Figure 26. General Purpose Register
(FEH; Read/Write)

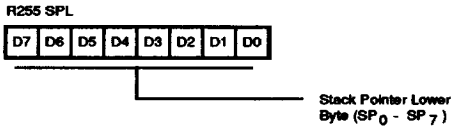


Figure 27. Stack Pointer
(FFH; Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed Address
DA	Direct Address
RA	Relative Address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-Register or indirect working-egister address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition Code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt Mask Register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

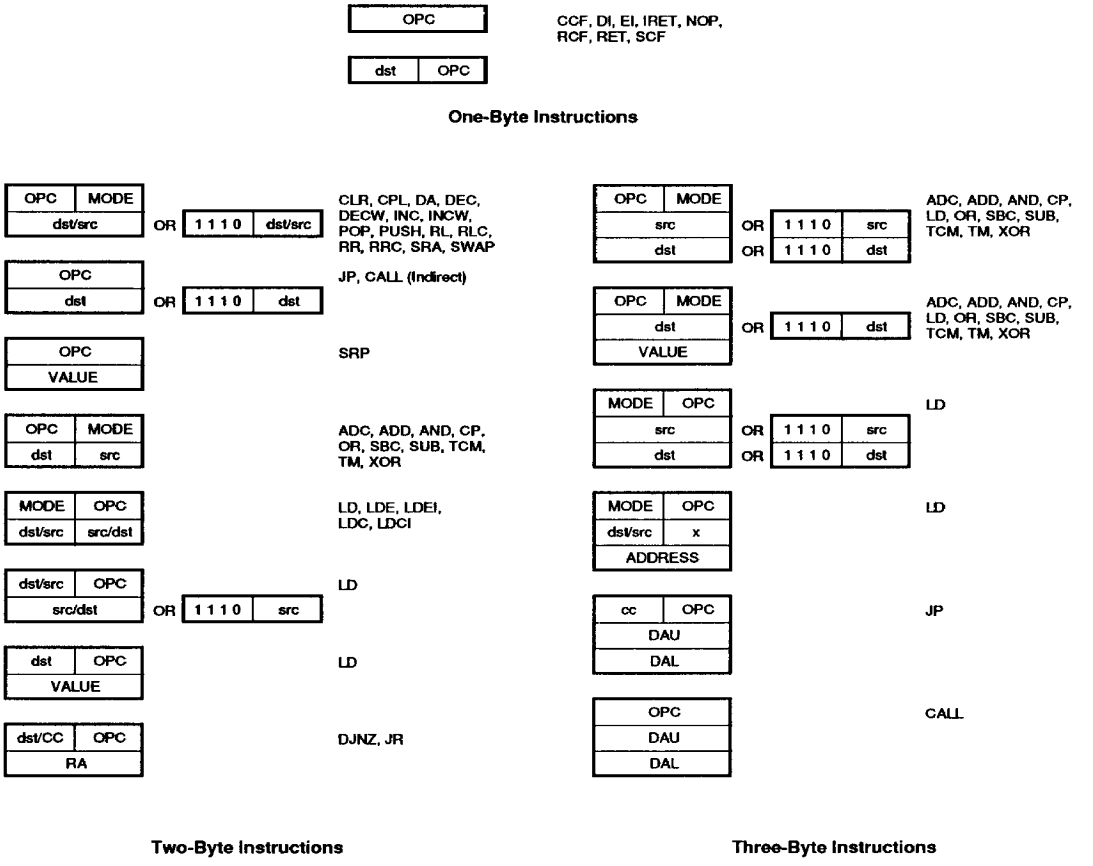
Affected flages are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

Table 3. Condition Codes

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "—". For example:

dst — dst + src

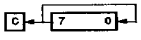
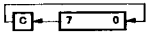
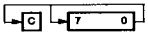
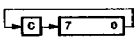
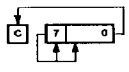
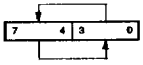
indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
WDT			5F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r r Ir R R R IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

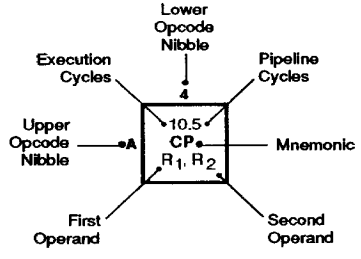
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								5.0 **WDT**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								
8	10.5 **DECW** RR1	10.5 **DECW** IR1														**DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2					10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	**LDCI** Ir1,Irr2		20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2				3		1	



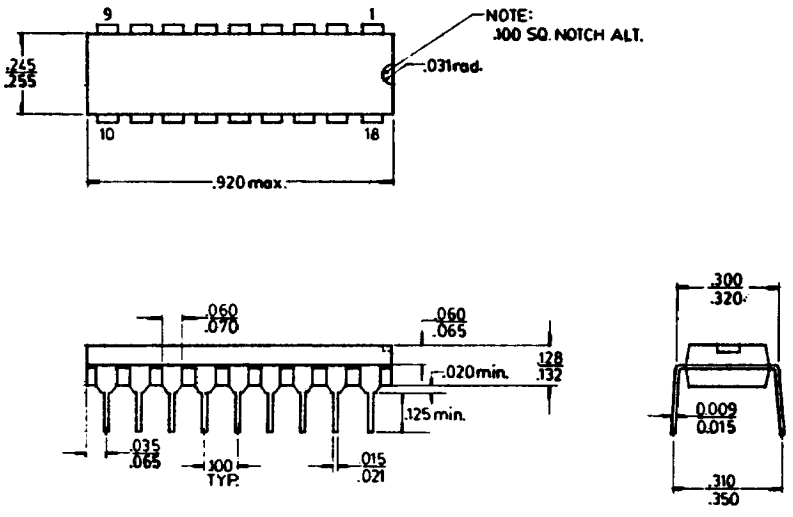
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank are not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



18-Pin Plastic Package Diagram

ORDERING INFORMATION

Z8604

8 MHz
Z0860408PSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package
P = Plastic DIP
V = Plastic Chip Carrier
C = Ceramic DIP
L = Ceramic LCC

Longer Lead Time
F = Plastic Quad Flat Pack

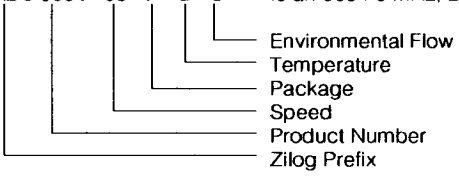
Temperature
E = -40°C to +100°C
S = 0°C to +70°C

Speed
8 = 8 MHz

Environmental
C = Plastic Standard

Example:

Z 0 8604 08 P S C Is an 8604 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow.



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