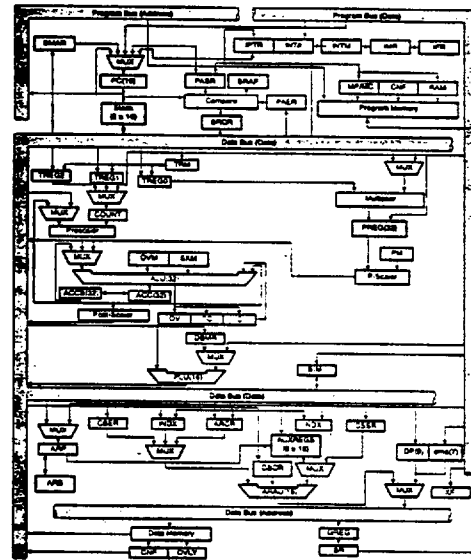# Radiation Hardened
# 320C50RP CMOS Field 16-Bit Microprocessor

## For Space Applications

SEI's 320C50RP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilo-rad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 320C50RP is 100% pin-for-pin compatible with Texas Instruments TMS 320C50. This device is structured using static CMOS integrated circuit technology. The combination of separate buses for program memory and data memory, additional on-chip peripherals, more on-chip memory, and a highly specialized instruction set is the basis of the operational flexibility and speed of this device. The 320C50RP is designed to execute more than 28 million instructions per second. It also has new static design techniques for minimizing power consumption and maximizing radiation hardness. Many other key features are available for this device. Two indirectly addressed circular buffers are used for circular addressing. Sixteen software-programmable wait-state generators for program, data, and I/O memory spaces. Capable of surviving space environments, the 320C50RP is ideal for satellite, spacecraft, and space probe missions. RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 320C50RP is available in Class S packaging and screening.
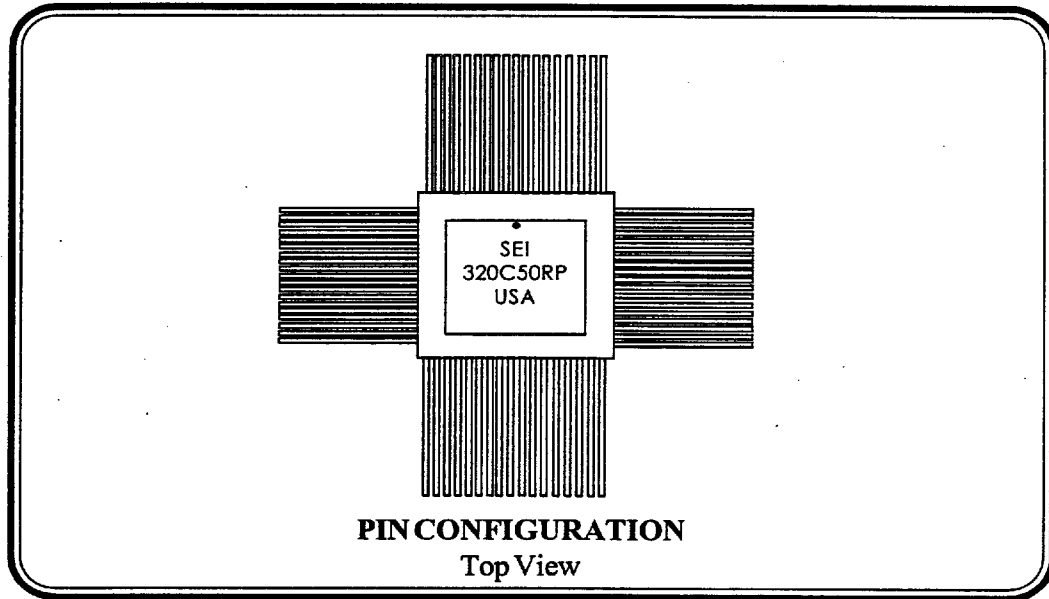
# Radiation Hardened
# 320C50RP
## CMOS Field
## 16 - Bit Microprocessor



**PIN CONFIGURATION**
Top View

SEI
320C50RP
USA

## Features:

- Total Memory Address Range is 224K 16-bit Words Divided Into 4 Segments
  - 64K program memory
  - 64K local data memory
  - 32K global data memory
  - 64K I/O port memory
- Pin Compatible to TMS320C50
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
  - 132 Pin RAD-PAK® quad flat pack (0.9 in. x 0.9 in.)
- Weight - 12 grams
- JEDEC Approved Byte Wide Pinout

- Enhanced Mode CMOS Technology
  - RAM-based memory operation
  - Sixteen programmable wait-state generators for program, data, and I/O memory spaces
  - Divide-by-one clock option
  - On-chip clock generator
  - On-chip scan-based emulation logic
  - Extended hold operation for concurrent external DMA
  - Time-division multiple-access serial port
  - Index addressing mode
  - Extended hold operation for concurrent external DMA
  - JTAG boundary scan logic

Specifications and design are subject to change without notice.

**TQM**
Total Quality Management.

May 1995

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## 320C50RP RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.75 | 5.25 | V |
| Supply Voltage | $V_{SS}$ | -0.3 | 7 | V |
| High-level input voltage<br>CLKIN, CLKIN2<br>CLKX, CLKR, TCLKX, TCLKR<br>All others | $V_{IH}$ | 3.0<br>2.5<br>2.0 | $V_{DD}$+0.3<br>$V_{DD}$+0.3<br>$V_{DD}$+0.3 | V<br>V<br>V |
| Low-level input voltage | $V_{IL}$ | -0.3 | 0.8 | V |
| High-level output current | $I_{OH}$ | | -300 | uA |
| Low-level output current | $I_{OL}$ | | 2 | mA |
| Input clock frequency | $f_x$ | 0 | 40.96 | MHz |
| Operating case temperature | T | -55 | +125 | °C |

## 320C50RP SWITCHING CHARACTERISTICS[1]

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| CLKOUT1 cycle time | $t_{c(CO)}$ | 48.8 | | ns |
| CLKIN high to CLKOUT1 high/low | $t_{d(CIH-CO)}$ | 3 | 20 | ns |
| CLKOUT1 fall time | $t_{f(CO)}$ | | | ns |
| CLKOUT1 rise time | $t_{r(CO)}$ | | | ns |
| CLKOUT1 low pulse duration | $t_{w(COL)}$ | H-2 | H+2 | ns |
| CLKOUT1 high pulse duration | $t_{w(COH)}$ | H-2 | H+2 | ns |

Notes:
1. $H=0.5t_{c(CO)}$

## 320C50RP DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| High-level output voltage, $I_{OH}$=Max | $V_{OH}$ | 2.4 | | V |
| Low-level output voltage, $I_{OL}$=Max | $V_{OL}$ | | 0.6 | V |
| Three-state current<br>($V_{DD}$ = Max)<br>BR\<br>All other three-state | $I_Z$ | <br><br>-400<br>-20 | <br><br>20<br>20 | <br><br>uA<br>uA |
| Input current<br>($V_I$= $V_{SS}$ to $V_{DD}$)<br>TRST\ pin (with internal pulldown)<br>TMS, TCK, TDI pins (with internal pullups)<br>X2/CLKIN pin<br>All other input-only pins | $I_I$ | <br>-10<br>-400<br><br>-50<br>-10 | <br>800<br>10<br><br>+50<br>10 | <br>uA<br>uA<br><br>uA<br>uA |
| Supply current, core CPU<br>Operating $T_A$=25°C, $V_{DD}$=5.25V,$f_x$=40/96MHz | $I_{DDC}$ | | 130 | mA |
| Supply current, pins<br>Operating $T_A$=25°C, $V_{DD}$=5.25V,$f_x$=40.96MHz | $I_{DDP}$ | | 85 | mA |
| Supply current, standby<br>IDLE2, clocks shut off | $I_{DD}$ | | 40 | uA |
| Input capacitance | $C_I$ | | 20 | pF |
| Output capacitance | $C_O$ | | 20 | pF |

## 320C50RP READ TIMING CHARACTERISTICS[1]

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Setup time, address valid before RD\ low | $t_{su(A)R}$ | H-10 | | ns |
| Hold time, address valid after RD\ high | $t_{h(A)R}$ | 0 | | ns |
| Delay time, RD\ high to WE\ low | $t_{d(RW)}$ | 2H-5 | | ns |
| RD\ high pulse duration | $t_{w(RH)}$ | H-2 | | ns |
| RD\ low pulse duration | $t_{w(RL)}$ | H-2 | H+2 | ns |
| Read data access from address valid | $t_{a(A)}$ | | 2H-18 | ns |
| Read data setup time before RD\ high | $t_{su(D)R}$ | 10 | | ns |
| Read data hold time after RD\ high | $t_{h(D)R}$ | 0 | | ns |
| Read data access time after RD\ low | $t_{a(R)}$ | | H-10 | ns |

## SPACE ELECTRONICS INC.

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| Parameter | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Setup time, address valid before WE\ low | $t_{su(A)W}$ | H-5 | | ns |
| Hold time, address valid after WE\ high | $t_{h(A)W}$ | H-10 | | ns |
| WE\ low pulse duration | $t_{w(WL)}$ | 2H-2 | 2H+2 | ns |
| WE\ high pulse duration | $t_{w(WH)}$ | 2H-2 | | ns |
| Delay time, WE\ high to RD\ low | $t_{d(WR)}$ | 2H-10 | | ns |
| Setup time, write data valid before WE\ high | $t_{su(D)W}$ | 2H-20 | 2H | ns |
| Hold time, write data valid after WE\ high | $t_{h(D)W}$ | H-5 | H+10 | ns |
| Enable time, WE\ to data bus driven | $t_{en(D)W}$ | -5 | | ns |

Notes:
1. $H = 0.5t_{c(CO)}$

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| READY setup time before CLKOUT1 rises | $t_{su(R-CO)}$ | 10 | | ns |
| READY hold time after CLKOUT1 rises | $t_{h(CO-R)}$ | 0 | | ns |
| READY setup time before RD\ falls | $t_{su(R)R}$ | 10 | | ns |
| READY hold time after RD\ falls | $t_{h(R)R}$ | 5 | | ns |
| READY valid after WE\ falls | $t_{v(R)W}$ | H-15 | | ns |
| READY hold after WE\ falls | $t_{h(R)W}$ | H+5 | | ns |

## 320C50RP GENERAL TIMING REQUIREMENTS[1]

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| CLKIN cycle time | $t_{c(CI)}$ | 24.4 | | ns |
| CLKIN fall time | $t_{f(CI)}$ | | 5 | ns |
| CLKIN rise time | $t_{r(CI)}$ | | 5 | ns |
| CLKIN low pulse duration | $t_{w(CIL)}$ | 11 | | ns |
| CLKIN high pulse duration | $t_{w(CIH)}$ | 11 | | ns |
| CLKIN2 cycle time | $t_{c(CI)}$ | 48.8 | 75 | ns |
| CLKIN2 fall time | $t_{f(CI)}$ | | 5 | ns |
| CLKIN2 rise time | $t_{r(CI)}$ | | 5 | ns |
| CLKIN2 low pulse duration | $t_{w(CIL)}$ | 15 | 60 | ns |
| CLKIN2 high pulse duration | $t_{w(CIH)}$ | 15 | 60 | ns |

Notes:
1. $H = 0.5 t_{c(CO)}$

## 320C50RP RESET, INTERRUPT, AND BIO\ TIMINGS[1]

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| INT1\ - INT4\, NMI\, RS\ setup time before CLKOUT1 low | $t_{su(IN)}$ | 15 | | ns |
| INT1\ - INT4\, NMI\, RS\ hold time after CLKOUT1 low | $t_{h(IN)}$ | 0 | | ns |
| INT1\ - INT4\, NMI\ low pulse duration, synchronous | $t_{w(INL)s}$ | 4H+15 | | ns |
| INT1\ - INT4\, NMI\ high pulse duration, synchronous | $t_{w(INH)s}$ | 2H+15 | | ns |
| INT1\ - INT4\, NMI\ low pulse duration, asynchronous | $t_{w(INL)a}$ | 6H+15 | | ns |
| INT1\ - INT4\, NMI\ high pulse duration, asynchronous | $t_{w(INH)a}$ | 4H+15 | | ns |
| RS\ set up time before X2/CLKIN low | $t_{su(R)}$ | 10 | | ns |
| RS\ low pulse duration | $t_{w(RSL)}$ | 12H | | ns |
| RS\ high to reset vector fetch | $t_{d(FX)}$ | 34H | | ns |
| BIO\ low pulse duration, synchronous | $t_{w(BI)s}$ | 15 | | ns |
| BIO\ low pulse duration, asynchronous | $t_{w(BI)a}$ | H+15 | | ns |
| BIO\ setup before CLKOUT1 low | $t_{su(BI)}$ | 15 | | ns |
| BIO\ hold time after CLKOUT1 low | $t_{h(BI)}$ | 0 | | ns |

Notes:
1. $H = 0.5 t_{c(CO)}$

## 320C50RP Package Ordering Guide

| Package Style | Case Outline | 1/ | Description |
|---|---|---|---|
| Q | Q-132 | | 132 Pin Quad Flat Package |

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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