APR 26 1993

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Order this data sheet
by 32S128/D

Military 32S128

Advance Information

4 Megabit CMOS SRAM User-Configurable Multichip Module

The Motorola 32S128 is a 4-megabit CMOS SRAM module organized as 128K words by 32 bits, 256K x 16 or 512K x 8. The module is constructed on a multilayer ceramic substrate, hermetically sealed, with a welded metal cover, hex-in-line package (HIP) utilizing four 128K x 8 SRAM devices.

This module is compatible with most 66 pin HIP packaged SRAM, EEPROM and Flash memory modules.

The 32S128 is available with access times of 25 to 120 ns over commercial, Industrial, and Military temperature ranges.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both low. Reading the device is accomplished by taking the chip selects low while write enable remains high. Under these conditions the contents of the memory locations specified on the address pins will appear on the data input/output pins.

FEATURES:

- Access Times 25 to 120 ns
- 66-pin, PGA Type, 1.2 inch square HIP Package
- User-Configurable as 128K x 32, 256K x 16 or 512K x 8
- Hermetic Ceramic Package
- Battery Back-Up Operation
- Commercial, Industrial, and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Commercial Plus Processing Available
- Low Power CMOS Fully Static Design
- 5 Volt Power Supply
- Built in Decoupling Capacitors and Multiple Ground pins for Low Noise Operation
- Military Temperature Range (- 55°C to + 125°C)
- MIL-STD-883 Compliant Devices (Planned)
- Military Screening and Burn-In Available

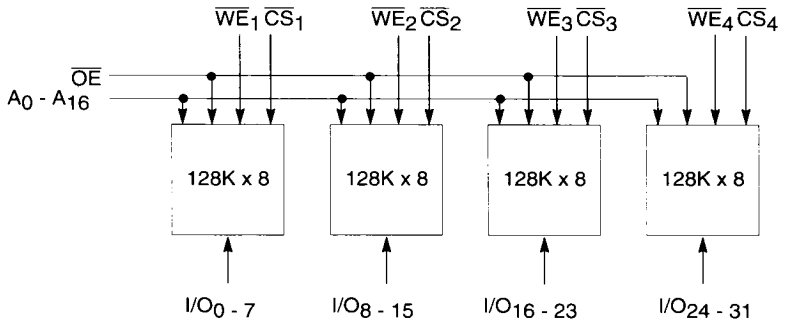
SRAM MULTICHIP MODULE

AVAILABLE AS
1) JAN: N/A
2) SMD: Planned
3) 883: 32S128-XX/BZCJC
4) CMP: 32S128-XX/ *
*** See Commercial Plus and Avionics Options: (BR914/D)**
PACKAGE: PGA: Z

XX = Speed in ns (25 to 120)
20 ns Planned Q4 1993

PIN NAMES	
A_0 - A_{16}	Address Inputs
I/O_0 - I/O_{31}	Data Input/Output
$\overline{CS}_{1-4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}_{1-4}$	Write Enable
V_{CC}	+ 5.0 Power
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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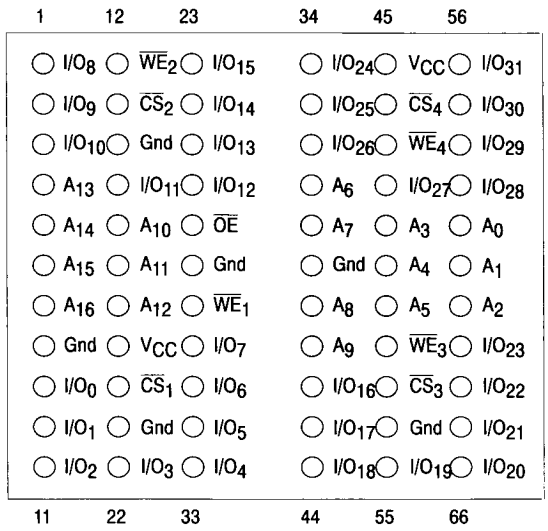
Pin Assignment



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Operating Temperature	T_A	- 55 to + 125	°C
Storage Temperature Range	T_{STG}	- 65 to + 150	°C
Supply Voltage (Relative to GND)	V_G	- 0.5 to + 7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High-Z	Standby (deselect/power down)
L	L	H	Read	Data Out	Active
L	H	H	Read	High-Z	Active (deselect)
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	- 0.5	+ 0.8	V

CAPACITANCE (@ T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz	30	pF

Periodically sampled rather than 100% tested.

DC CHARACTERISTICS

(V_{CC} = 5 V, T_A = - 55°C to + 125°C)

Parameter	Symbol	Limits		Unit	Test Condition (Unless Otherwise Specified)
		Min	Max		
Input Leakage Current	I_{LI}		8	µA	V_{CC} = Max, V_{IN} = Gnd
Output Leakage Current	I_{LO}		8	µA	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Gnd to V_{CC}, V_{CC} = Max
Operating Supply Current x 32 mode	I_{CCx32}		450 *	mA	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max
Operating Supply Current x 16 mode	I_{CCx16}		280 *	mA	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max
Operating Supply Current x 8 mode	I_{CCx8}		150 *	mA	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max
Standby Current	I_{SB}		200	mA	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max, V_{CC} = Max
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 2.1 mA (- 70 to 120 ns), I_{OL} = 8 mA (- 25 to - 55 ns)
Output High Voltage	V_{OH}	2.4		V	I_{OH} = - 1.0 mA (for - 70 to - 125 ns)
		2.4		V	I_{OH} = - 4.0 mA (for - 25 to - 55 ns)

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AC CHARACTERISTICS

(V_{CC} = 5 V,V_{SS} = 0 V, T_A = - 55°C to + 125°C)

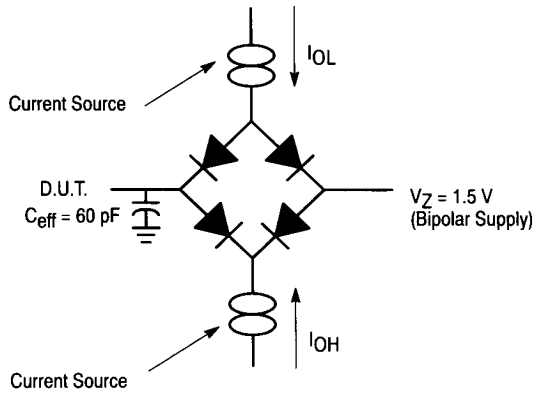
Parameter	Symbol	Limits								Unit
Read Cycle:		- 25		- 35		- 45		- 55		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		55		ns
Address Access Time	t_{AA}		25		35		45		55	ns
Data Hold from Address Change	t_{OH}	4		4		4		4		ns
Chip Select Access	t_{ACS}		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		15		20		25		30	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip deselect to Output in High Z	t_{CHZ}[1]		12		15		20		25	ns
Output disable to Output in High Z	t_{OHZ}[1]		12		15		20		25	ns

1. This parameter is guaranteed by design but not tested.

Parameter	Symbol	Limits								Unit
Read Cycle:		- 70		- 85		- 100		- 120		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Data Hold from Address Change	t_{OH}	5		5		5		5		ns
Chip Select Access	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		40		45		50	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip deselect to Output in High Z	t_{CHZ}[1]		30		35		40		50	ns
Output disable to Output in High Z	t_{OHZ}[1]		30		35		40		50	ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameters	Typ.	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall Time	5	ns
Input Timing Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from - 2 V to + 7 V
I_{OL} & I_{OH} programmable from 0 to 16 mA
Tester Impedance Z_0 = 75Ω
V_Z is typically the midpoint of V_{OH} and V_{OL}
(i.e. (2.4 + 0.4)/2 = 1.4 V)
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit
D.U.T. Device Under Test
C_{eff} Effective Capacitance
ATE Tester Includes Jig Capacitance

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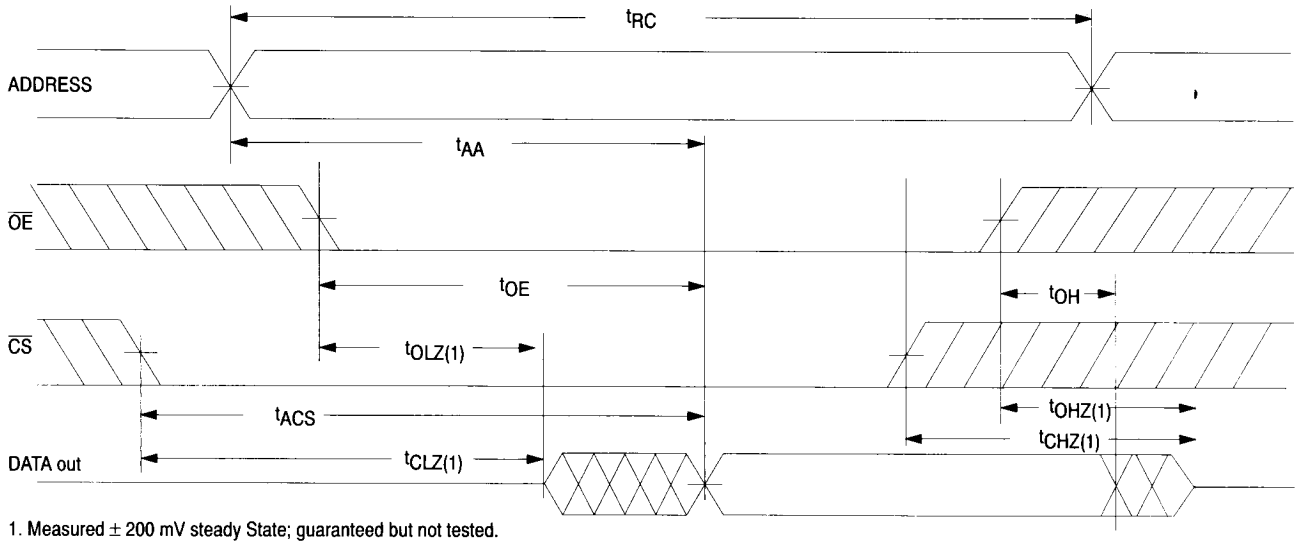
READ CYCLE TIMING DIAGRAM



1. Measured ± 200 mV steady State; guaranteed but not tested.

AC CHARACTERISTICS

(V_{CC} = 5 V, T_A = - 55°C to + 125°C)

Parameter	Symbol	Limits								Unit
Write Cycle:		- 25		- 35		- 45		- 55		
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		45		55		ns
Chp Select to End of Write	t_{CW}	20		30		40		45		ns
Address Valid to End of Write	t_{AW}	20		30		40		45		ns
Data to Write-Time Overlap	t_{DW}	15		18		20		25		ns
Data Hold from Write Time	t_{DH}	3		3		3		5		ns
Write Pulse Width	t_{WP}	20		25		35		40		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write to Output in High Z	t_{WHZ}[1]		10		15		15		20	ns

Parameter	Symbol	Limits								Unit
Write Cycle:		- 70		- 85		- 100		- 120		
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chp Select to End of Write	t_{CW}	65		80		90		110		ns
Address Valid to End of Write	t_{AW}	65		80		90		110		ns
Data to Write-Time Overlap	t_{DW}	30		35		40		55		ns
Data Hold from Write Time	t_{DH}	5		5		5		5		ns
Write Pulse Width	t_{WP}	45		50		55		65		ns
Address Setup Time	t_{AS}	5		5		5		5		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write to Output in High Z	t_{WHZ}[1]		30		35		40		50	ns

1. This parameter is guaranteed by design but not tested.

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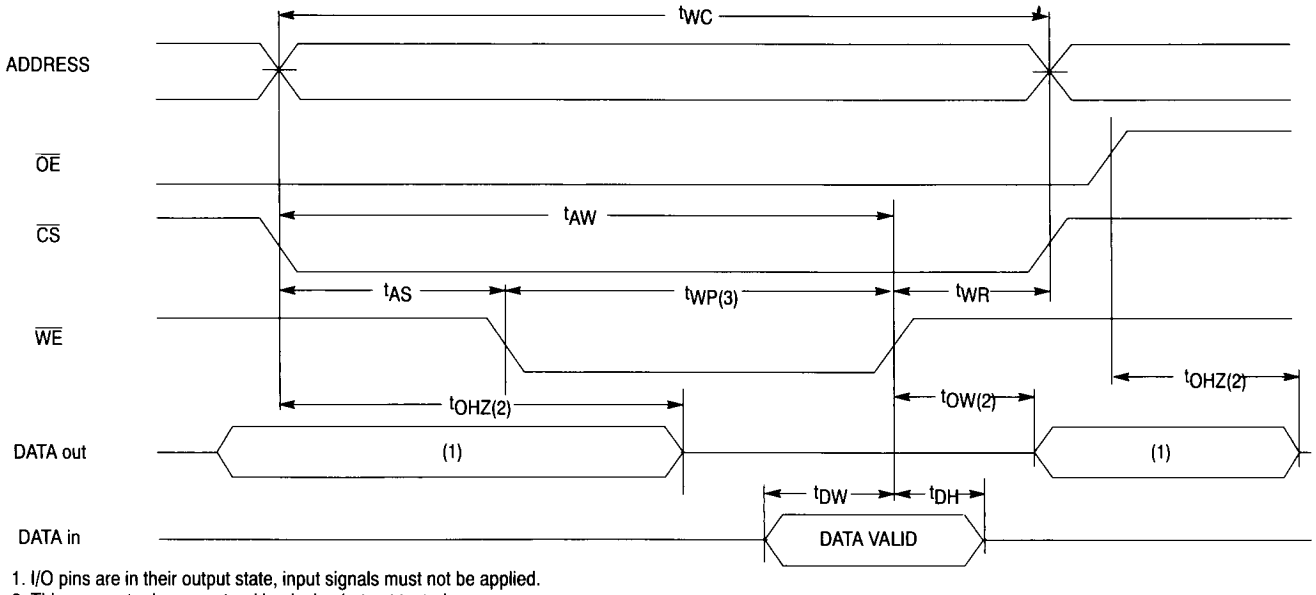
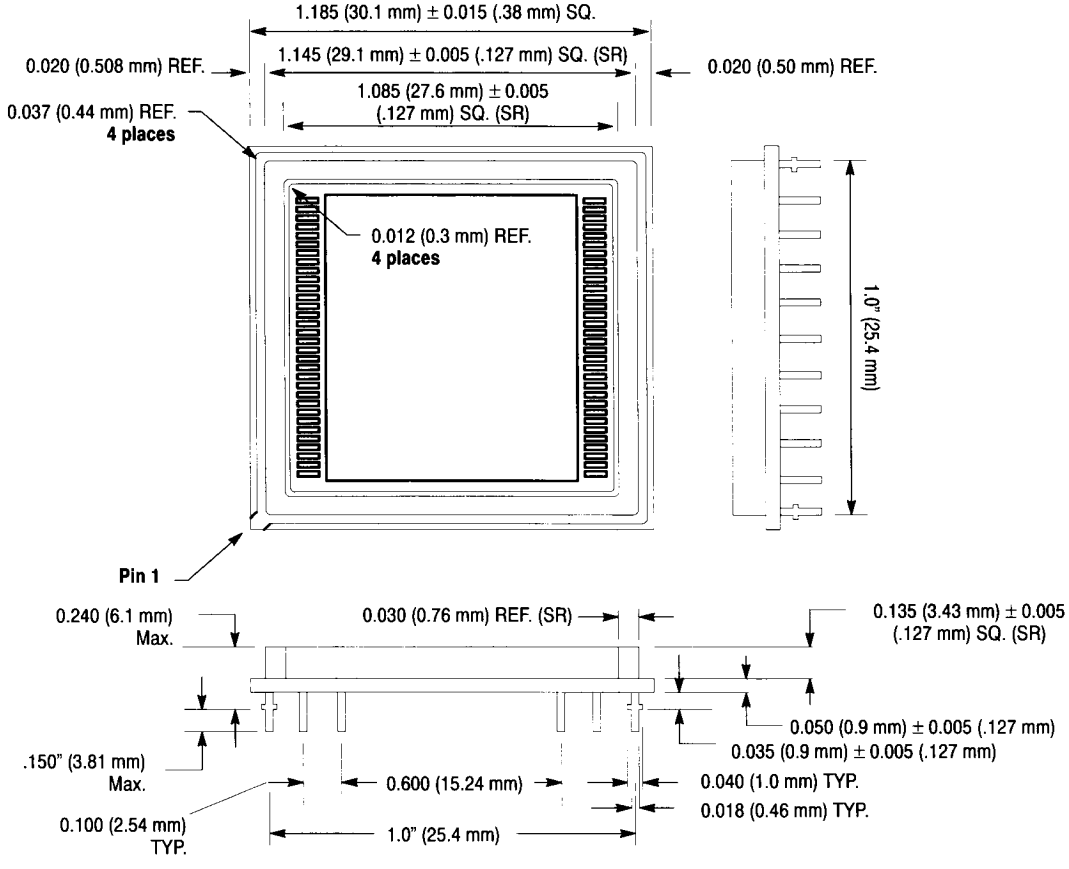
WRITE CYCLE TIMING DIAGRAM



1. I/O pins are in their output state, input signals must not be applied.
2. This parameter is guaranteed by design but not tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

Package Outline



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