# 16-bit bus transceiver with 30Ω series termination resistors (3-State)

# 74ABT162245A
# 74ABTH162245A

## FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple $V_{CC}$ and GND pins minimize switching noise
- 3-State buffers
- Output capability: +12mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74ABT16245A-1
- 74ABTH162245A incorporates bus hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

## DESCRIPTION

The 74ABT162245A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT162245A device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction (1DIR, 2DIR) inputs for direction control.

The 74ABT162245A is designed with 30 ohm series resistance in both the upper and lower output structures on both A and B ports. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receiver/transmitters.

The 74ABT162245A is the same as the 74ABT16245A-1. The part number has been changed to reflect industry standards

Two options are available, 74ABT162245A which does not have the bus hold feature and the 74ABTH162245A which incorporates the bus hold feature.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb}$ = 25°C; GND = 0V | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>nAx to nBx or nBx to nAx | $C_L$ = 50pF; $V_{CC}$ = 5V | 2.0<br>3.0 | ns |
| $C_{IN}$ | Input capacitance | $V_I$ = 0V or $V_{CC}$ | 3 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_O$ = 0V or $V_{CC}$; 3-State | 7 | pF |
| $I_{CCZ}$ | Quiescent supply current | Outputs disabled; $V_{CC}$ = 5.5V | 300 | nA |
| $I_{CCL}$ | | Outputs Low; $V_{CC}$ = 5.5V | 10 | mA |

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 48-Pin Plastic SSOP Type III | –40°C to +85°C | 74ABT162245A DL | BT162245A DL | SOT370-1 |
| 48-Pin Plastic TSSOP Type II | –40°C to +85°C | 74ABT162245A DGG | BT162245A DGG | SOT362-1 |
| 48-Pin Plastic SSOP Type III | –40°C to +85°C | 74ABTH162245A DL | BH162245A DL | SOT370-1 |
| 48-Pin Plastic TSSOP Type II | –40°C to +85°C | 74ABTH162245A DGG | BH162245A DGG | SOT362-1 |

# 16-bit bus transceiver with 30Ω series termination resistors (3-State)

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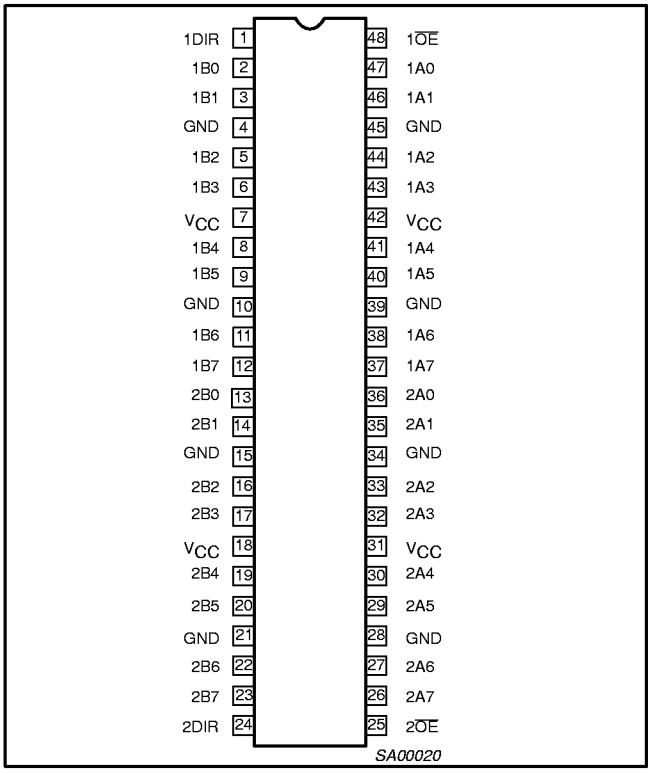
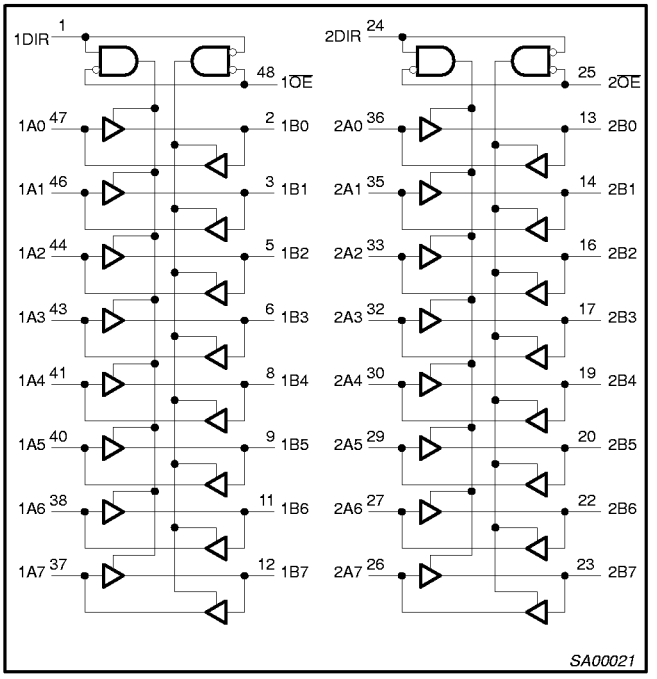
# 74ABTH162245A

## PIN CONFIGURATION




## LOGIC SYMBOL




## PIN DESCRIPTION

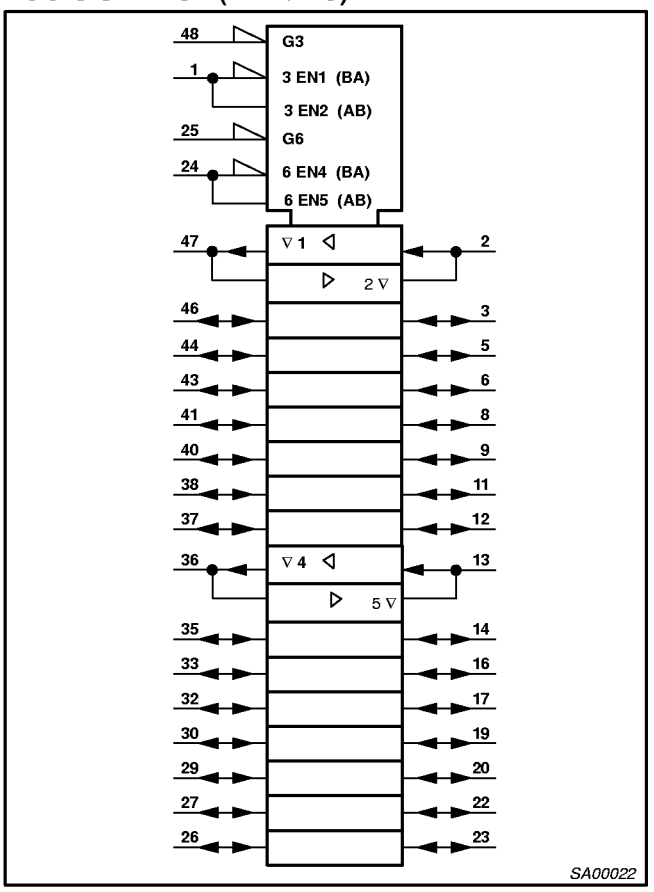
| SYMBOL | PIN NUMBER | NAME AND FUNCTION |
|---|---|---|
| 1DIR, 2DIR | 1, 24 | Direction control inputs (Active-High) |
| 1A0 – 1A7, 2A0 – 2A7 | 47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26 | Data inputs/outputs (A side) |
| 1B0 – 1B7 2B0 – 2B7 | 2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23 | Data inputs/outputs (B side) |
| $1\overline{OE}$, $2\overline{OE}$ | 48, 25 | Output enables |
| GND | 4, 10, 15, 21 28, 34, 39, 45 | Ground (0V) |
| $V_{CC}$ | 7, 18, 31, 42 | Positive supply voltage |

## FUNCTION TABLE

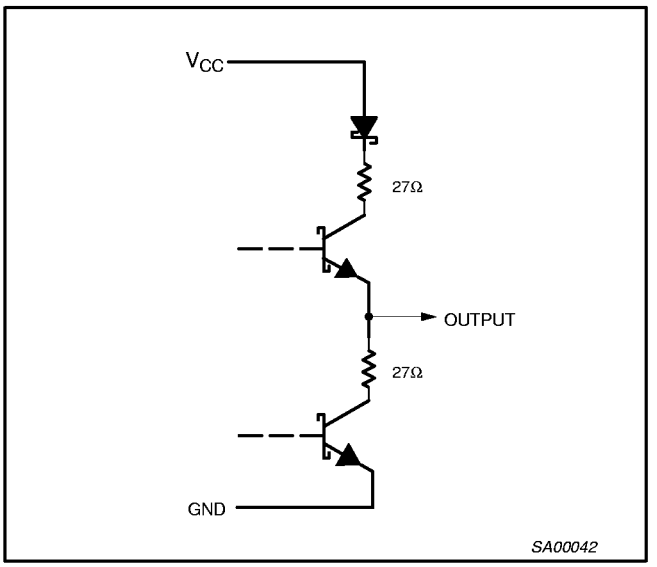
| INPUTS | | INPUTS/OUTPUTS | |
|---|---|---|---|
| $n\overline{OE}$ | nDIR | nAx | nBx |
| L | L | A = B | Inputs |
| L | H | Inputs | B = A |
| H | X | Z | Z |

H = HIGH voltage level
L = LOW voltage level
X = D0n't care
Z = High impedance "off" state

## LOGIC SYMBOL (IEEE/IEC)




## SCHEMATIC OF EACH OUTPUT



## ABSOLUTE MAXIMUM RATINGS[1, 2]

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +7.0 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –18 | mA |
| $V_I$ | DC input voltage[3] | | –1.2 to +7.0 | V |
| $I_{OK}$ | DC output diode current | $V_O < 0$ | –50 | mA |
| $V_{OUT}$ | DC output voltage[3] | output in Off or High state | –0.5 to +5.5 | V |
| $I_{OUT}$ | DC output current | output in Low state | 128 | mA |
| | | output in High state | –64 | |
| $T_{stg}$ | Storage temperature range | | –65 to 150 | °C |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | DC supply voltage | 4.5 | 5.5 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | 2.0 | | V |
| $V_{IL}$ | Low-level Input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 12 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| $T_{amb}$ | Operating free-air temperature range | –40 | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C | | | $T_{amb}$ = –40°C to +85°C | | |
| | | | Min | Typ | Max | Min | Max | |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.5V; $I_{IK}$ = –18mA | | –0.9 | –1.2 | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 4.5V; $I_{OH}$ = –3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 2.5 | 2.9 | | 2.5 | | V |
| | | $V_{CC}$ = 5.0V; $I_{OH}$ = –3mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 3.0 | 3.4 | | 3.0 | | V |
| | | $V_{CC}$ = 4.5V; $I_{OH}$ = –32mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | 2.0 | 2.4 | | 2.0 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.5V; $I_{OL}$ = 8mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 0.46 | 0.65 | | 0.65 | V |
| | Low-level output voltage | $V_{CC}$ = 4.5V; $I_{OL}$ = 12mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 0.50 | 0.80 | | 0.80 | V |
| $I_I$ | Input leakage current | $V_{CC}$ = 5.5V; $V_I$ = GND or 5.5V (Control pins) | | ±0.01 | ±1.0 | | ±1.0 | µA |
| $I_{HOLD}$ | Bus hold current A and B inputs[4] 74ABTH162245A | $V_{CC}$ = 4.5V; $V_I$ = 0.8V | 50 | | | 50 | | µA |
| | | $V_{CC}$ = 5.5V; $V_I$ = 2.0V | –75 | | | –75 | | |
| | | $V_{CC}$ = 5.5V; $V_I$ = 0 to 5.5V | ±500 | | | | | |
| $I_{OFF}$ | Power-off leakage current | $V_{CC}$ = 0.0V; $V_O$ or $V_I$ ≤ 4.5V | | ±5.0 | ±100 | | ±100 | µA |
| $I_{PU}/I_{PD}$ | Power-up/down 3-State output current[3] | $V_{CC}$ = 2.0V; $V_O$ = 0.5V; $V_I$ = GND or $V_{CC}$; $V_{OE}$ = Don't care | | ±5.0 | ±50 | | ±50 | µA |
| $I_{IH}+I_{OZH}$ | 3-State output High current | $V_{CC}$ = 5.5V; $V_O$ = 5.5V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | 0.5 | 10 | | 10 | µA |
| $I_{IL}+I_{OZL}$ | 3-State output Low current | $V_{CC}$ = 5.5V; $V_O$ = 0.0V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | –0.5 | –10 | | –10 | µA |
| $I_{CEX}$ | Output high leakage current | $V_{CC}$ = 5.5V; $V_O$ = 5.5V; $V_I$ = GND or $V_{CC}$ | | 5.0 | 50 | | 50 | µA |
| $I_O$ | Output current[1] | $V_{CC}$ = 5.5V; $V_O$ = 2.5V | –50 | –92 | –180 | –50 | –180 | mA |
| $I_{CCH}$ | Quiescent supply current | $V_{CC}$ = 5.5V; Outputs High, $V_I$ = GND or $V_{CC}$ | | 0.3 | 0.70 | | 0.70 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5V; Outputs Low, $V_I$ = GND or $V_{CC}$ | | 10 | 19 | | 19 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5V; Outputs 3-State; $V_I$ = GND or $V_{CC}$ | | 0.3 | 0.70 | | 0.70 | mA |
| $\Delta I_{CC}$ | Additional supply current per input pin[2] | Outputs enabled, one data input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5V | | 400 | 700 | | 700 | µA |
| | | Outputs 3-State, one data input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5V 74ABT162245A | | 1.0 | 50 | | 50 | µA |
| | | Outputs 3-State, one data input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5V 74ABTH162245A | | 100 | 250 | | 250 | µA |
| | | Control pins, outputs disabled, one enable input at 3.4V, other inputs at $V_{CC}$ or GND; $V_{CC}$ = 5.5V | | 400 | 700 | | 700 | µA |

**NOTES:**

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any $V_{CC}$ between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC}$ = 2.1V to $V_{CC}$ = 5 ±10% a transition time of up to 100 µsec is permitted.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.

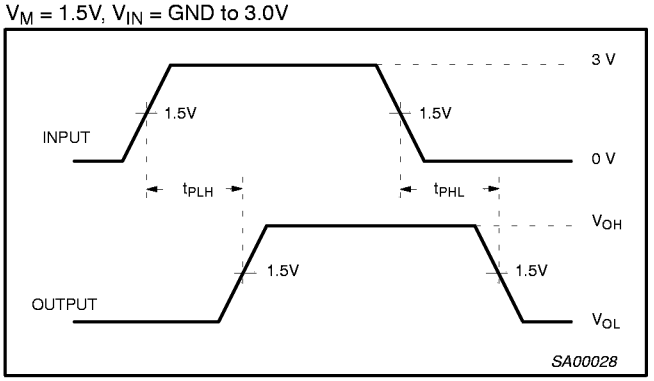
## AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; $C_L$ = 50pF, $R_L$ = 500Ω

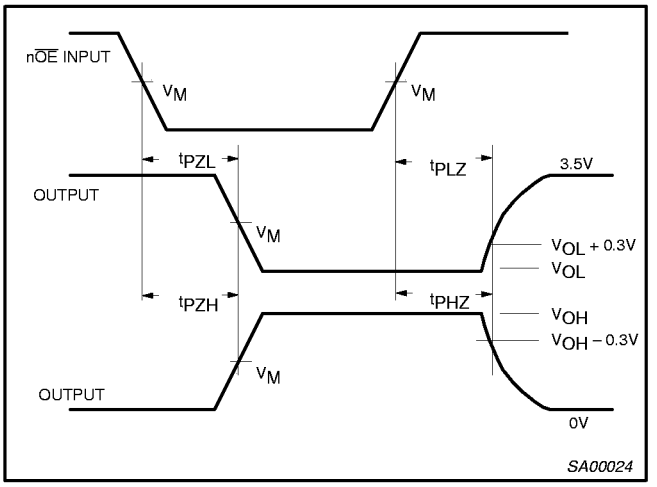
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = +5.0V | | | $T_{amb}$ = –40°C to +85°C, $V_{CC}$ = +5.0V ±0.5V | | |
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>nAx to nBx or nBx to nAx | 1 | 1.0<br>1.5 | 2.0<br>3.0 | 3.3<br>4.5 | 1.0<br>1.5 | 3.5<br>4.9 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>to High and Low level | 2 | 1.5<br>2.0 | 3.1<br>5.0 | 4.3<br>6.1 | 1.5<br>2.0 | 5.0<br>7.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>from High and Low level | 2 | 1.7<br>1.5 | 3.5<br>3.2 | 4.8<br>4.5 | 1.7<br>1.5 | 5.4<br>4.9 | ns |

## AC WAVEFORMS

$V_M$ = 1.5V, $V_{IN}$ = GND to 3.0V

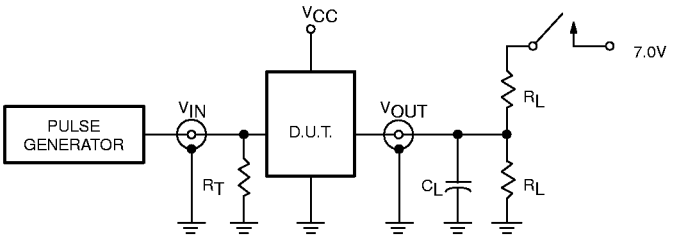



**Waveform 1. Input to Output Propagation Delays**

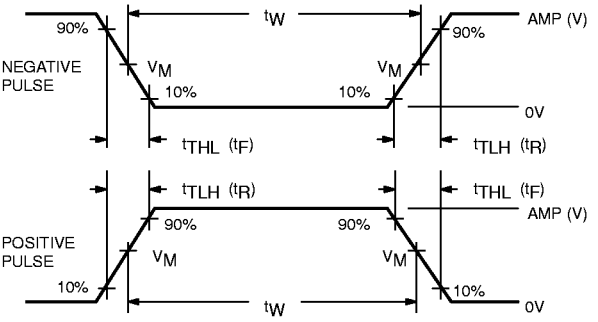



**Waveform 2. 3-State Output Enable and Disable Times**

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for 3-State Outputs**




**$V_M$ = 1.5V**
**Input Pulse Definition**

### SWITCH POSITION

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open |

### DEFINITIONS

$R_L$ = Load resistor; see AC CHARACTERISTICS for value.

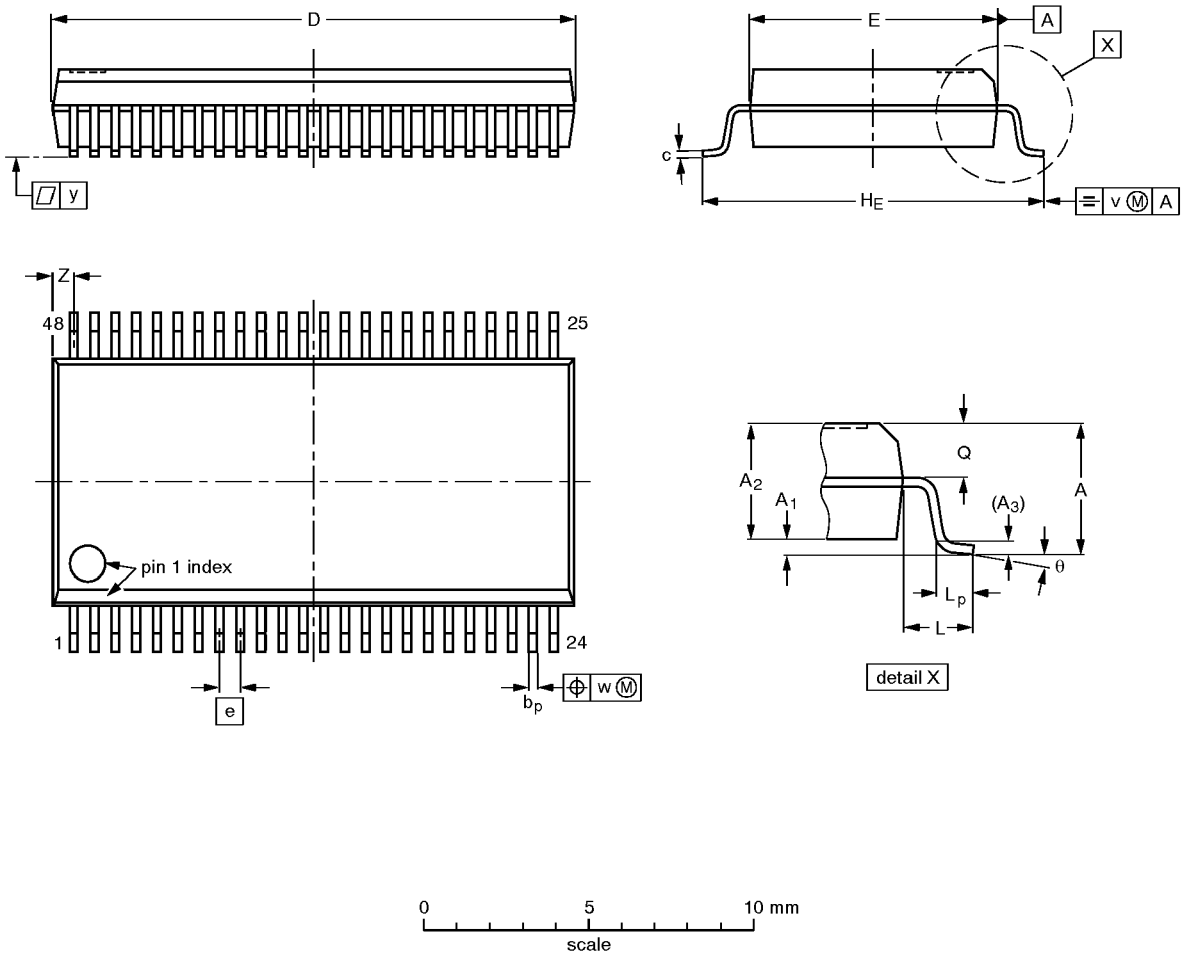
$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---|---|---|---|---|---|
| | Amplitude | Rep. Rate | $t_W$ | $t_R$ | $t_F$ |
| 74ABT/H16 | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

*SA00018*

## SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm SOT370-1




**DIMENSIONS (mm are the original dimensions)**

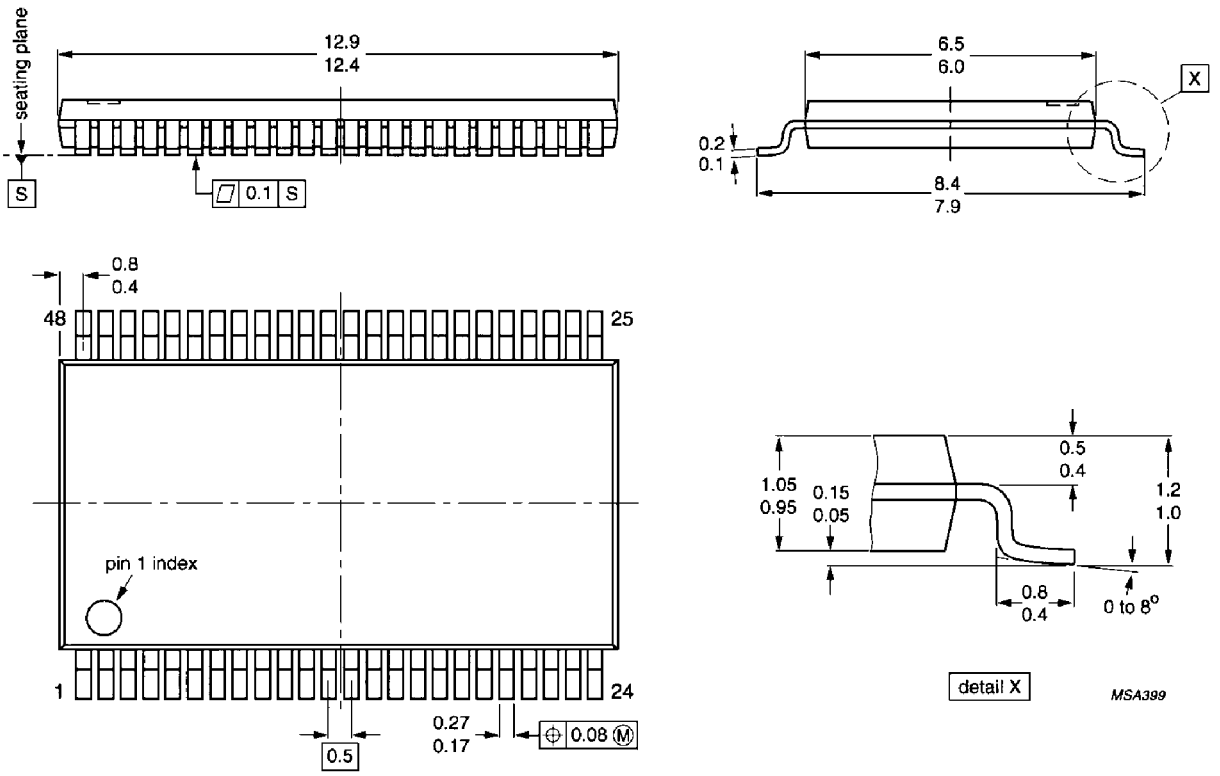
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 16.00<br>15.75 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT370-1 | | MO-118AA | | | | ~~93-11-02~~<br>95-02-04 |

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm** **SOT362-1**




Dimensions in mm.