

High Performance
128K×8
CMOS SRAM



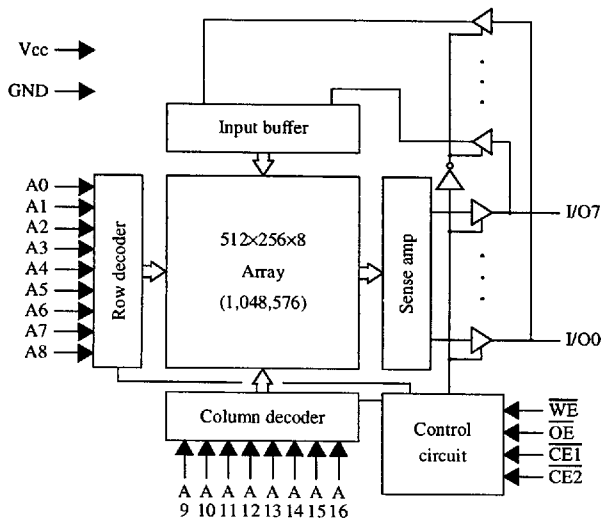
AS7C1024
AS7C1024L

128K×8 CMOS SRAM

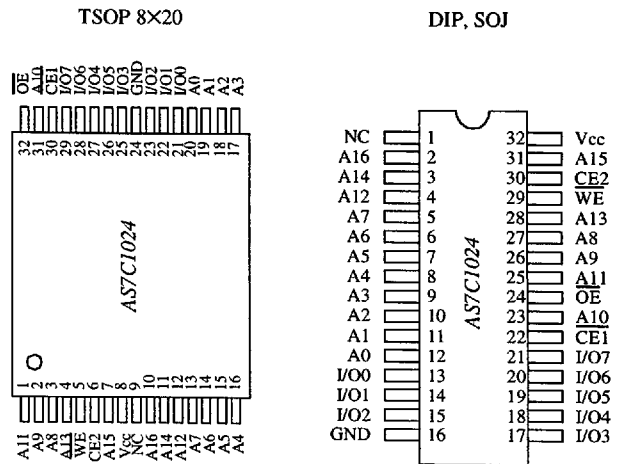
Features

- Organization: 131,072 words × 8 bits
- High speed
 - 10/12/15/20/25/35 ns address access time
 - 3/3/4/5/6/8 ns output enable access time
- Low power consumption
 - Active: 770 mW max (10 ns cycle)
 - Standby: 55 mW max, CMOS I/O
11 mW max, CMOS I/O, L version
 - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, CE2, \overline{OE} inputs
- TTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
 - 300 mil PDIP and SOJ
Socket compatible with 7C256 and 7C512
 - 400 mil PDIP and SOJ
 - 8 × 20 TSOP
- ESD protection >2000 volts
- Latch-up current > 200 mA

Logic block diagram



Pin arrangement



Selection guide

	7C1024-10	7C1024-12	7C1024-15	7C1024-20	7C1024-25	7C1024-35	Unit
Maximum address access time	10	12	15	20	25	35	ns
Maximum output enable access time	3	3	4	5	6	8	ns
Maximum operating current	140	130	120	110	100	90	mA
Maximum CMOS standby current	10.0	10.0	10.0	10.0	10.0	10.0	mA
	L	2.0	2.0	2.0	2.0	2.0	mA

Shaded areas contain advance information.

ALLIANCE SEMICONDUCTOR

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Functional description

The AS7C1024 is a high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 131,072 words \times 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 10/12/15/20/25/35 ns with output enable access times (t_{OE}) of 3/3/4/5/6/8 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, $CE2$) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CE1}$ is HIGH or $CE2$ is LOW the device enters standby mode. The standard AS7C1024 is guaranteed not to exceed 55 mW power consumption in standby mode; the L version is guaranteed not to exceed 11 mW, and typically requires only 5 mW. The L version also offers 2.0V data retention.

A write cycle is accomplished by asserting write enable (\overline{WE}) and both chip enables ($\overline{CE1}$, $CE2$). Data on the input pins I/O0-I/O7 is written on the rising edge of \overline{WE} (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or $CE2$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting output enable (\overline{OE}) and both chip enables ($\overline{CE1}$, $CE2$), with write enable (\overline{WE}) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C1024 is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_t	-0.5	+7.0	V
Power dissipation	P_D	—	1.0	W
Storage temperature (plastic)	T_{stg}	-55	+150	$^{\circ}\text{C}$
Temperature under bias	T_{bias}	-10	+85	$^{\circ}\text{C}$
DC output current	I_{out}	—	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	$CE2$	\overline{WE}	\overline{OE}	Data	Mode
H	X	X	X	High Z	Standby (I_{SB} , I_{SB1})
X	L	X	X	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

($T_a = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.2	—	$V_{CC}+1$	V
	V_{IL}	-0.5 [†]	—	0.8	V

[†] V_{IL} min = -3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics¹(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test Conditions	-10		-12		-15		-20		-25		-35		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	I _{LI}	V _{CC} = Max, V _{in} = GND to V _{CC}	-	1	-	1	-	1	-	1	-	1	-	1	μA
Output leakage current	I _{LO}	CE1 = V _{IH} or CE2 = V _{IL} , V _{CC} = Max, V _{out} = GND to V _{CC}	-	1	-	1	-	1	-	1	-	1	-	1	μA
Operating power supply current	I _{CC}	CE1 = V _{IL} , CE2 = V _{IH} , f = f _{max} , I _{out} = 0 mA	-	140	-	130	-	120	-	110	-	100	-	90	mA
			L	135	125	115	105	95	75						mA
Standby power supply current	I _{SB}	CE1 = V _{IH} or CE2 = V _{IL} , f = f _{max}	-	55	-	50	-	40	-	40	-	35	-	35	mA
			L	50	45	35	35	30	30						mA
Output voltage	V _{OL} V _{OH}	I _{OL} = 8 mA, V _{CC} = Min I _{OH} = -4 mA, V _{CC} = Min	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	V
			L	2.4	2.4	2.4	2.4	2.4	2.4						V

Shaded areas contain advance information.

Capacitance²(f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input capacitance	C _{IN}	A, CE1, CE2, WE, OE	V _{in} = 0V	5	pF
I/O capacitance	C _{I/O}	I/O	V _{in} = V _{out} = 0V	7	pF

Read cycle^{3,9,12}(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	-10		-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	10	-	12	-	15	-	20	-	25	-	35	-	ns	
Address access time	t _{AA}	-	10	-	12	-	15	-	20	-	25	-	35	ns	3
Chip enable (CE1) access time	t _{ACE1}	-	10	-	12	-	15	-	20	-	25	-	35	ns	3, 12
Chip enable (CE2) access time	t _{ACE2}	-	10	-	12	-	15	-	20	-	25	-	35	ns	3, 12
Output enable (OE) access time	t _{OE}	-	3	-	3	-	4	-	5	-	6	-	8	ns	
Output hold from address change	t _{OH}	2	-	3	-	3	-	3	-	3	-	3	-	ns	5
CE1 LOW to output in Low Z	t _{CLZ1}	3	-	3	-	3	-	3	-	3	-	3	-	ns	4, 5, 12
CE2 HIGH to output in Low Z	t _{CLZ2}	3	-	3	-	3	-	3	-	3	-	3	-	ns	4, 5, 12
CE1 HIGH to output in High Z	t _{CHZ1}	-	3	-	3	-	4	-	5	-	6	-	8	ns	4, 5, 12
CE2 LOW to output in High Z	t _{CHZ2}	-	3	-	3	-	4	-	5	-	6	-	8	ns	4, 5, 12
OE LOW to output in Low Z	t _{OLZ}	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5
OE HIGH to output in High Z	t _{OHZ}	-	3	-	3	-	4	-	5	-	6	-	8	ns	4, 5
Power up time	t _{PU}	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5, 12
Power down time	t _{PD}	-	10	-	12	-	15	-	20	-	25	-	35	ns	4, 5, 12



Key to switching waveforms

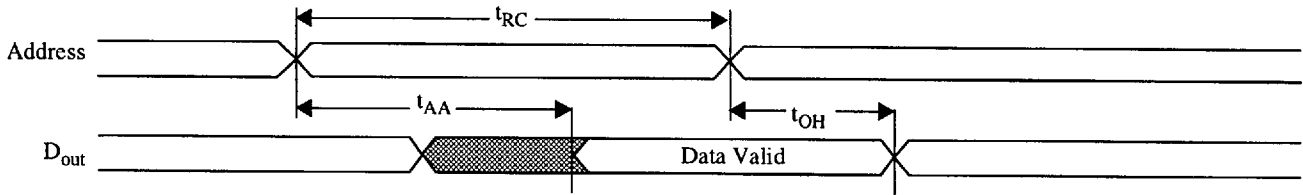
Rising input

Falling input

Undefined output/don't care

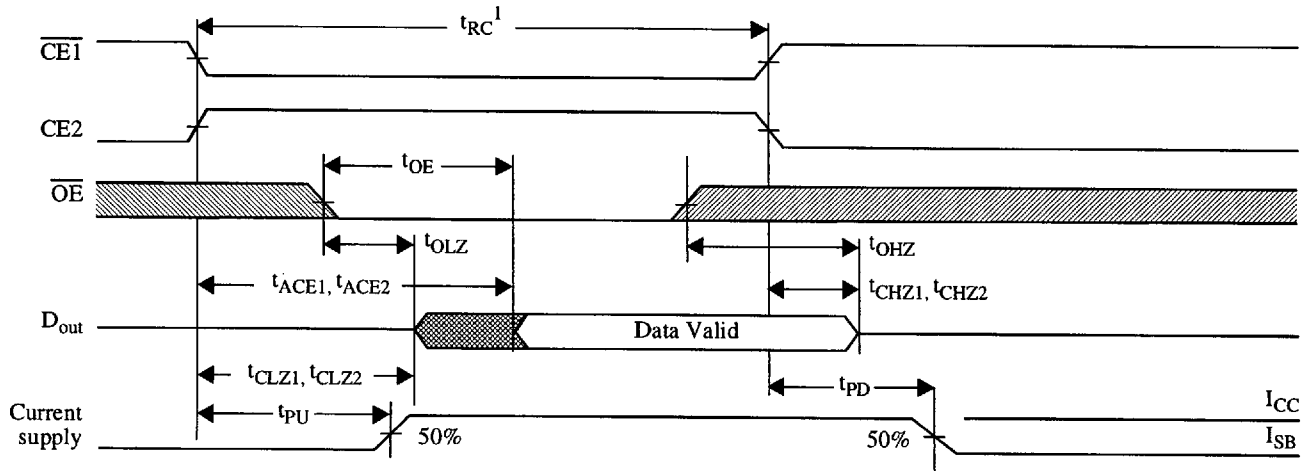
Read waveform 1^{3,6,7,9,12}

Address controlled



Read waveform 2^{3,6,8,9,12}

$\overline{CE1}$ and CE2 controlled



Write cycle^{11, 12}

($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$)

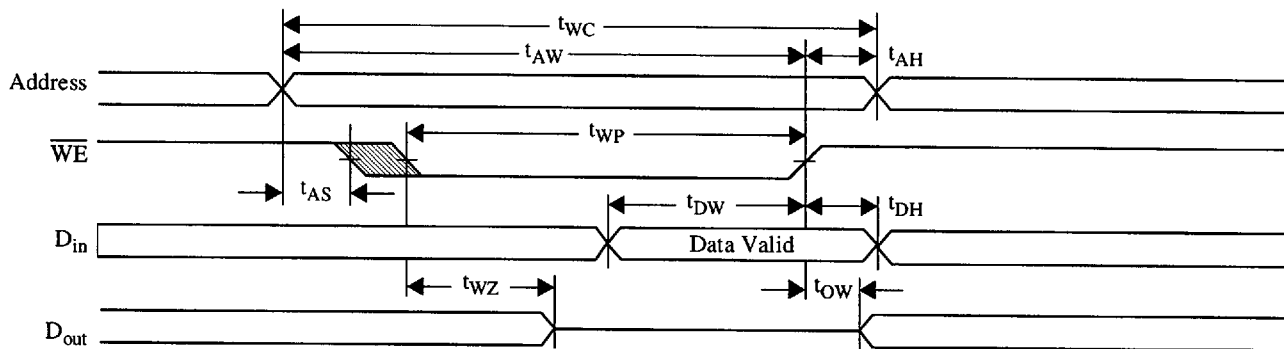
Parameter	Symbol	10		12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	—	12	—	15	—	20	—	20	—	30	—	ns	
Chip enable ($\overline{CE1}$) to write end	t_{CW1}	9	—	10	—	12	—	12	—	15	—	20	—	ns	12
Chip enable (CE2) to write end	t_{CW2}	9	—	10	—	12	—	12	—	15	—	20	—	ns	12
Address setup to write end	t_{AW}	9	—	10	—	12	—	12	—	15	—	20	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	12
Write pulse width	t_{WP}	7	—	8	—	9	—	12	—	15	—	17	—	ns	
Address hold from end of write	t_{AH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Data valid to write end	t_{DW}	6	—	6	—	9	—	10	—	10	—	12	—	ns	
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	4, 5
Write enable to output in High Z	t_{WZ}	—	5	—	5	—	5	—	5	—	5	—	5	ns	4, 5
Output active from write end	t_{OW}	3	—	3	—	3	—	3	—	3	—	3	—	ns	4, 5

Shaded areas contain advance information.



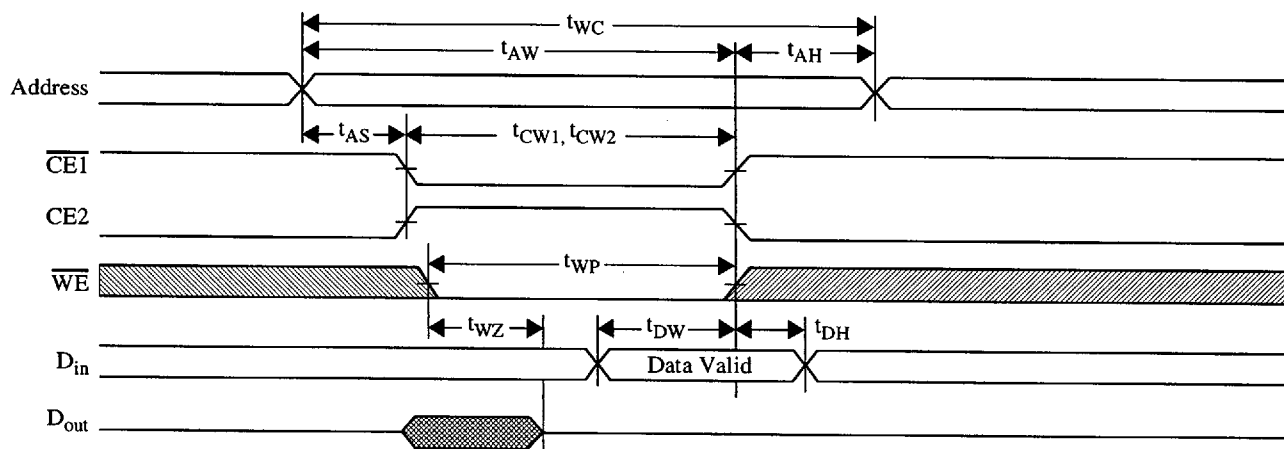
Write waveform 1^{10,11,12}

$\overline{\text{WE}}$ controlled



Write waveform 2^{10,11,12}

$\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ controlled



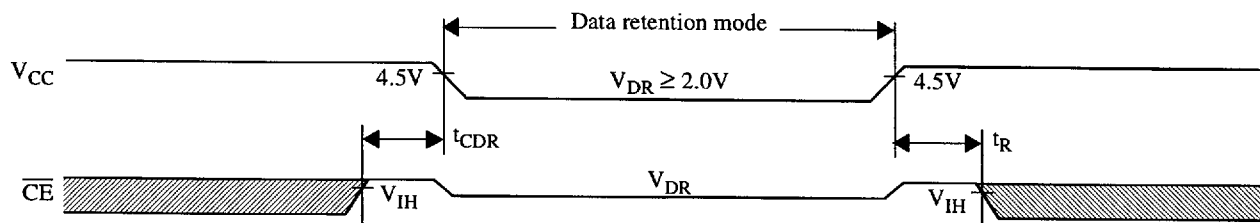
Data retention characteristics

L version only

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	$V_{CC} = 2.0V$	2.0	—	V
Data retention current	I_{CCDR}	$\overline{\text{CE1}} \geq V_{CC} - 0.2V$ or $\overline{\text{CE2}} \leq 0.2V$	—	500	μA
Chip deselect to data retention time	t_{CDR}		0	—	ns
Operation recovery time	t_R	$V_{in} \geq V_{CC} - 0.2V$ or $V_{in} \leq 0.2V$	t_{RC}	—	ns
Input leakage current	$ I_{LI} $		—	1	μA

Data retention waveform

L version only





AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

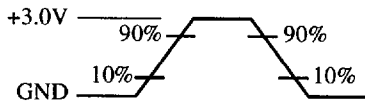


Figure A: Input waveform

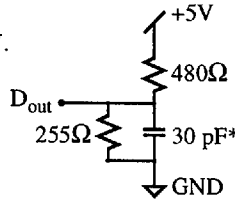


Figure B: Output load

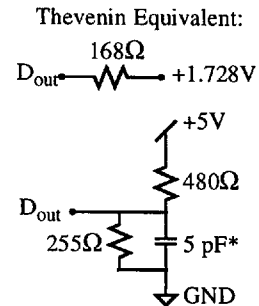


Figure C: Output load for t_{CLZ} , t_{CHZ}

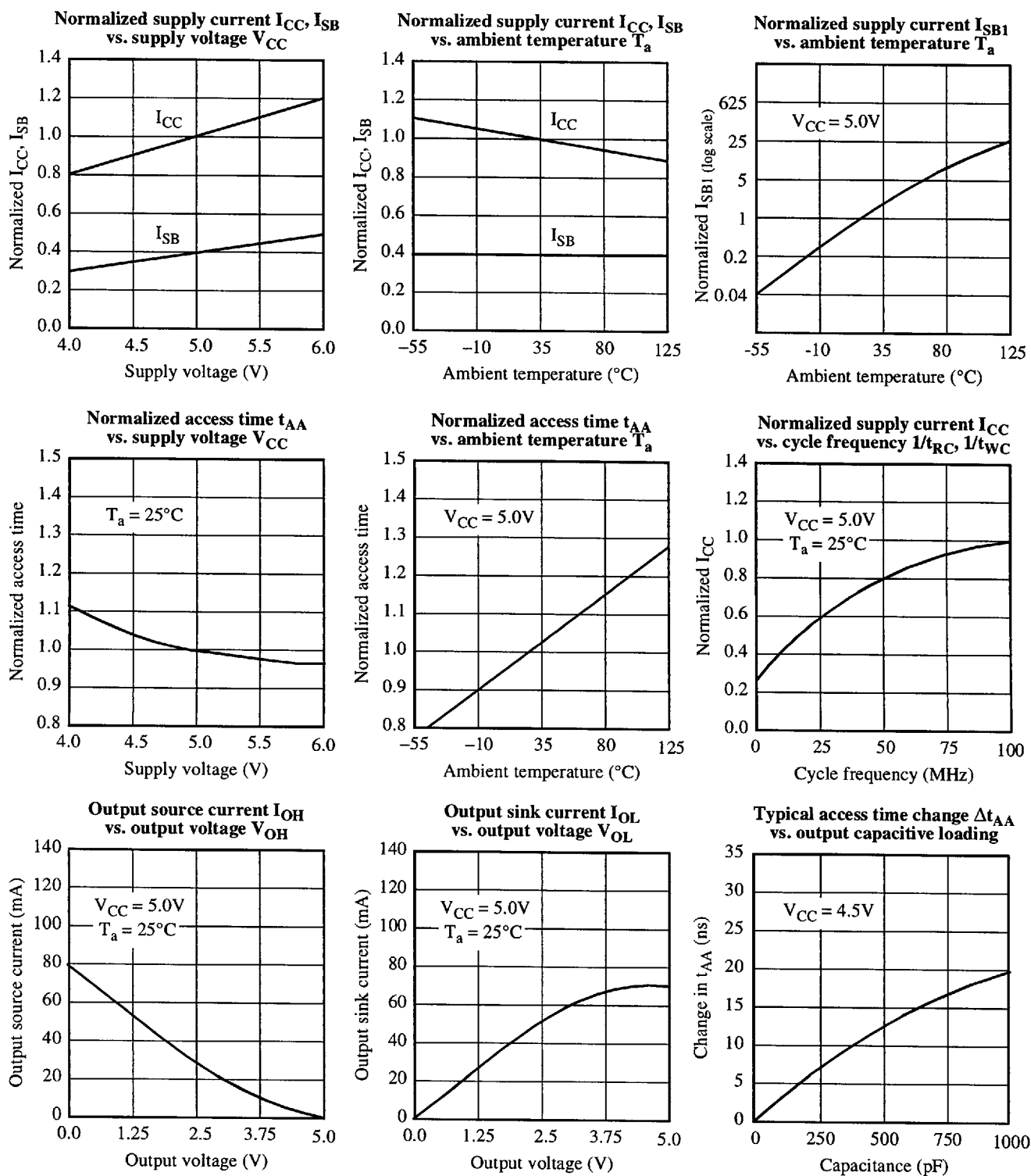
*including scope and jig capacitance

Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
- 2 This parameter is sampled and not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A, B, C.
- 4 t_{CLZ} and t_{CHZ} are specified with $CL = 5pF$ as in Figure C. Transition is measured $\pm 500mV$ from steady-state voltage.
- 5 This parameter is guaranteed but not tested.
- 6 \overline{WE} is HIGH for read cycle.
- 7 $\overline{CE1}$ and \overline{OE} are LOW and $CE2$ is HIGH for read cycle.
- 8 Address valid prior to or coincident with \overline{CE} transition LOW.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 $\overline{CE1}$ or \overline{WE} must be HIGH or $CE2$ LOW during address transitions.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 $\overline{CE1}$ and $CE2$ have identical timing.



Typical DC and AC characteristics





Ordering codes

Package \ Access Time	10 ns	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C1024-10TPC	AS7C1024-12TPC	AS7C1024-15TPC	AS7C1024-20TPC	AS7C1024-25TPC	AS7C1024-35TPC
	AS7C1024L-10TPC	AS7C1024L-12TPC	AS7C1024L-15TPC	AS7C1024L-20TPC	AS7C1024L-25TPC	AS7C1024L-35TPC
Plastic DIP, 400 mil	AS7C1024-10PC	AS7C1024-12PC	AS7C1024-15PC	AS7C1024-20PC	AS7C1024-25PC	AS7C1024-35PC
	AS7C1024L-10PC	AS7C1024L-12PC	AS7C1024L-15PC	AS7C1024L-20PC	AS7C1024L-25PC	AS7C1024L-35PC
Plastic SOJ, 300 mil	AS7C1024-10TJC	AS7C1024-12TJC	AS7C1024-15TJC	AS7C1024-20TJC	AS7C1024-25TJC	AS7C1024-35TJC
	AS7C1024L-10TJC	AS7C1024L-12TJC	AS7C1024L-15TJC	AS7C1024L-20TJC	AS7C1024L-25TJC	AS7C1024L-35TJC
Plastic SOJ, 400 mil	AS7C1024-10JC	AS7C1024-12JC	AS7C1024-15JC	AS7C1024-20JC	AS7C1024-25JC	AS7C1024-35JC
	AS7C1024L-10JC	AS7C1024L-12JC	AS7C1024L-15JC	AS7C1024L-20JC	AS7C1024L-25JC	AS7C1024L-35JC
TSOP 8x20	AS7C1024-10TC	AS7C1024-12TC	AS7C1024-15TC	AS7C1024-20TC	AS7C1024-25TC	AS7C1024-35TC
	AS7C1024L-10TC	AS7C1024L-12TC	AS7C1024L-15TC	AS7C1024L-20TC	AS7C1024L-25TC	AS7C1024L-35TC

Shaded areas contain advance information.

Part numbering system

AS7C	1024	X	Blank	Standard Power	Access Time	Package Size	Temperature Range
SRAM Prefix	Device Number	Blank	= Standard Power	Access Time	Package Size	Temperature Range	
ALABAMA	(816) 358-8100		= Low Power	Access Time	Package Size	Temperature Range	
Concord Component	(205) 772-8883			Access Time	Package Size	Temperature Range	

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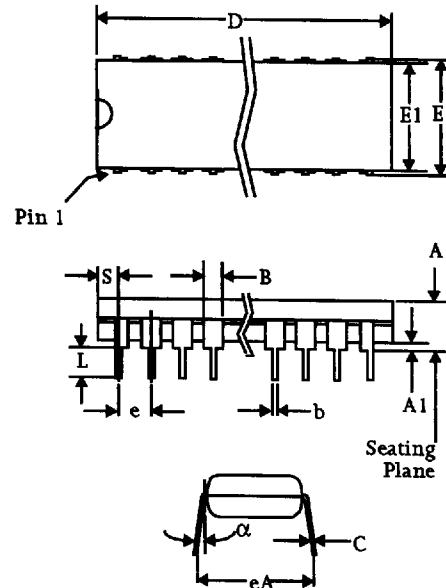
8



Plastic dual in-line package (PDIP)

	20-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.175	-	0.175	-	0.180	-	0.200
A1	0.010	-	0.010	-	0.015	-	0.015	-
B	0.046	0.054	0.058	0.064	0.045	0.055	0.045	0.065
b	0.018	0.024	0.016	0.022	0.015	0.021	0.014	0.022
C	0.008	0.014	0.008	0.014	0.008	0.012	0.009	0.015
D	-	0.980	-	1.400	-	1.571	-	1.620
E	0.290	0.310	0.295	0.320	0.300	0.325	0.390	0.425
E1	0.263	0.293	0.278	0.298	0.280	0.295	0.340	0.390
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
eA	0.310	0.350	0.330	0.370	0.330	0.370	0.430	0.470
L	0.110	0.130	0.120	0.140	0.110	0.142	0.118	0.162
α	0°	15°	0°	15°	0°	15°	0°	15°
S	-	0.040	-	0.055	-	0.043	-	0.065

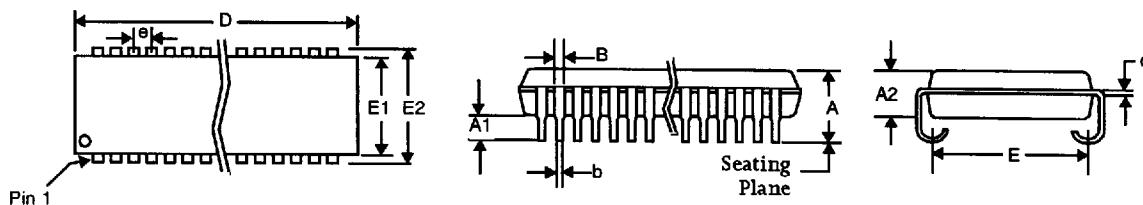
Dimensions in inches



Plastic small outline J-bend (SOJ)

	20/26-pin 300 mil		28-pin 300 mil		32-pin 300 mil		28-pin 400 mil		32-pin 400 mil		36-pin 400 mil		40-pin 400 mil		42-pin 400 mil		44-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.140	-	0.140	-	0.145	0.132	0.146	-	0.145	-	-	-	0.145	0.128	0.148	0.128	0.148
A1	0.020	-	0.025	-	0.025	-	0.062	-	0.025	-	-	-	0.025	-	0.025	-	0.025	-
A2	0.095	0.105	0.095	0.105	0.086	0.105	0.105	115	0.086	0.115	0.102 NOM		0.086	0.115	1.105	1.115	1.105	1.115
B	0.025	0.032	0.028 TYP		0.026	0.032	0.024	0.032	0.026	0.032	-	0.032	0.026	0.032	0.026	0.032	0.026	0.032
b	0.016	0.022	0.018 TYP		0.014	0.020	0.013	0.021	0.015	0.020	0.013	0.021	0.015	0.022	0.015	0.020	0.015	0.020
c	0.008	0.014	0.010 TYP		0.006	0.013	0.005	0.012	0.007	0.013	-	-	0.007	0.014	0.007	0.013	0.007	0.013
D	-	0.686	-	0.730	0.820	0.830	0.720	0.729	0.820	0.830	0.920	0.930	1.015	1.035	1.070	1.080	1.120	1.130
E	0.327	0.347	0.327	0.347	0.330	0.340	0.430	0.440	0.435	0.445	0.350	0.390	0.435	0.445	0.370 NOM		0.370 NOM	
E1	0.295	0.305	0.295	0.305	0.292	0.305	0.395	0.405	0.395	0.405	0.400 NOM		0.395	0.405	0.395	0.405	0.395	0.405
E2	0.245	0.285	0.245	0.285	0.250	0.275	0.354	0.378	0.360	0.380	0.435	0.445	0.348	0.390	0.435	0.445	0.435	0.445
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.045	0.055	0.050 BSC		0.050 NOM		0.050 NOM	

Dimensions in inches



Package diagrams

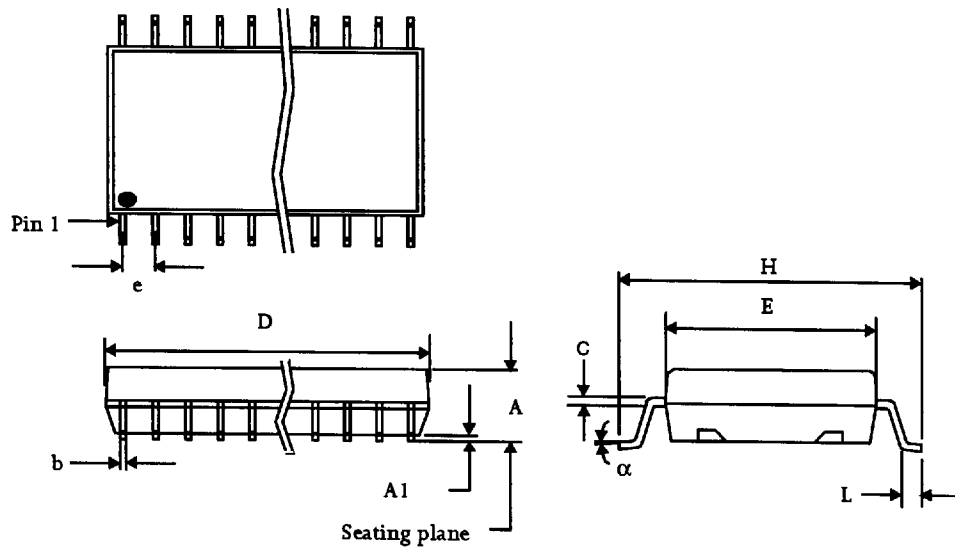


Plastic small outline gull wing IC (SOIC)

28-pin
330 mil

	Min	Max
A	-	0.112
A1	0.004	-
b	0.014	0.020
C	0.008	0.014
D	-	0.733
e	0.050 nominal	
E	0.326	0.336
H	0.453	0.477
L	0.028	0.044
α	0°	10°

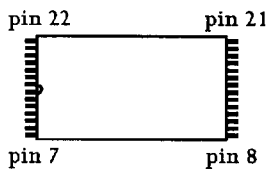
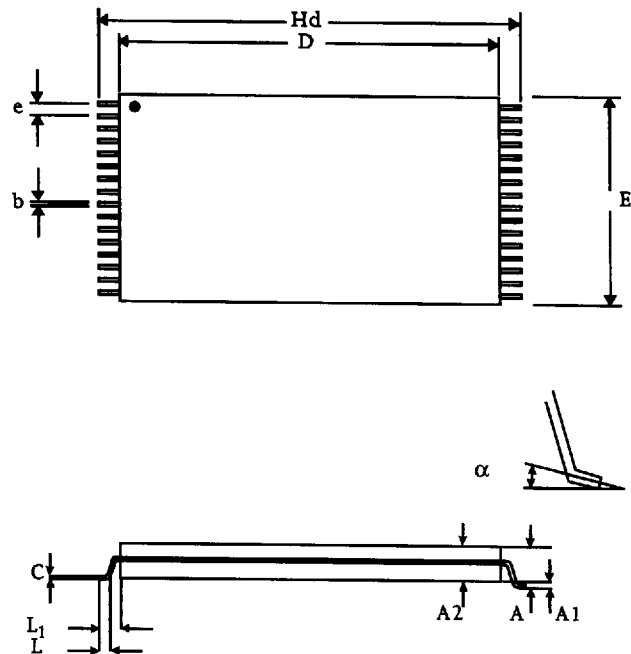
Dimensions in inches



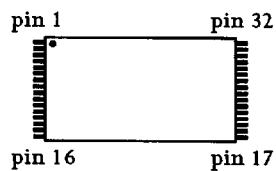
Thin small outline package (TSOP-I)

	28-pin 8x13.4		32-pin 8x20		40-pin 10x20	
	Min	Max	Min	Max	Min	Max
A	-	1.20	-	1.20	-	1.20
A1	0.05	0.15	0.05	0.15	0.05	0.15
A2	0.90	1.05	0.90	1.05	0.95	1.05
b	0.17	0.27	0.17	0.23	0.17	0.27
C	0.10	-	0.10	-	0.10	0.20
D	11.70	11.90	18.20	18.60	18.30	18.50
e	0.55 nominal		0.50 nominal		0.50 nominal	
E	8.0 nominal		7.80	8.20	9.90	10.10
Hd	13.20	13.60	19.80	20.20	19.80	20.20
L	0.30	0.70	0.40	0.60	0.50	0.70
α	0°	5°	1°	5°	0°	5°

Dimensions in millimeters



28-pin



32-pin