CSC™ CHERRY SEMICONDUCTOR

CS-2841B

CURRENT MODE PWM CONTROL CIRCUIT

DESCRIPTION

The CS-2841B provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

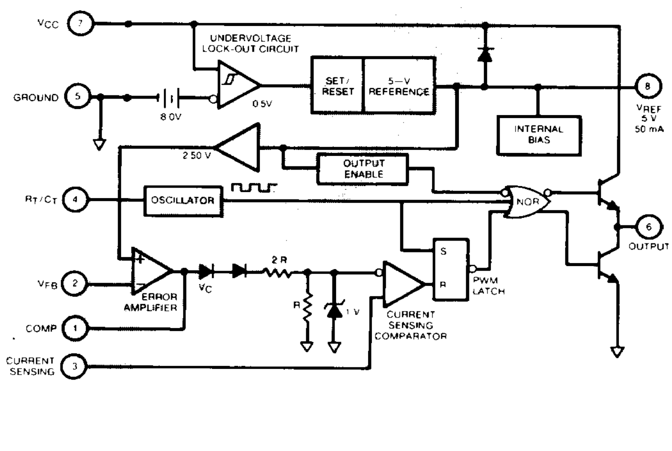
The CS-2841B is a variation of the CS-2843A designed specifically for use in automotive operation. The low start threshold voltage of typically 8.0V, and the ability to survive 42 volt automotive load dump transients are important for automotive subsystem designs. The CS-2841 series has a history of quality and reliability in automotive applications.

The CS-2841B incorporates a precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty-cycle clamp eliminates any need for an external oscillator when at, or near, a 50% duty-cycle condition. Duty-cycles greater than 50% are also possible. Special logic ensures that Vref is stabilized before the output stage is enabled. Ion-implant resistors provide tighter control of under-voltage lockout.

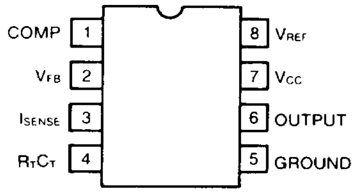
FEATURES:

- Optimized for off-line control
- Internally trimmed temperature compensated oscillator
- Maximum duty-cycle clamp
- Vref stabilized before output stage is enabled
- Low start-up current
- Pulse-by-pulse current limiting
- Improved U/V lockout
- Double pulse suppression
- 1% trimmed bandgap reference
- High current totem pole output

BLOCK DIAGRAM



PIN CONNECTIONS (TOP VIEW) DIP



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{cc}<30mA) ....Self Limiting
Supply Voltage (Low Impedence Source) 30V
Output Current ....±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pin 2, Pin 3) ....-0.3V to 5.5V
Error Amp Output Sink Current....................10mA

ELECTRICAL SPECIFICATIONS: Unless otherwise stated, specifications apply for $-40 \le T_a \le 85°C$
R_T=680Ω, C_T=.022µF for triangular mode, R_T=10K, C_T=3.3nf for sawtooth mode (see Fig. 3)

PARAMETER	TEST CONDITIONS	CS-2841B MIN.	CS-2841B TYP.	CS-2841B MAX.	UNITS
Reference Section					
Output Voltage	T_j=25°C, I_o=1mA	4.90	5.00	5.10	V
Line Regulation	$8.4 \le V_{IN} \le 16V$		6	20	mV
Load Regulation	$1 \le I_o \le 20mA$		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.82		5.18	V
Output Noise Voltage	$10Hz \le f \le 10kHz$, T_j=25°C (Note 2)		50		µV
Long Term Stability	T_A=125°C, 1000 Hrs. (Note 2)		5	25	mV
Output Short Circuit	T_A=25°C	-30	-100	-180	mA
Oscillator Section					
Initial Accuracy	Sawtooth Mode: (See Fig. 3)T_j=25°C	47	52	57	kHz
	Sawtooth Mode: $-40°C \le T_a \le +85°$	44	52	60	kHz
	Triangular Mode (see Fig. 3), T_j=25°C	44	52	60	kHz
Voltage Stability	$8.4V \le V_{cc} \le 16V$		0.2	1	%
Temp. Stability	Sawtooth Mode $T_{MIN} \le T_A \le T_{MAX}$ (Note 2)		5		%
	Triangular Mode $T_{MIN} \le T_A \le T_{MAX}$ (Note 2)		8		%
Amplitude	V_{OSC} peak to peak		1.7		V
Discharge Current	T_j=25°C	7.4	8.3	9.2	mA
	$T_{MIN} \le Ta \le T_{MAX}$	7.2		9.4	mA
Error Amp Section					
Input Voltage	V_{COMP}=2.5V	2.42	2.50	2.58	V
Input Bias Current	V_{FB}= 0V		-0.3	-2	µA
A_{VOL}	$2 \le V_O \le 4V$	65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1		MHz
PSRR	$8.4 \le V_{CC} \le 16V$	60	70		dB
Output Sink Current	V_{FB}=2.7V, V_{COMP}=1.1V	2	6		mA
Output Source Current	V_{FB}=2.3V, V_{COMP}=5V	-0.5	-0.8		mA
V_{OUT} High	V_{FB}=2.3V, R_L=15K to ground	5	6		V
V_{OUT} Low	V_{FB}=2.7V, R_L=15K to Pin 8		0.7	1.1	V
Current Sense Section					
Gain	(Notes 3 & 4)	2.85	3	3.15	V/V
Maximum Input Signal	V_{COMP}=5V (Note 3)	0.9	1	1.1	V
PSRR	$8.4 \le V_{CC} \le 16V$ (Note 3)		70		dB
Input Bias Current	V_{SENSE}= 0V		-2	-10	µA
Delay to Output	T_j=25° (Note 2)		150	300	ns
Output Section					
Output Low Level	I_{SINK}=20mA		0.1	0.4	V
	I_{SINK}=200mA		1.5	2.2	V
Output High Level	I_{SOURCE}=20mA	13	13.5		V
	I_{SOURCE}=200mA	12	13.5		V
Rise Time	T_j=25°C, C_L=1nF (Note 2)		50	150	ns
Fall Time	T_j=25°C, C_L=1nF (Note 2)		50	150	ns
Output Leakage	V_{CC}=14V, UVLO Active, $V_{PIN\ 6}$=0		-0.01	-10	µA
Total Standby Current					
Start-Up Current			0.5	1	mA
Operating Supply Current	$V_{FB}=V_{SENSE}$=0V R_T=10K, C_T=3.3nF		11	17	mA

Notes: 1. Adjust V_{CC} above the start threshold before setting at 15V.
2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with $V_{PIN\ 2}$=0.
4. Gain defined as:

$$A=\frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}};0 \le V_{PIN\ 3} \le 0.8V.$$

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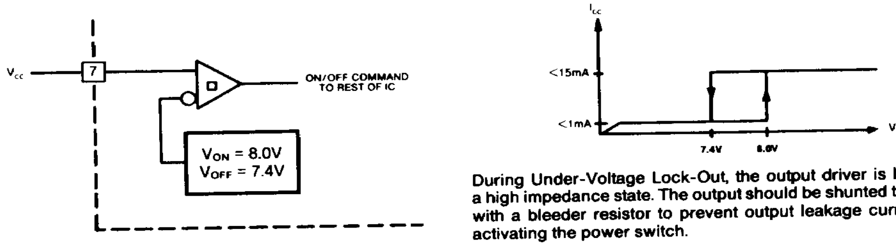
ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	CS-2841B MIN.	CS-2841B TYP.	CS-2841B MAX.	UNITS
Under-Voltage Lockout Section					
Start Threshold		7.6		8.4	V
Min. Operating Voltage	AfterTurn On	7.0		7.8	V



During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. The output should be shunted to ground with a bleeder resistor to prevent output leakage current from activating the power switch.

Fig. 1

TIMING DIAGRAM

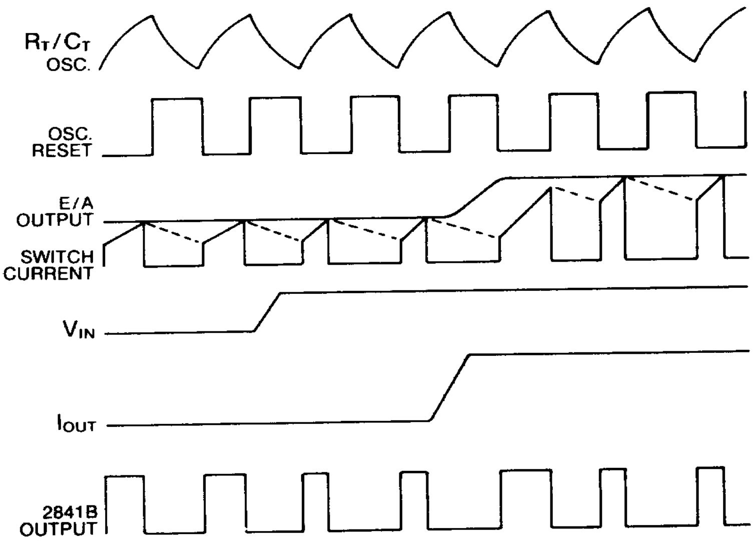


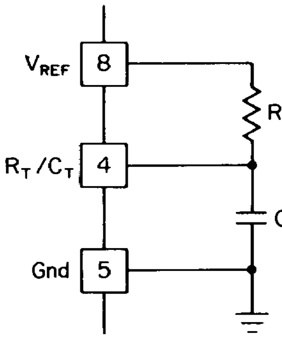
Fig. 2

NOTES ON CS-2841B TIMING DIAGRAM

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current. An increase in V_{IN} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed, to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of R_T/C_T components.

APPLICATIONS INFORMATION



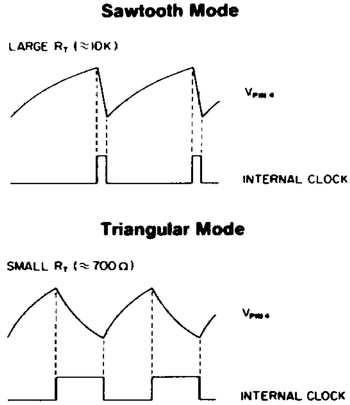
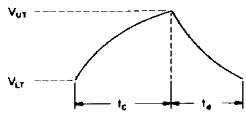


Fig. 3

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the LO state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:



$$t_c = R_T C_T \ln\left(\frac{V_{REF}-V_{LT}}{V_{REF}-V_{UT}}\right)$$

$$t_d = R_T C_T \ln\left(\frac{V_{REF}-I_d R_T-V_{UT}}{V_{REF}-I_d R_T-V_{LT}}\right)$$

Assuming typical values for the parameters in the above formulas:

V_{REF}=5.0V, V_{UT}=2.7V, V_{LT}=1.0V, I_d=8.3A, then

$t_c \approx .5534\ R_T C_T$

$$t_d \approx R_T C_T \ln\left(\frac{2.3-.0083R_T}{4.0-.0083R_T}\right)$$

The frequency and maximum duty cycle can be approximately determined from the following graphs

OSCILLATOR FREQUENCY VS. C_T

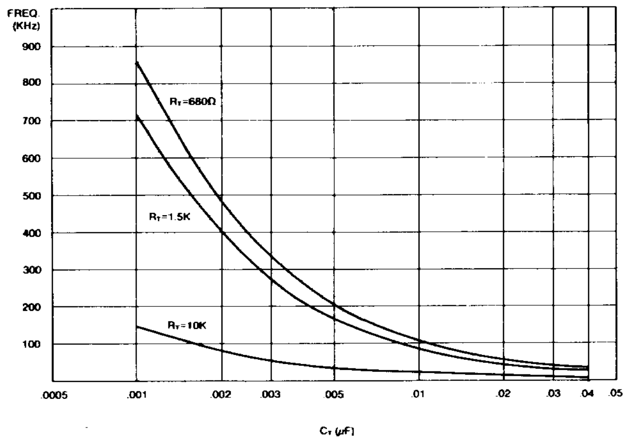


Fig. 4

OSCILLATOR DUTY CYLCLE VS. R_T

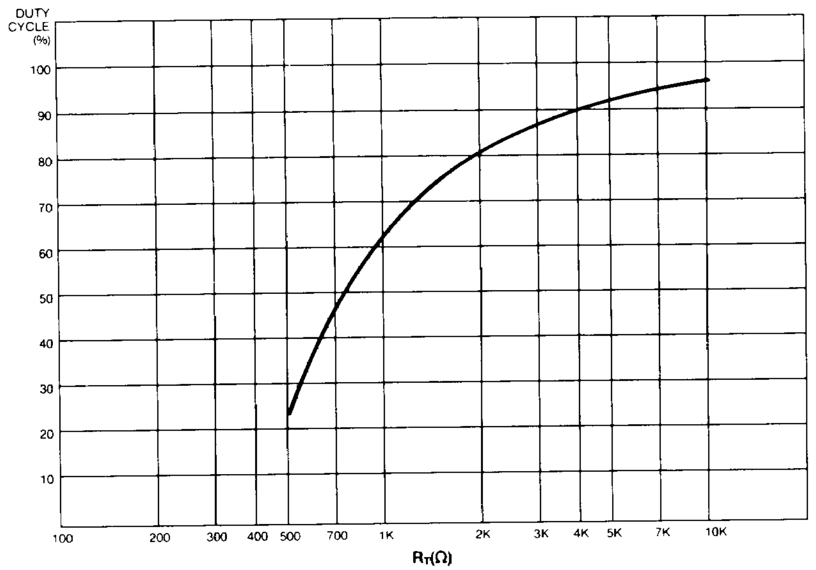
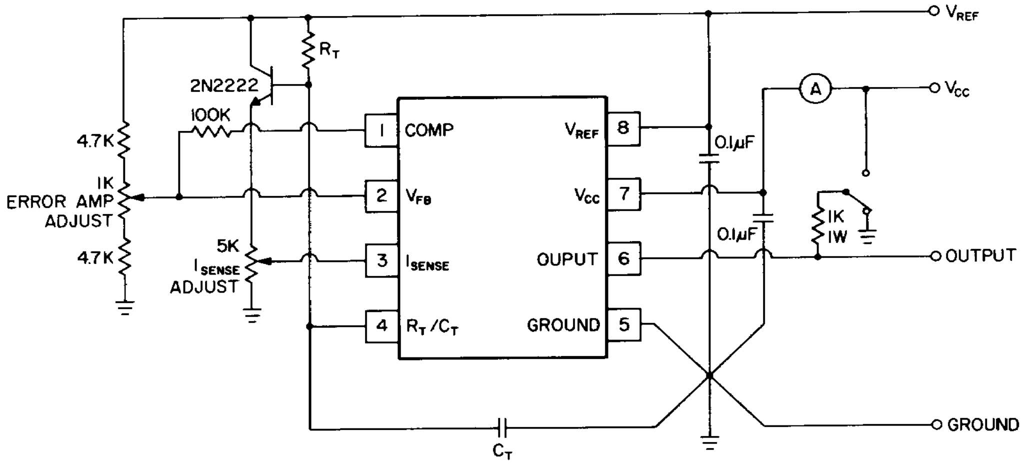


FIG. 5

OPEN-LOOP LABORATORY TEST FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

ORDERING INFORMATION

PART NUMBER	PACKAGE
CS-2841B	8L PDIP