SONY CXB1130Q/Q-Y

T-68-11-51

9, 8, Dual 4-bit Multiplexer

Description

The CXB1130Q is an ultra high speed monolithic ECL Multiplexer which functions as a 9-bit, 8-bit or dual 4-bit Parallel to Serial Converter.

The IC fetches a parallel data (D0-D8) present at the inputs and converts it into a serial data. Multiplexing is carried out in sequence from D0 to D8. S1 and S2 select a bit length.

With Load Select (LS) input set to LOW, internal load pulse loads parallel data. Start Load pulse (ST), which starts multiplexing, has to be maintaind HIGH for at least (bit length−1) clock periods.

With LS set to HIGH, External Load pulse (EL) loads parallel data. The bit length is determined by a period of EL.

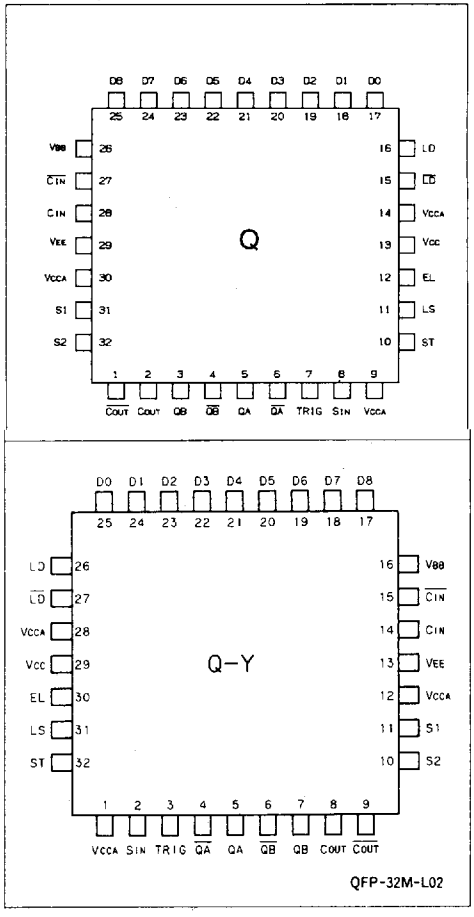
Features

- Typical clock rate up to 1.6 GHz
- Variable bit length: 9-bit, 8-bit and dual-4-bit
- Internal pull down resistors on input pins to maintain logic Low level with the pins left open
- ECL 100K compatible I/O levels

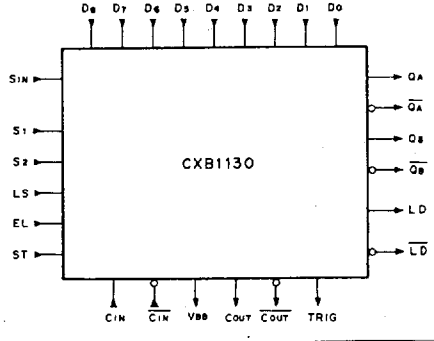
Pin Names

Dn	Parallel Data inputs
Sn	Bit length Select inputs
LS	Load Select input
ST	Load Start input
EL	External Load pulse input
SIN	Serial data input
CIN, $\overline{CIN}$	Clock inputs (positive edge trigger)
QA, $\overline{QA}$	Multiplexed serial data outputs (9, 8 and 4-bit)
QB, $\overline{QB}$	Multiplexed serial data outputs (4bit)
TRIG	Trigger pulse output
COUT, $\overline{COUT}$	Buffered Clock outputs
LD, $\overline{LD}$	Load pulse outputs
VCC	Circuit ground
VCCA	Circuit ground for outputs
VEE	Negative power supply

Pin Assignment



Logic Symbol



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DC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−190	−140	−98	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

$V_{EE}=-4.5\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item		Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time		T_{PLH}	C_{IN}	Q_A, Q_B		1000	1330	1690	ps
		T_{PHL}				1010	1350	1710	
		T_{PLH}		C_{OUT}		760	1010	1280	
		T_{PHL}				760	1010	1280	
		T_{PLH}		TRIG	ST=L	970	1290	1640	
		T_{PHL}				1100	1470	1870	
		T_{PLH}		LD	LS=L	970	1290	1640	
		T_{PHL}				1000	1330	1690	
		T_{PLH}	EL		LS=H	650	860	1090	
		T_{PHL}				660	880	1110	
Set up time		T_S	$D_n, S_{IN} \rightarrow C_{IN}$	Q_A, Q_B	LS=L	−290			
			EL, C_{IN}		LS=H	100			
Hold time		T_h	$C_{IN} \rightarrow D_n, S_{IN}$		LS=L	640			
			C_{IN}, EL		LS=H	220			
Release time		T_R	ST, C_{IN}			100			
Max. Clock frequency	9Bit	f_{MAX}	C_{IN}			1.5	1.9		GHz
	8Bit					1.3	1.6		
	4Bit					1.3	1.6		
	External					1.7	2.1		
Rise time		T_{TLH}		Q_A, Q_B, LD TRIG, C_{OUT}	20% to 80%		400	500	ps
Fall time		T_{THL}					360	460	

Note: AC test circuit; See pages 4-4 and 4-5.

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Function Table

LS	S1	S2	ST	EL	C_{IN}	Function		
L	L	L	L	×	∫	Internal Load	9bit	Load and Shift Right, D0-D8 → QA
L	L	L	H	×	∫			Initialize
L	L	H	L	×	∫		8bit	Load and Shift Right, D0-D7 → QA
L	L	H	H	×	∫			Initialize
L	H	×	L	×	∫		4bit ×2	Load and Shift Right, D0-D3 → QA, D4-D7 → QB
L	H	×	H	×	∫			Initialize
H	×	×	×	L	∫	External Load	Shift Right	≥ 9bit D0-D8 → QA; ≤ 4bit { D0-D3 → QA, D4-D7 → QB
H	×	×	×	H	∫		Load Data	

H: HIGH level voltage, L: LOW level voltage, ∫: Positve trasition edge, X: Don't care

In the External Load mode, any bit length can be selected by the period of the External Load (EL) pulse. See Timing Diagram.

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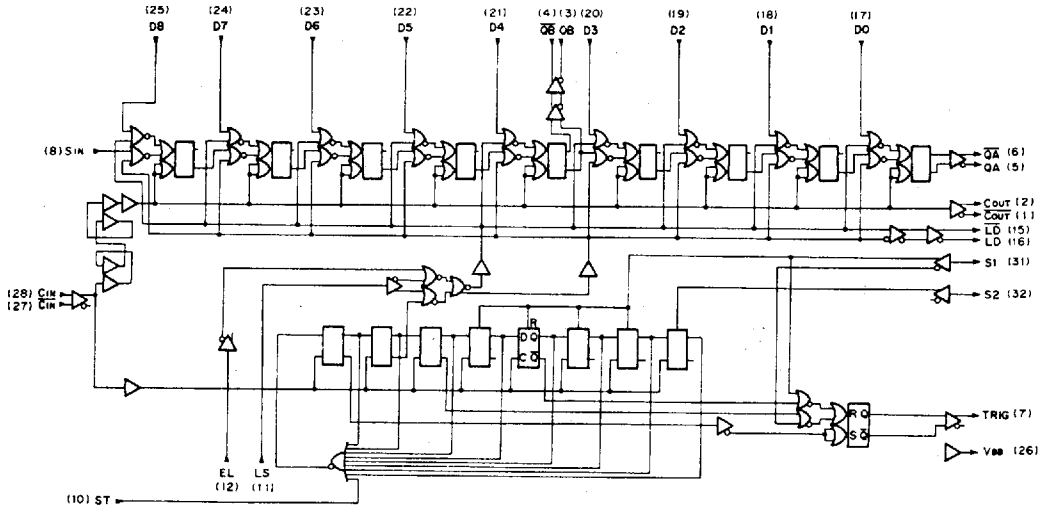
Logic Diagram



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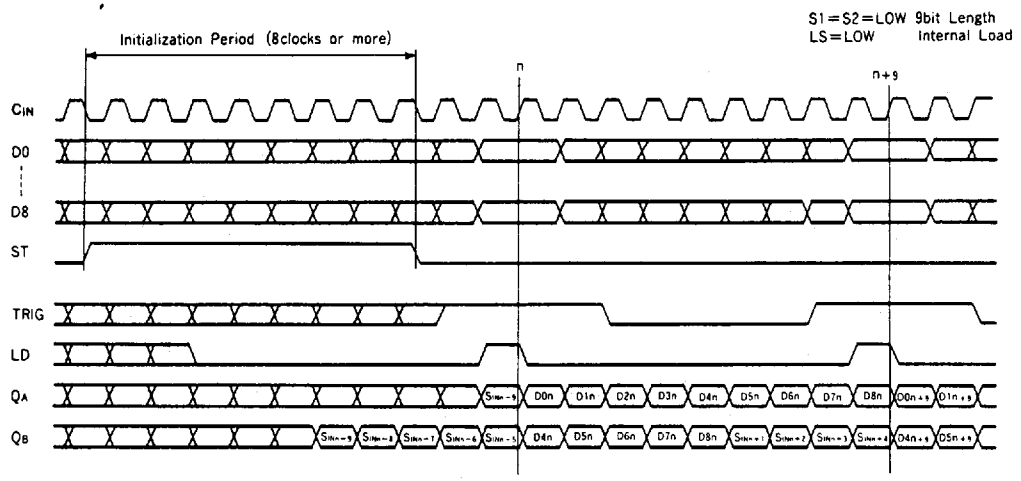
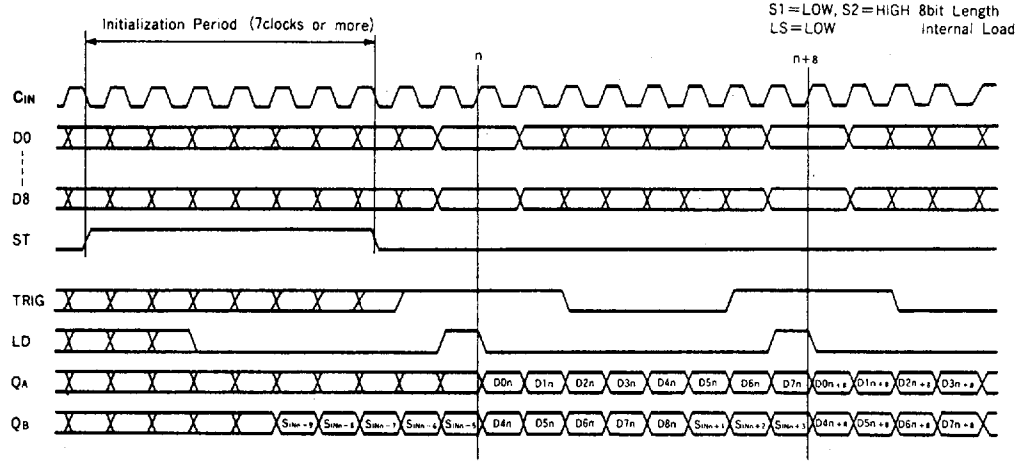
Timing Diagram—9bit



Timing Diagram—8bit



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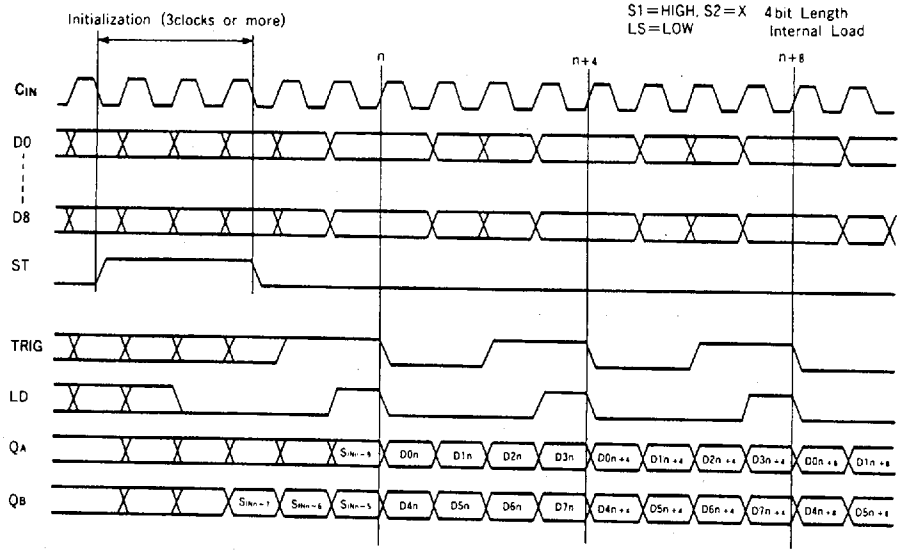
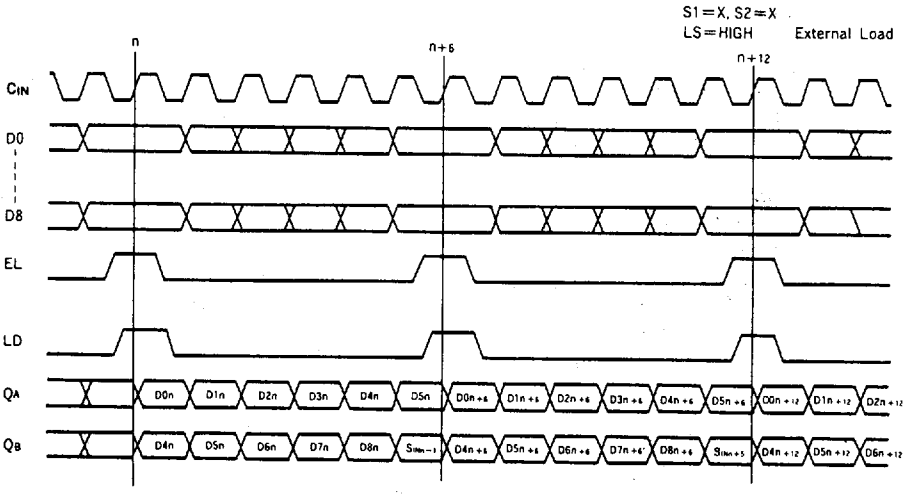
Timing Diagram—4bit×2



Timing Diagram—6bit External Load



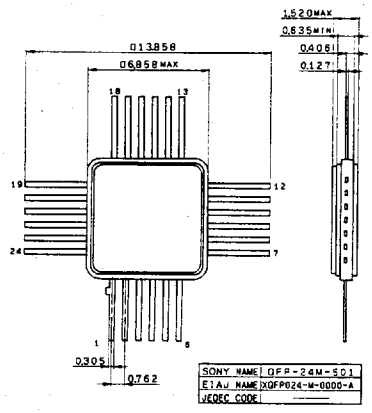
Package Data

T-90-20

Package Outline Uuit: mm

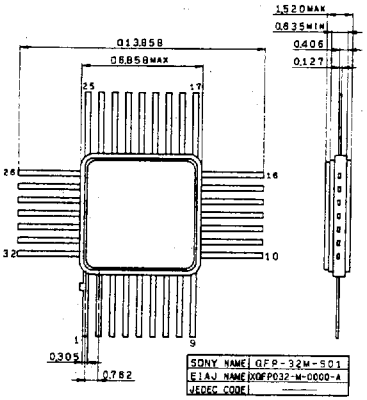
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



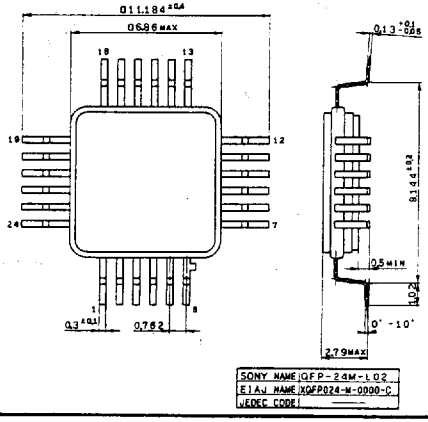
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



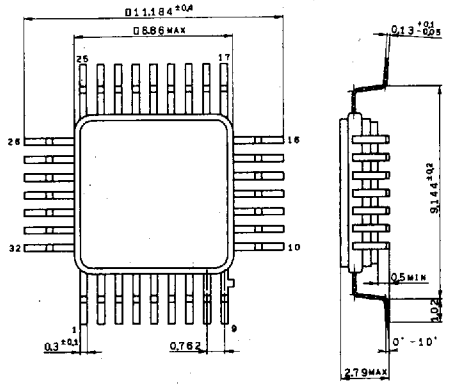
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

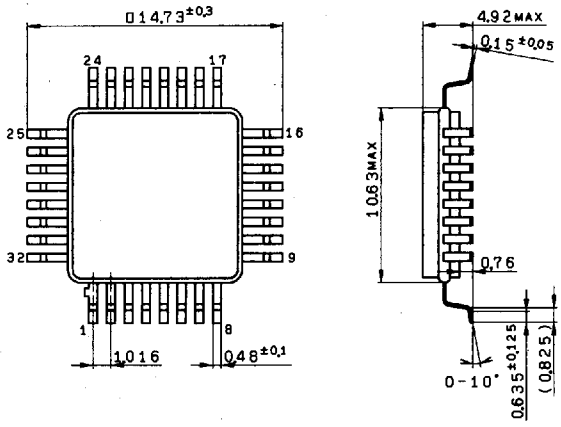
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

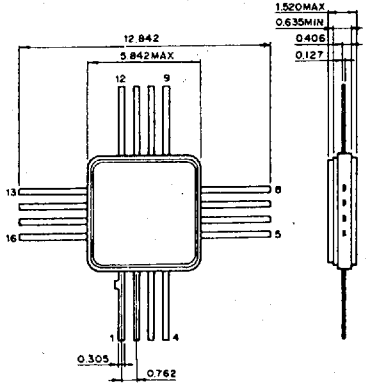
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

Package Data	Page
1. 16 pin QFP	6-3
2. 24 pin QFP	6-3
3. 32 pin QFP	6-3
4. 24 pin QFP with formed lead	6-4
5. 32 pin QFP with formed lead	6-4

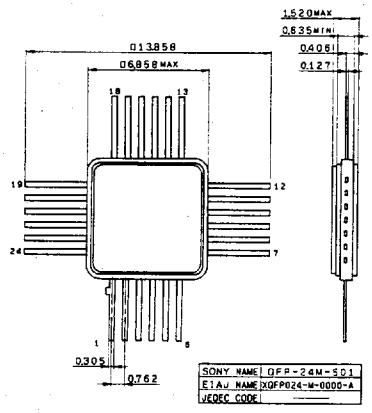
Package Data

T-90-20

Package Outline Uuit: mm

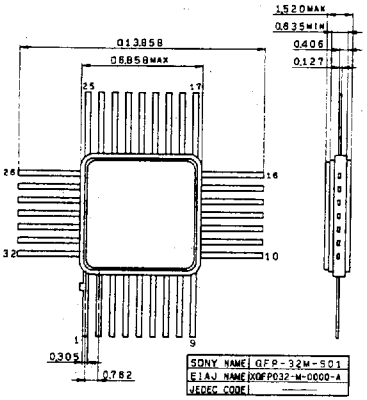
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



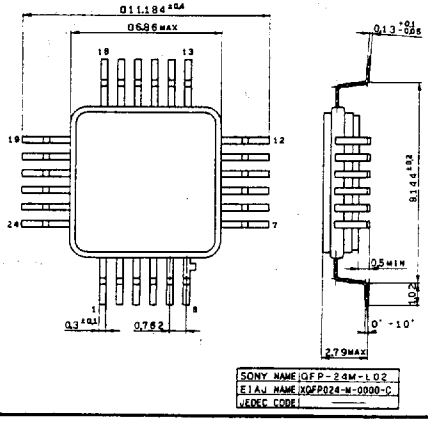
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



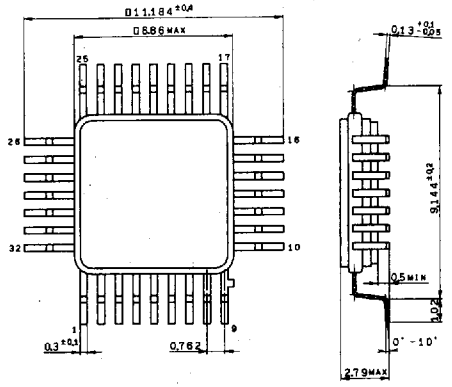
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

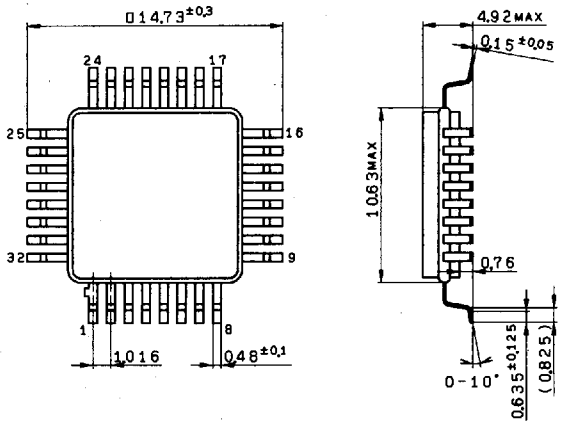
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP