SONY CXB1140Q/Q-Y

Hex 2 : 1 Multiplexer with Latch

T-68-11-51

Description

The CXB1140Q is an ultra high speed monolithic ECL IC, which contains six 2 : 1 multiplexers with transparent Latched outputs. The data select (SEL) input determines which data input is enabled. When both Latch enable (LEN1, LEN2) inputs are LOW, the Latch is transparent. The selected data is Latched on the positive transition of the Latch enable inputs. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

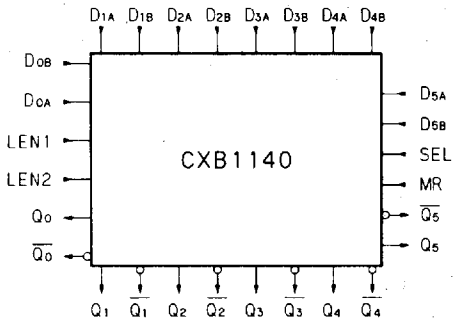
Features

- Typical propagation delay time: Tpd=780ps (Dn to Qn)
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

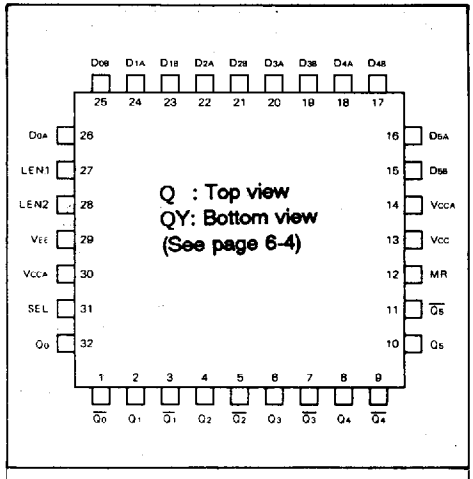
Pin Names

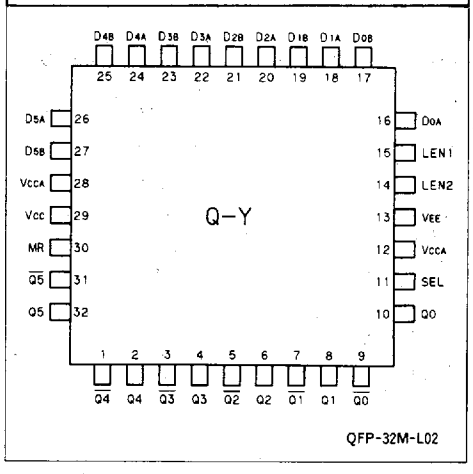
D_{nA}, D_{nB}	Data inputs
Qn, $\overline{Qn}$	Data outputs
SEL	Data Select input
LENn	Latch enable inputs
MR	Direct Master Reset input
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment





T-68-11-51

DC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−133	−98	−68	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	D_{nA}, D_{nB}	Qn	LENn=L	570	770	1000	ps
	T_{PHL}				580	780	1020	
	T_{PLH}	SEL			700	940	1220	
	T_{PHL}				720	960	1250	
	T_{PLH}	LENn			640	860	1120	
	T_{PHL}				640	860	1120	
	T_{PLH}	MR			700	930	1210	
	T_{PHL}				670	900	1170	
Gate-to-Gate skew	T_{SG-G}	D_{nA}, D_{nB}		LENn=L		60	100	
Set Up time	Ts	D, LENn			80			
		SEL, LENn			320			
Hold time	Th	LENn, D			170			
		LENn, SEL			−70			
Release time	T_R	MR, LENn			310			
Min. Pulse width	T_{PW}	MR			430			
Rise time	T_{TLH}	D_{nA}, D_{nB}		20% to 80%		290	380	
Fall time	T_{THL}					270	340	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Truth Table

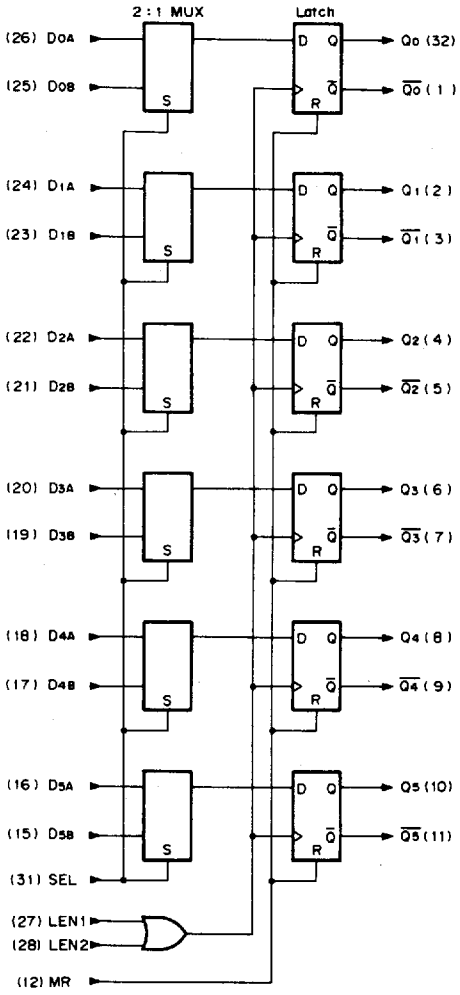
Select input	Outputs
SEL	Qn
L	D_{nA}
H	D_{nB}

Inputs		Latch
LEN1	LEN2	
L	L	Transparent
H	X	Latch
X	H	Latch

Note : H ; HIGH voltage Level
L ; LOW voltage Level
X ; Don't care

T-68-11-51

Block Diagram



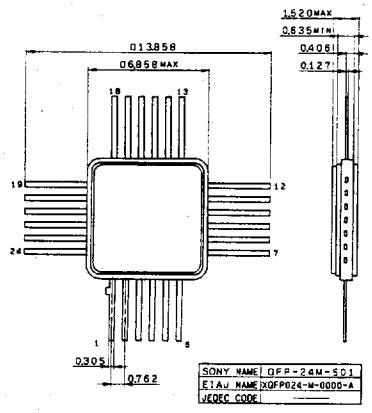
Package Data

T-90-20

Package Outline Uuit: mm

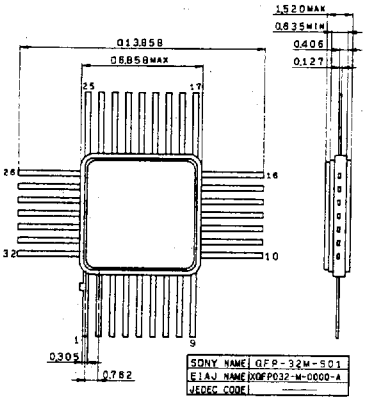
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



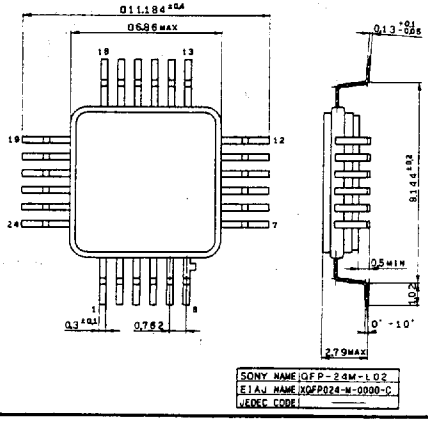
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



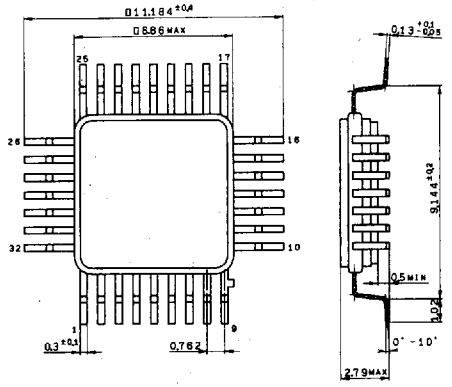
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

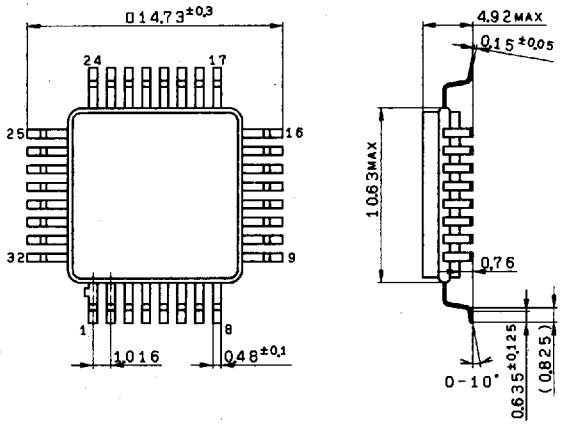
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

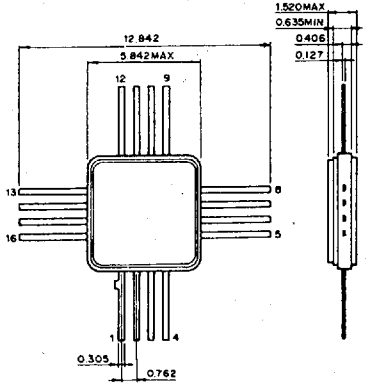
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

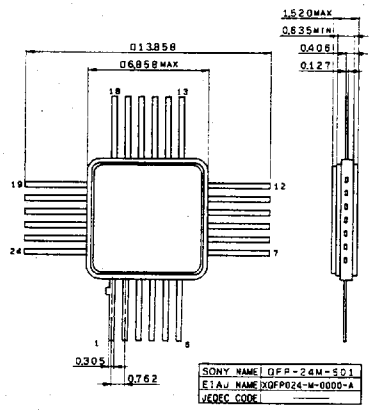
Package Data

T-90-20

Package Outline Uuit: mm

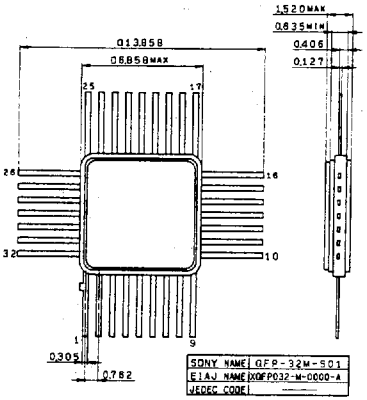
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



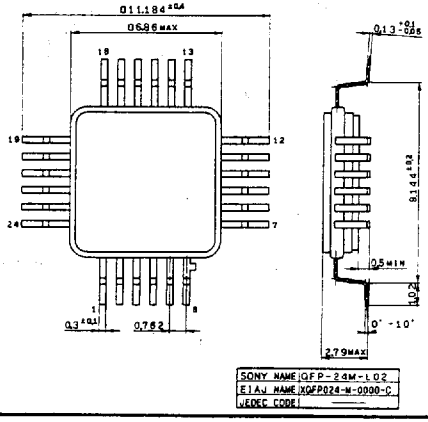
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



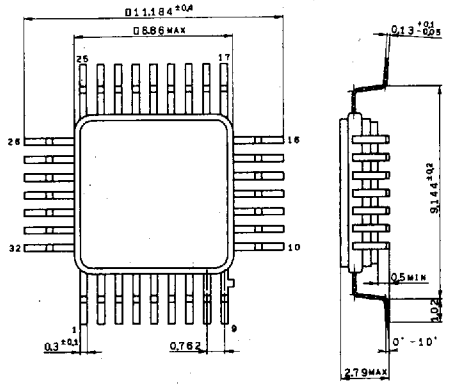
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

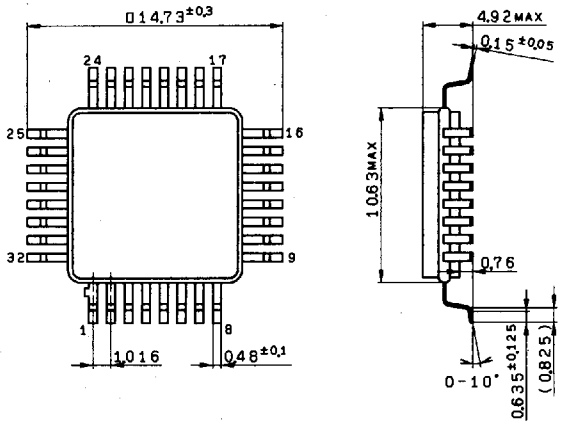
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP