



**DDR SDRAM Module 256Mbyte (32Mx72bit), based on 32Mx8, 4Banks
8K Ref., 184Pin-DIMM with PLL & Register Part No. HDD32M72D9RPW**

GENERAL DESCRIPTION

The HDD32M72D9RPW is a 32M x 72 bit Double Data Rate(DDR) Synchronous Dynamic RAM high-density memory module. The module consists of nine CMOS 32M x 8 bit with 4banks DDR SDRAMs in 66pin TSOP-II 400mil packages and 2K EEPROM in 8-pin TSSOP package on a 184-pin glass-epoxy. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The HDD32M72D9RPW is a DIMM(Dual in line Memory Module) .Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications. All module components may be powered from a single 2.5V DC power supply and all inputs and outputs are SSTL_2 compatible.

FEATURES

- Part Identification

HDD32M72D9RPW – 10A : 100MHz (CL=2)

HDD32M72D9RPW – 13A : 133MHz (CL=2)

HDD32M72D9RPW – 13B : 133MHz (CL=2.5)

- 2.5V ± 0.2V VDD and VDDQ power supply
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and /CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- The used device is 8M x 8bit x 4Banks DDR SDRAM

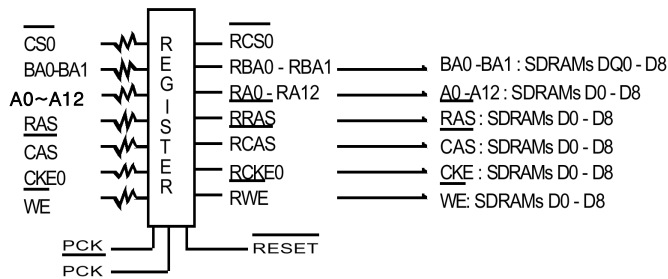
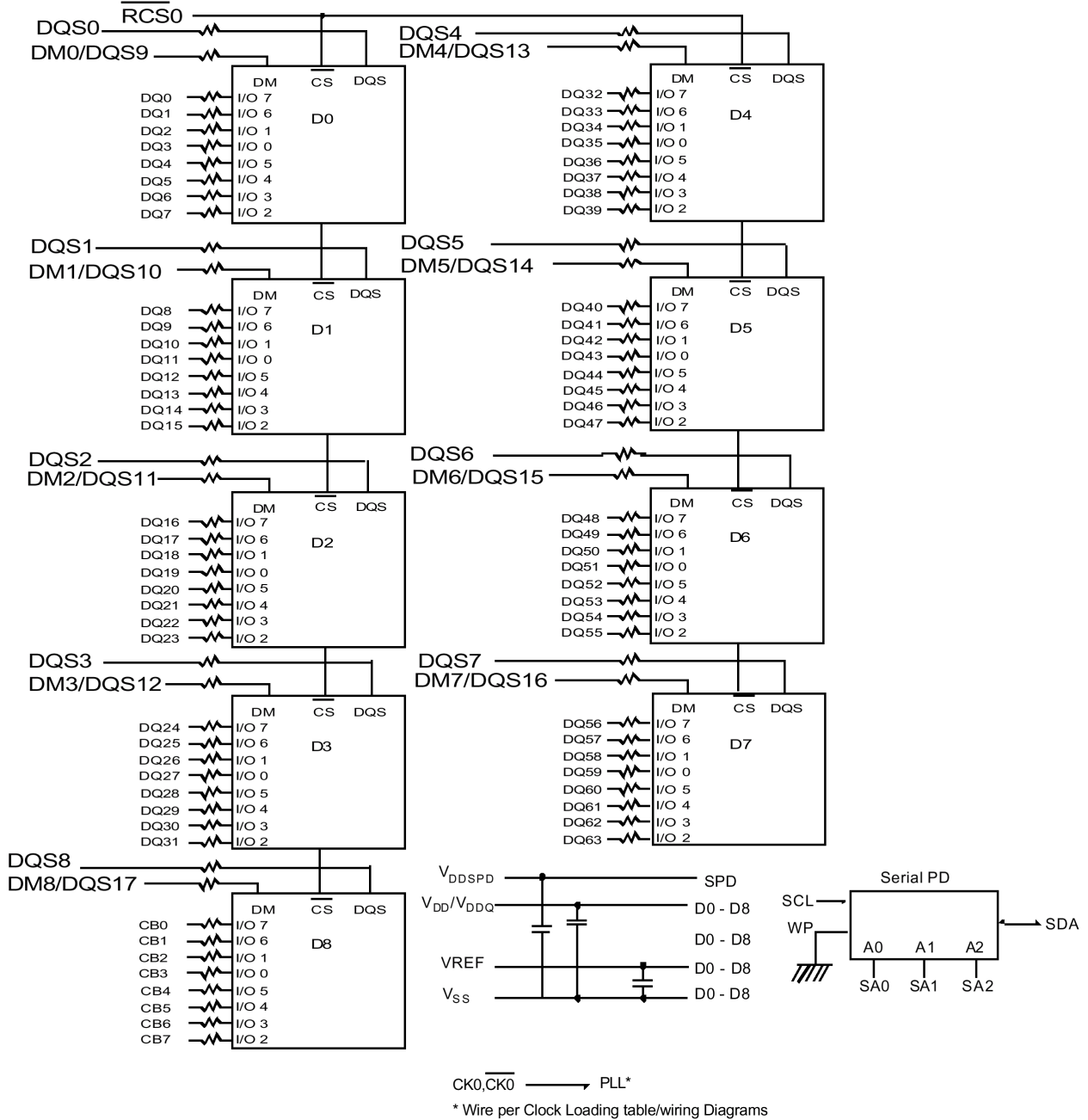
PIN ASSIGNMENT

| PIN | Front | PIN | Back | PIN | Frontl | PIN | Back | PIN | Front | PIN | Back |
|-----|--------|-----|------|-----|--------|-----|-------|-----|-------|-----|--------|
| 1 | VREF | 32 | A5 | 62 | VDDQ | 93 | Vss | 124 | Vss | 154 | /RAS |
| 2 | DQ0 | 33 | DQ24 | 63 | /WE | 94 | DQ4 | 125 | A6 | 155 | DQ45 |
| 3 | Vss | 34 | Vss | 64 | DQ41 | 95 | DQ5 | 126 | DQ28 | 156 | VDDQ |
| 4 | DQ1 | 35 | DQ25 | 65 | /CAS | 96 | VDDQ | 127 | DQ29 | 157 | /CS0 |
| 5 | DQS0 | 36 | DQS3 | 66 | Vss | 97 | DM0 | 128 | VDDQ | 158 | /CS1 |
| 6 | DQ2 | 37 | A4 | 67 | DQS5 | 98 | DQ6 | 129 | DM3 | 159 | DM5 |
| 7 | VDD | 38 | VDD | 68 | DQ42 | 99 | DQ7 | 130 | A3 | 160 | Vss |
| 8 | DQ3 | 39 | DQ26 | 69 | DQ43 | 100 | Vss | 131 | DQ30 | 161 | DQ46 |
| 9 | NC | 40 | DQ27 | 70 | VDD | 101 | NC | 132 | Vss | 162 | DQ47 |
| 10 | /RESET | 41 | A2 | 71 | * /CS2 | 102 | NC | 133 | DQ31 | 163 | * /CS3 |
| 11 | Vss | 42 | Vss | 72 | DQ48 | 103 | *A13 | 134 | CB4 | 164 | VDDQ |
| 12 | DQ8 | 43 | A1 | 73 | DQ49 | 104 | VDDQ | 135 | CB5 | 165 | DQ52 |
| 13 | DQ9 | 44 | CB0 | 74 | Vss | 105 | DQ12 | 136 | VDDQ | 166 | DQ53 |
| 14 | DQS1 | 45 | CB1 | 75 | * CK2 | 106 | DQ13 | 137 | CK0 | 167 | NC |
| 15 | VDDQ | 46 | VDD | 76 | * /CK2 | 107 | DM1 | 138 | /CK0 | 168 | VDD |
| 16 | * CK1 | 47 | DQS8 | 77 | VDDQ | 108 | VDD | 139 | Vss | 169 | DM6 |
| 17 | * /CK1 | 48 | A0 | 78 | DQS6 | 109 | DQ14 | 140 | DM8 | 170 | DQ54 |
| 18 | Vss | 49 | CB2 | 79 | DQ50 | 110 | DQ15 | 141 | A10 | 171 | DQ55 |
| 19 | DQ10 | 50 | Vss | 80 | DQ51 | 111 | CKE1 | 142 | CB6 | 172 | VDDQ |
| 20 | DQ11 | 51 | CB3 | 81 | Vss | 112 | VDDQ | 143 | VDDQ | 173 | NC |
| 21 | CKE0 | 52 | BA1 | 82 | VDDID | 113 | * BA2 | 144 | CB7 | 174 | DQ60 |
| 22 | VDDQ | KEY | | 83 | DQ56 | 114 | DQ20 | KEY | | 175 | DQ61 |
| 23 | DQ16 | 53 | DQ32 | 84 | DQ57 | 115 | A12 | 145 | Vss | 176 | Vss |
| 24 | DQ17 | 54 | VDDQ | 85 | VDD | 116 | Vss | 146 | DQ36 | 177 | DM7 |
| 25 | DQS2 | 55 | DQ33 | 86 | DQS7 | 117 | DQ21 | 147 | DQ37 | 178 | DQ62 |
| 26 | Vss | 56 | DQS4 | 87 | DQ58 | 118 | A11 | 148 | VDD | 179 | DQ63 |
| 27 | A9 | 57 | DQ34 | 88 | DQ59 | 119 | DM2 | 149 | DM4 | 180 | VDDQ |
| 28 | DQ18 | 58 | Vss | 89 | Vss | 120 | VDD | 150 | DQ38 | 181 | SA0 |
| 29 | A7 | 59 | BA0 | 90 | NC | 121 | DQ22 | 151 | DQ39 | 182 | SA1 |
| 30 | VDDQ | 60 | DQ35 | 91 | SDA | 122 | A8 | 152 | Vss | 183 | SA2 |
| 31 | DQ19 | 61 | DQ40 | 92 | SCL | 123 | DQ23 | 153 | DQ44 | 184 | VDDSPD |

*These pins should be NC in the system which does not support SPD

| PIN | PIN DESCRIPTION | PIN | PIN DESCRIPTION |
|-------------------|------------------------------|---------|---------------------------------|
| A0~A12 | Address input | VDD | Power supply(2.5V) |
| BA0~BA1 | Bank Select Address | VDDQ | Power supply for DQs(2.5V) |
| DQ0~DQ63 | Data input/output | VREF | Power supply for reference |
| CB0~CB7 | Check bit(Data input/output) | VSPD | Serial EEPROM Power supply(3.3) |
| DQS0~DQS7 | Data Strobe input/output | VSS | Ground |
| DM0~DM7 | Data-in Mask | SA0~SA2 | Address in EEPROM |
| CK0~CK2,/CK0~/CK2 | Clock input | SDA | Serial data I/O |
| CKE0 | Clock enable input | SCL | Serial clock |
| /CS0 | Chip Select input | WP | Write protection |
| /RAS | Row Address strobe | VDDIN | VDD identification flag |
| /CAS | Column Address strobe | NC | No connection |
| /RESET | Reset Enable | | |

FUNCTIONAL BLOCK DIAGRAM



- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/ \overline{CS} relationships must be maintained as shown.
 3. DQ, DQS, DM/DQS resistors: 22 Ohms.

PIN FUNCTION DESCRIPTION

| Pin | Name | Input Function |
|-----------|----------------------|---|
| CK, /CK | Clock | CK and /CK are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of CK. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/CK. |
| CKE | Clock Enable | CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN(row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognize an LVCMOS LOW level prior to VREF being stable on power-up. |
| /CS | Chip Select | /CS enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code. |
| A0 ~ A12 | Address | Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9 |
| BA0 ~ BA1 | Bank select address | BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRE-CHARGE command is being applied. |
| /RAS | Row address strobe | Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge. |
| /CAS | Columnaddress strobe | Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access. |
| /WE | Write enable | Enables write operation and row precharge. Latches data in starting from /CAS, /WE active. |
| DQS0 ~ 7 | Data Strobe | Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. |
| DM0~7 | Input Data Mask | DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS load-ing. |
| DQ0 ~ 63 | Data input/output | Data inputs/outputs are multiplexed on the same pins. |
| WP | Write Protection | WP pin is connected to Vcc. When WP is "high", EEPROM Programming will be inhibited and the entire memory will be write-protected. |
| VDDQ | Supply | DQ Power Supply : +2.5V ± 0.2V. |
| VDD | Supply | Power Supply : +2.5V ± 0.2V (device specific). |
| VSS | Supply | DQ Ground. |
| VREF | Supply | SSTL_2 reference voltage. |

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNTE |
|--|-------------------|------------|------|
| Voltage on any pin relative to Vss | V_{IN}, V_{OUT} | -0.5 ~ 3.6 | V |
| Voltage on V _{DD} supply relative to Vss | V_{DD} | -1.0 ~ 3.6 | V |
| Voltage on V _{DDQ} supply relative to Vss | V_{DDQ} | -1.0 ~ 3.6 | V |
| Storage temperature | T_{STG} | -55 ~ +150 | °C |
| Power dissipation | P_D | 13.5 | W |
| Short circuit current | I_{OS} | 50 | mA |

Notes: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C))

| PARAMETER | SYMBOL | MIN | MAX | UNIT | NOTE |
|--|---------------|------------------|------------------|------|------|
| Supply Voltage | V_{DD} | 2.3 | 2.7 | V | |
| I/O Supply Voltage | V_{DDQ} | 2.3 | 2.7 | V | |
| I/O Reference Voltage | V_{REF} | $V_{DDQ}/2-50mV$ | $V_{DDQ}/2+50mV$ | V | 1 |
| I/O Termination Voltage(system) | V_{TT} | $V_{REF} - 0.04$ | $V_{REF} + 0.04$ | V | 2 |
| Input High Voltage | $V_{IH} (DC)$ | $V_{REF} + 0.15$ | $V_{REF} + 0.3$ | V | |
| Input Low Voltage | $V_{IL} (DC)$ | -0.3 | $V_{REF} - 0.15$ | V | |
| Input Voltage Level, CK and /CK inputs | $V_{IN} (DC)$ | -0.3 | $V_{DDQ} + 0.3$ | V | |
| Input Differential Voltage, CK and /CK inputs | $V_{ID} (DC)$ | 0.3 | $V_{DDQ} + 0.6$ | V | |
| Input leakage current | I_{LI} | -2 | 2 | uA | 3 |
| Output leakage current | I_{OZ} | -5 | 5 | uA | |
| Output High current (Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$ | I_{OH} | -16.8 | | mA | |
| Output Low current (Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$ | I_{OL} | 16.8 | | mA | |
| Output High current (Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$ | I_{OH} | -9 | | mA | |
| Output Low current (Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$ | I_{OL} | 9 | | mA | |

Notes

1. Includes ± 25mV margin for DC offset on V_{REF} , and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF} , bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF} , both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of £ 3nH.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.

5. The value of V_{IX} is expected to equal $0.5 \cdot V_{DDQ}$ of the transmitting device and must track variations in the dc level of the same.

6. These characteristics obey the SSTL-2 class II standards.

INPUT/OUTPUT Capacitance (V_{DD} = 2.5V, V_{DDQ} = 2.5V, T_A = 25°C, F = 1MHZ)

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS |
|--|-------------------|-----|-----|-------|
| Input Capacitance(A0 ~ A12, BA0 ~ BA1,/RAS,/CAS,/ WE) | C _{IN1} | - | 12 | pF |
| Input Capacitance(CKE0) | C _{IN2} | - | 12 | pF |
| Input Capacitance(/CS0) | C _{IN3} | - | 11 | pF |
| Input Capacitance(CLK0,/CLK0) | C _{IN4} | - | 12 | pF |
| Data & DQS input/output Capacitance(DQ0~DQ63) | C _{OUT1} | - | 11 | PF |
| Data input/output Capacitance(CB0~CB7) | C _{OUT2} | - | 11 | PF |
| Input Capacitance(DM0~DM8) | C _{IN5} | - | 11 | pF |

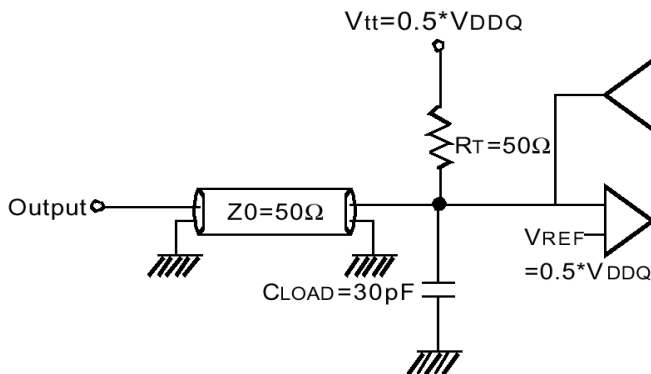
AC Operating Conditions

| PARAMETER/ Condition | STMBOL | MIN | MAX | UNIT | NOTE |
|--|----------------------|---------------------------|---------------------------|------|------|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | V _{IH} (AC) | V _{REF} + 0.31 | | | 3 |
| Input Low (Logic 0) Voltage, DQ, DQS and DM signals. | V _{IL} (AC) | | V _{REF} - 0.31 | V | 3 |
| Input Differential Voltage, CK and CK inputs | V _{ID} (AC) | 0.7 | V _{DDQ} +0.6 | V | 1 |
| Input Crossing Point Voltage, CK and CK inputs | V _{IX} (AC) | 0.5*V _{DDQ} -0.2 | 0.5*V _{DDQ} +0.2 | V | 2 |

- Note 1. V_{ID} is the magnitude of the difference between the input level on CK and the input on CK.
- Note 2. The value of V_{IX} is expected to equal 0.5* V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
- Note 3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifacitims are refation to a V_{REF} envelope that has been bandwidth limited 20MHz.

AC Operating TEST Conditions

| PARAMETER | VALUE | UNIT | NOTE |
|---|---|------|------|
| Input reference voltage for Clock | 0.5 * V _{DDQ} | V | |
| Input signal maximum peak swing | 1.5 | V | |
| Input Levels(V _{IH} /V _{IL}) | V _{REF} +0.31/V _{REF} -0.31 | V | |
| Input timing measurement reference level | V _{REF} | V | |
| Output timing measurement reference level | V _{TT} | V | |
| Output load condition | See Load Circuit | V | |



Output Load Circuit (SSTL_2)

AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)

| PARAMETER | SYMBOL | DDR200 | | DDR266A | | DDR266B | | UNIT | NOTE | |
|---|-------------|----------|------|---------|-------|---------|-------|----------|------|---|
| | | -10A | | -13A | | -13B | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| Row cycle time | t_{RC} | 70 | | 65 | | 65 | | ns | 1 | |
| Refresh row cycle time | t_{RFC} | 80 | | 75 | | 75 | | ns | 1,2 | |
| Row active time | t_{RAS} | 48 | 120K | 45 | 120K | 45 | 120K | ns | 1,2 | |
| /RAS to /CAS delay | t_{RCD} | 20 | | 20 | | 20 | | ns | 3 | |
| Row precharge time | t_{RP} | 20 | | 20 | | 20 | | ns | 3 | |
| Row active to Row active delay | t_{RRD} | 15 | | 15 | | 15 | | ns | 3 | |
| Write recovery time | t_{WR} | 15 | | 15 | | 15 | | t_{CK} | 3 | |
| Last data in to Read command | t_{CDLR} | 1 | | 1 | | 1 | | t_{CK} | 2 | |
| Col. address to Col. address delay | t_{CCD} | 1 | | 1 | | 1 | | t_{CK} | | |
| Clock cycle time | CL=2.0 | t_{CK} | 10 | 12 | 7.5 | 12 | 10 | 12 | ns | 5 |
| | CL=2.5 | | | | 7.5 | 12 | 7.5 | 12 | ns | 5 |
| Clock high level width | t_{CH} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | | |
| Clock low level width | t_{CL} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | | |
| DQS-out access time from CK/CK | t_{DQSK} | -0.8 | +0.8 | -0.75 | +0.75 | -0.75 | +0.75 | ns | | |
| Output data access time from CK/CK | t_{AC} | -0.8 | +0.8 | -0.75 | +0.75 | -0.75 | +0.75 | ns | | |
| Data strobe edge to output data edge | t_{DQSQ} | - | +0.6 | - | +0.5 | - | +0.5 | ns | 5 | |
| Read Preamble | t_{RPRE} | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | t_{CK} | | |
| Read Postamble | t_{RPST} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t_{CK} | | |
| Data out high impedance time from CK-/CK | t_{HZQ} | -0.8 | +0.8 | -0.75 | +0.75 | -0.75 | +0.75 | ns | 2 | |
| CK to valid DQS-in | t_{DQSS} | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | t_{CK} | | |
| DQS-in setup time | t_{WPRES} | 0 | | 0 | | 0 | | ns | 3 | |
| DQS-in hold time | t_{WPREH} | 0.25 | | 0.25 | | 0.25 | | t_{CK} | | |
| DQS-in falling edge to CK rising-setup time | t_{DSS} | 0.2 | | 0.2 | | 0.2 | | t_{CK} | | |
| DQS-in falling edge to CK rising hold time | t_{DSH} | 0.2 | | 0.2 | | 0.2 | | t_{CK} | | |
| DQS-in high level width | t_{DQSH} | 0.35 | | 0.35 | | 0.35 | | t_{CK} | | |
| DQS-in low level width | t_{DQSL} | 0.35 | | 0.35 | | 0.35 | | t_{CK} | | |
| DQS-in cycle time | t_{DSC} | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | t_{CK} | | |
| Address and Control Input setup time | t_{IS} | 1.1 | | 0.9 | | 0.9 | | ns | 6 | |
| Address and Control Input hold time | t_{IH} | 1.1 | | 0.9 | | 0.9 | | ns | 6 | |
| Mode register set cycle time | t_{MRD} | 16 | | 15 | | 15 | | ns | | |
| DQ & DM setup time to DQS | t_{DS} | 0.6 | | 0.5 | | 0.5 | | ns | | |
| DQ & DM hold time to DQS | t_{DH} | 0.6 | | 0.5 | | 0.5 | | ns | | |
| DQ & DM input pulse width | t_{DIPW} | 2 | | 1.75 | | 1.75 | | ns | | |
| Power down exit time | t_{PDEX} | 10 | | 7.5 | | 7.5 | | ns | | |
| Exit self refresh to write command | t_{XSW} | 116 | | 95 | | | | ns | | |
| Exit self refresh to bank active command | t_{XSA} | 80 | | 75 | | 75 | | ns | | |
| Exit self refresh to read command | t_{XSR} | 200 | | 200 | | 200 | | Cycle | | |
| Refresh interval time | t_{REF} | 7.8 | | 7.8 | | 7.8 | | us | 1 | |
| DQS write postamble time | t_{WPST} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t_{CK} | 3 | |

Notes :

1. Maximum burst refresh cycle : 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS} .
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. For registered DIMMs, t_{CL} and t_{CH} are $\geq 45\%$ of the period including both the half period jitter ($t_{JIT}(HP)$) of the PLL and the half jitter due to crosstalk ($t_{JIT}(crosstalk)$) on the DIMM.

6. Input Setup/Hold Slew Rate Derating

| Input Setup/Hold Slew Rate | Δt_{IS} | Δt_{IH} |
|----------------------------|-----------------|-----------------|
| (V/ns) | (ps) | (ps) |
| 0.5 | 0 | 0 |
| 0.4 | +50 | +50 |
| 0.3 | +100 | +100 |

- This derating table is used to increase t_{DS}/t_{DH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

| Input Setup/Hold Slew Rate | Δt_{IS} | Δt_{IH} |
|----------------------------|-----------------|-----------------|
| (V/ns) | (ps) | (ps) |
| 0.5 | 0 | 0 |
| 0.4 | +75 | +75 |
| 0.3 | +150 | +150 |

- This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

| I/O Input Level | Δt_{DS} | Δt_{DH} |
|-----------------|-----------------|-----------------|
| (mV) | (ps) | (ps) |
| ± 280 | +50 | +50 |

- This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below $V_{REF} \pm 310mV$ for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

| Delta Rise/Fall Rate | Δt_{DS} | Δt_{DH} |
|----------------------|-----------------|-----------------|
| (ns/V) | (ps) | (ps) |
| 0 | 0 | 0 |
| ± 0.25 | +50 | +50 |
| ± 0.5 | +100 | +100 |

- This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as $1/SlewRate1-1/SlewRate2$. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = $0/5ns/V$. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.
11. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is actual to the system clock cycle time.

COMMAND TRUTH TABLE (V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

| COMMAND | | CK E n-1 | CKE n | /CS | /RAS | /CAS | /WE | DM | BA 0,1 | A10/ AP | A11 A9~A0 | NOTE | |
|---------------------------------------|---------------------------|----------------|----------|-----|------|------|-----|----|-----------|-------------|--------------|--------------------------------|---|
| Register | Extended MRS | H | X | L | L | L | L | X | OP code | | | 1,2 | |
| Register | Mode register set | H | X | L | L | L | L | X | OP code | | | 1,2 | |
| Refresh | Auto refresh | | H | H | L | L | L | H | X | X | | 3 | |
| | Self refresh | Entry | | L | | | | | | | | | |
| | | Exit | L | H | L | H | H | H | X | X | | 3 | |
| | | | | | H | X | X | X | | | | 3 | |
| Bank active & Row Addr. | | H | X | L | L | H | H | X | V | Row address | | | |
| Read & column address | Auto precharge disable | | H | X | L | H | L | H | X | V | L | Column Address (A0 ~ A9) | 4 |
| | Auto precharge enable | | | | | | | | | | H | | |
| Write & column address | Auto precharge disable | | H | X | L | H | L | L | X | V | L | Column Address (A0 ~ A9) | 4 |
| | Auto precharge enable | | | | | | | | | | H | | |
| Burst Stop | | H | X | L | H | H | L | X | X | | | 7 | |
| Precharge | Bank selection | | H | X | L | L | H | L | X | V | L | X | |
| | All banks | | | | | | | | | X | H | | 5 |
| Clock suspend or active power down | Entry | H | L | H | X | X | X | X | X | | | | |
| | | | | L | V | V | V | | | | | | |
| Precharge power down mode | Entry | H | L | H | X | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | | |
| | Exit | L | H | H | X | X | X | X | | | | | |
| | | | | L | V | V | V | | | | | | |
| DM | | H | X | | | | | V | X | | 8 | | |
| No operation command | | H | X | H | X | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | | |

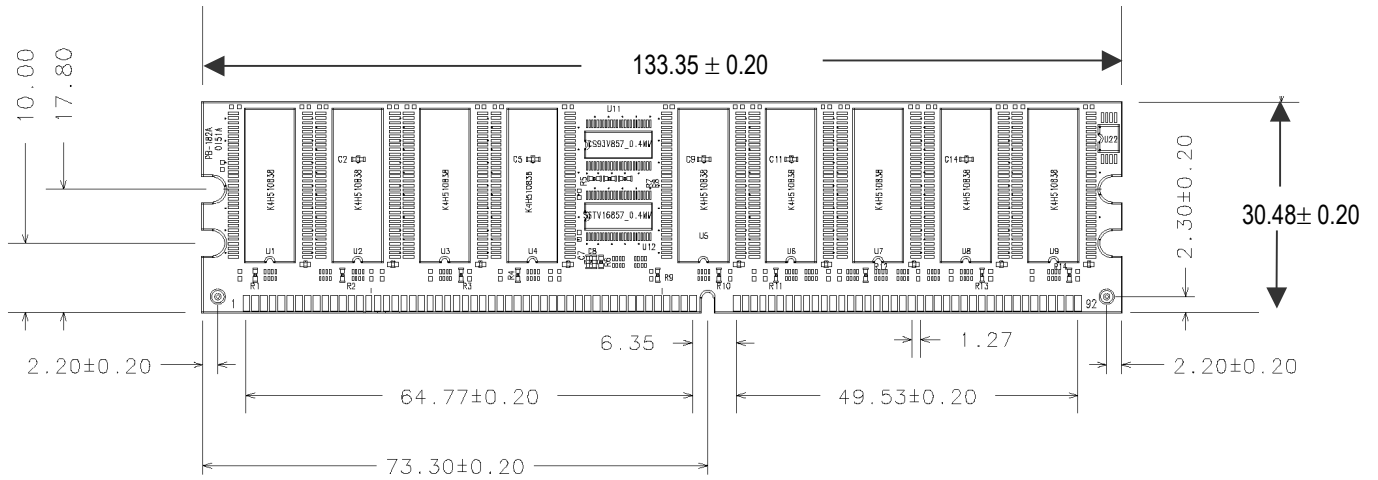
Note :

1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state.
A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

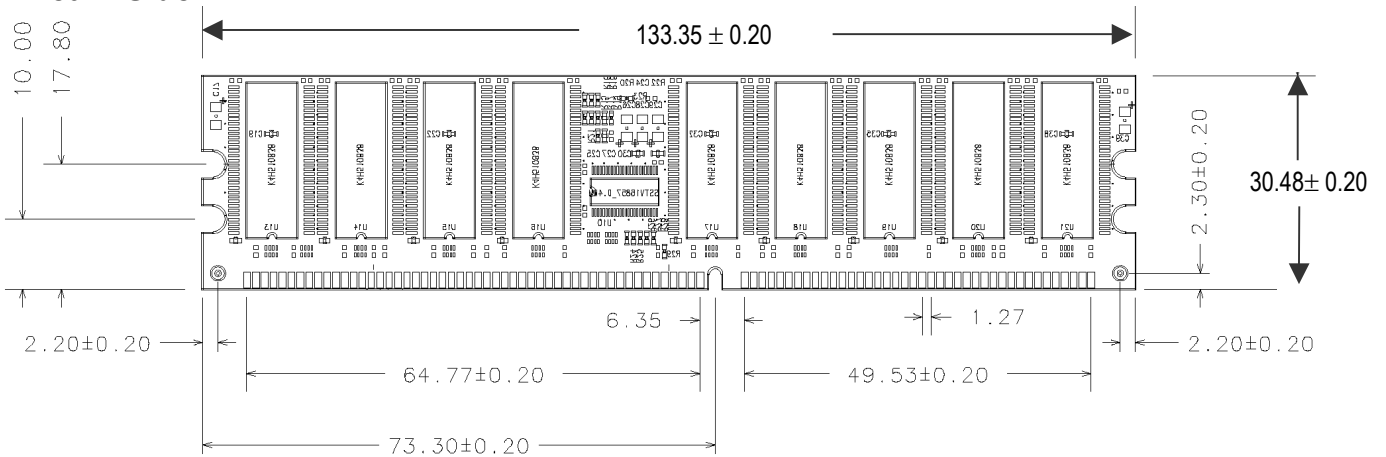
PACKAGE DIMENSIONS

Unit : mm

< Front -Side >



< Rear -Side >



ORDERING INFORMATION

| Part Number | Density | Org. | Package | Ref. | Vcc | MODE | MAX.frq |
|-------------------|----------|----------|-------------|------|------|------|--------------|
| HDD32M72D9RPW-10A | 256MByte | 32M x 72 | 184PIN DIMM | 8K | 2.5V | DDR | 100MHz/CL2 |
| HDD32M72D9RPW-13A | 256MByte | 32M x 72 | 184PIN DIMM | 8K | 2.5V | DDR | 133MHz/CL2 |
| HDD32M72D9RPW-13B | 256MByte | 32M x 72 | 184PIN DIMM | 8K | 2.5V | DDR | 133MHz/CL2.5 |