Agilent HSDL-3211 IrDA®
Data Compliant Low Power
1.15 Mbit/s Infrared Transceiver

Data Sheet

Features
- **Fully compliant to IrDA 1.4 physical layer low power specification from from 9.6 kbit/s to 1.152 Mbit/s (MIR)**
- **Miniature package**
  - **Height: 2.5 mm**
  - **Width: 8.0 mm**
  - **Depth: 3.0 mm**
- **No data rate switching required**
- **Typical link distance > 50 cm**
- **Guaranteed temperature performance, -25º to 85ºC**
  - **Critical parameters are guaranteed over temperature and supply voltage**
- **Low power consumption**
  - **Low shutdown current (1 nA typical)**
  - **Complete shutdown of TXD, RXD, and PIN diode**
- **Withstands >100 mV$_{p-p}$ power supply ripple typically**
- **Excellent EMI performance**
- **Vcc supply 2.4 to 3.6 Volts**
- **Interfacing with I/O logic circuits as low as 1.8 V**
- **Lead-free package**
- **LED stuck-high protection**
- **Designed to accommodate light loss with cosmetic windows**
- **IEC 825-class 1 eye safe**

Description
The HSDL-3211 is a new generation low profile high speed infrared transceiver module that provides interface between logic and IR signals for through-air, serial, half-duplex IR data-link. The module is fully compliant to IrDA Physical Layer specification version 1.4 low power from 9.6kbit/s to 1.152 Mbit/s (MIR) and is IEC825-Class 1 Eye Safe.

The HSDL-3211 can be shutdown completely to achieve very low power consumption. In the shutdown mode, the PIN diode will be inactive and thus producing very little photocurrent even under very bright ambient light. It is also designed to interface to input/output logic circuits as low as 1.8V. These features are ideal for mobile devices that require low power consumption.
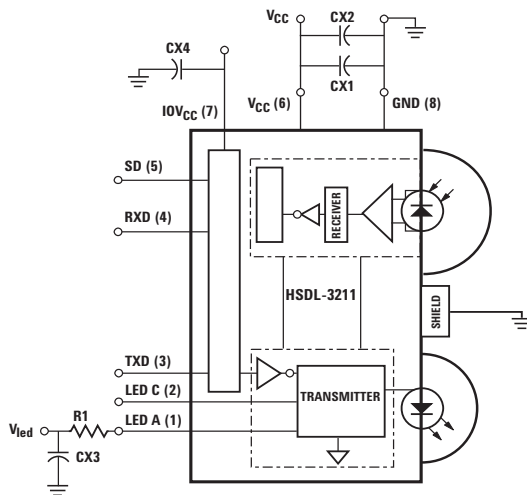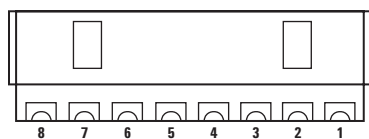
Applications
- **Mobile telecom**
  - **Mobile phones**
  - **Smart phones**
  - **Pagers**
- **Data communication**
  - **Pocket PC handheld products**
  - **Personal digital assistants**
  - **Portable printers**
- **Digital imaging**
  - **Digital cameras**
  - **Photo-imaging printers**
- **Electronic wallet**
- **Small industrial & medical instrumentation**
  - **General data collection devices**
  - **Patient & pharmaceutical data collection devices**

Figure 1. Functional block diagram of HSDL-3211.

Figure 2. Rear view diagram with pinout.

Agilent Technologies

Application Support Information
The Application Engineering Group is available to assist you with the application design associated with the HSDL-3211 infrared transceiver module. You can contact them through your local sales representatives for additional details.

Order Information

Part Number	Packaging Type	Package	Quantity
HSDL-3211-021	Tape and Reel	Front View	2500

I/O Pins Configuration Table

Pin	Symbol	Description	I/O Type	Notes
1	LED A	LED Anode	I	1
2	LED C	LED Cathode		2
3	TXD	Transmit Data. Active High.	I	3
4	RXD	Receive Data. Active Low.	O	4
5	SD	Shutdown. Active High.	I	5
6	Vcc	Supply Voltage		6
7	IOVcc	Input/Output ASIC Vcc		7
8	GND	Ground		8
-	Shield	EMI Shield		9

Recommended Application Circuit Components

Component	Recommended Value	Notes
R1	$3.9\Omega \pm 5\%$, 0.25 watt for $2.4 \leq Vled < 2.7V$ $5.6\Omega \pm 5\%$, 0.25 watt for $2.7 \leq Vled < 3.3V$ $10\Omega \pm 5\%$, 0.25 watt for $3.3 \leq Vled < 4.2V$ $15\Omega \pm 5\%$, 0.25 watt for $4.2 \leq Vled < 5.5V$	
CX1, CX4	$0.47\ \mu F \pm 20\%$, X7R Ceramic	10
CX2, CX3	$6.8\ \mu F \pm 20\%$, Tantalum	11

Notes:
1. Tied through external series resistor, R1, to regulated Vled from 2.4 to 5.5V. Please refer to table below for recommended series resistor value.
2. Internally connected to LED driver. Leave this pin unconnected.
3. This pin is used to transmit serial data when SD pin is low. If this pin is held high for longer than 50 ms, the LED is turned off. Do NOT float this pin.
4. This pin is capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. The pin is in tri-state when the transceiver is in shutdown mode. The receiver output echoes transmitted signal.
5. The transceiver is in shutdown mode if this pin is high. Do NOT float this pin.
6. Regulated, 2.4 to 3.6 Volts.
7. Connect to ASIC logic controller Vcc voltage or supply voltage. The voltage at this pin must be equal to or less than supply voltage.
8. Connect to system ground.
9. Connect to system ground via a low inductance trace. For best performance, do not connect directly to the transceiver pin GND
10. CX1 must be placed within 0.7 cm of the HSDL-3211 to obtain optimum noise immunity.
11. In environments with noisy power supplies, including CX2, as shown in Figure 1, can enhance supply ripple rejection performance.

CAUTIONS: The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is $\leq 50°C/W$.

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature	T_S	-40	+100	°C	
Operating Temperature	T_A	-25	+85	°C	
LED Anode Voltage	V_{LEDA}	0	6.5	V	
Supply Voltage	V_{CC}	0	6.5	V	
Input Voltage: TXD, SD/Mode	V_I	0	6.5	V	
Output Voltage: RXD	V_O	0	6.5	V	
DC LED Transmit Current	I_{LED} (DC)		150	mA	
Average Transmit Current	I_{LED} (PK)		600	mA	$\leq 90\,\mu s$ pulse width $\leq 25\%$ duty cycle

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature		T_A	-25		+85	°C	
Supply Voltage		V_{CC}	2.4		3.6	V	
Input/Output Voltage		IOVcc	1.8		Vcc	V	
Logic Input Voltage for TXD, SD/Mode	Logic High	V_{IH}	$IOV_{cc} - 0.5$		IOV_{cc}	V	
	Logic Low	V_{IL}	0		0.4	V	
Receiver Input Irradiance	Logic High	$EI_{H, min}$ $EI_{H, max}$			0.0081 500	mW/cm^2 mW/cm^2	9.6kbit/s $\leq$ in-band signals ≤ 1.152 Mbit/s[12]
	Logic Low	EI_L			0.3	$\mu W/cm^2$	For in-band signals[12]
LED (Logic High) Current Pulse Amplitude		I_{LEDA}		150		mA	
Receiver Data Rate			0.0096		1.152	Mbit/s	

Note :

12. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as $850 \leq \lambda p \leq 900$ nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification v1.4.

Electrical & Optical Specifications

Specifications (Min. & Max. values) hold over the recommended operating conditions unless otherwise noted.
Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C, Vcc set to 3.0V and IOVcc set to 1.8V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver							
Viewing Angle		2θ	30			°	
Peak Sensitivity Wavelength		λp		880		nm	
RXD Output Voltage	Logic High	V_{OH}	$IOV_{CC} - 0.2$		IOV_{CC}	V	I_{OH} = -200 μA, EI ≤ 0.3 μW/cm^2
	Logic Low	V_{OL}	0		0.4	V	I_{OL} = 200 μA, EI ≥ 8.1 μW/cm^2
RXD Pulse Width (SIR)[13]		t_{PW} (SIR)	1		4.0	μs	$\theta \leq 15°$, C_L = 9 pF
RXD Pulse Width (MIR)[14]		t_{PW}(MIR)	100		500	ns	$\theta \leq 15°$, C_L = 9 pF
RXD Rise and Fall Times		t_r, t_f		25		ns	C_L = 9 pF
Receiver Latency Time[15]		t_L		25	50	μs	
Receiver Wake Up Time[16]		t_W		50	100	μs	
Transmitter							
Radiant Intensity		IE_H	10	45		mW/sr	I_{LEDA}= 150 mA, $\theta \leq 15°$, $V_{TXD} \geq V_{IH}$, $V_{SD} \leq V_{IL}$, Ta=25°C
Viewing Angle		2θ	30		60	°	
Peak Wavelength		λ_p		875		nm	
Spectral Line Half Width		$\Delta\lambda$			35	nm	
TXD Input Current	High	I_H		0.02	10	μA	$V_{TXD} \geq V_{IH}$
	Low	I_L	-10	-0.02	10	μA	$0 \leq V_{TXD} \leq V_{IL}$
LED ON Current		I_{LEDA}		150		mA	$V_{TXD} \geq V_{IH}$, R1=5.6ohm, Vled=3.0V
TXD Pulse Width (SIR)		t_{PW} (SIR)	1.5	1.6	1.8	μs	t_{PW} (TXD) = 1.6 μs at 115.2 kbit/s
TXD Pulse Width (MIR)		t_{PW}(MIR)	148	217	260	ns	t_{PW} (TXD) = 217 ns at 1.152 Mbit/s
Maximum Optical PW[17]		$t_{PW(max.)}$		50	100	μs	
TXD Rise and fall Time (Optical)		t_r, t_f		40		ns	t_{PW} (TXD) = ns at 1.152 Mbit/s
LED Anode On-State Voltage		$V_{ON(LEDA)}$		1.6	2.0	V	I_{LEDA}=150 mA, $V_{TXD} \geq V_{IH}$
Transceiver							
Supply Current	Shutdown	I_{CC1}		0.001	1	μA	$V_{SD} \geq V_{IH}$, Ta= 25 °C
	Idle	I_{CC2}		0.4	1.0	mA	$V_{SD} \leq V_{IL}$, $V_{TXD} \leq V_{IL}$, EI=0

Notes:

13. For in-band signals from 9.6 kbit/s to 115.2 kbit/s, where 9 μW/cm^2 ≤ EI ≤ 500 mW/cm^2.

14. For in-band signals from 0.576 Mbit/s to 1.152 Mbit/s, where 22.5 μW/cm^2 ≤ EI ≤ 500 mW/cm^2.

15. Latency time is defined as the time from the last TxD light output pulse until the receiver has recovered full sensitivity.

16. Receiver wake up time is measured from Vcc power on or SD pin high to low transition to a valid RXD output.

17. The maximum optical PW is the maximum time the LED remains on when the TXD is constantly high. This is to prevent long turn on time of the LED for eye safety protection.
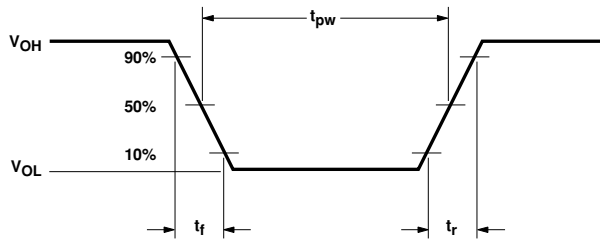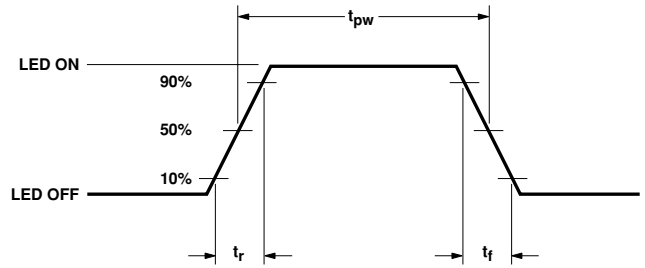
Figure 3. RxD output waveform.
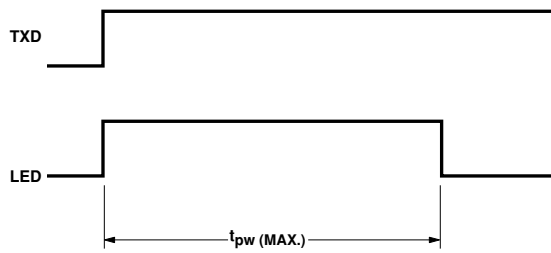

Figure 4. LED optical waveform.

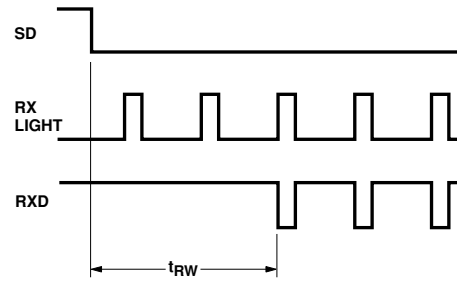**Figure 5. TxD "Stuck On" protection waveform.**
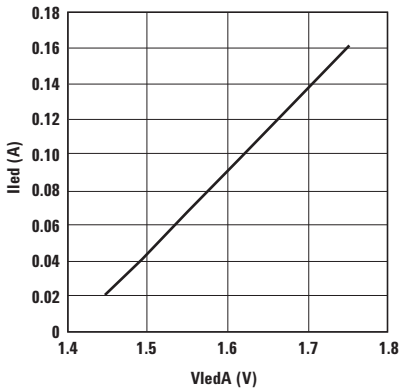

Figure 6. Receiver wakeup time waveform.
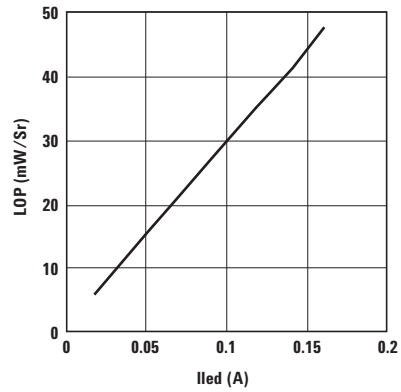

Figure 7. LED anode voltage vs. LED current.

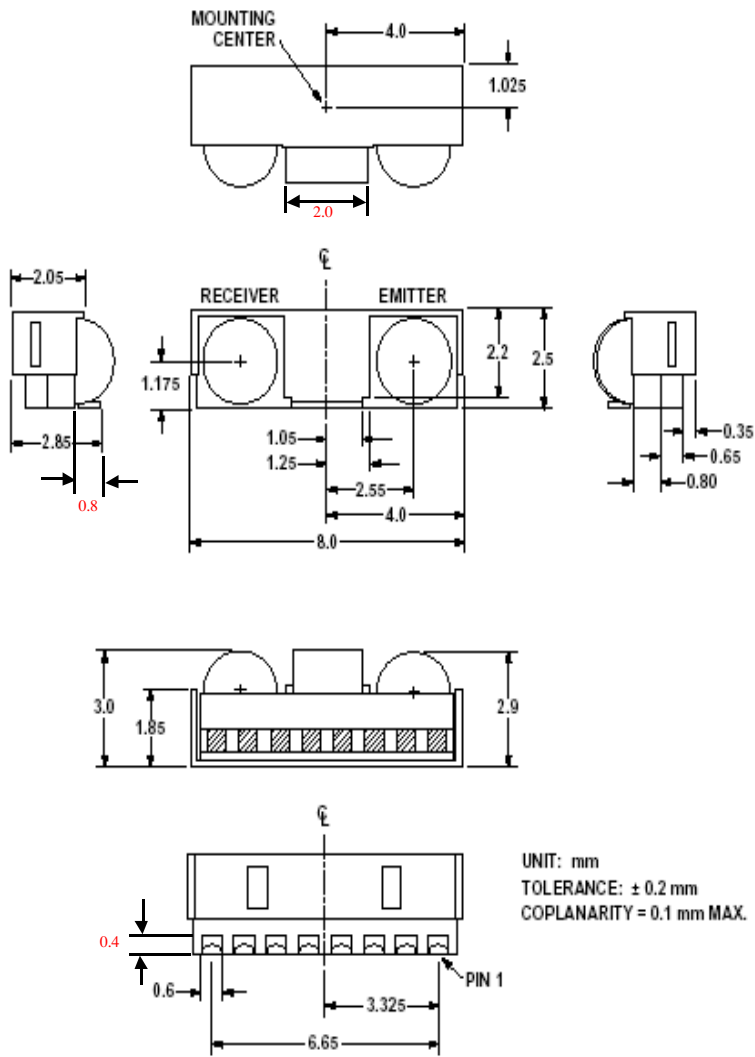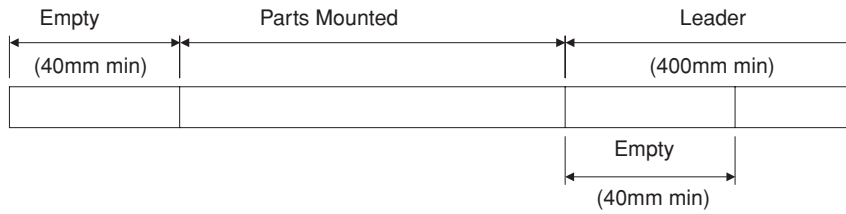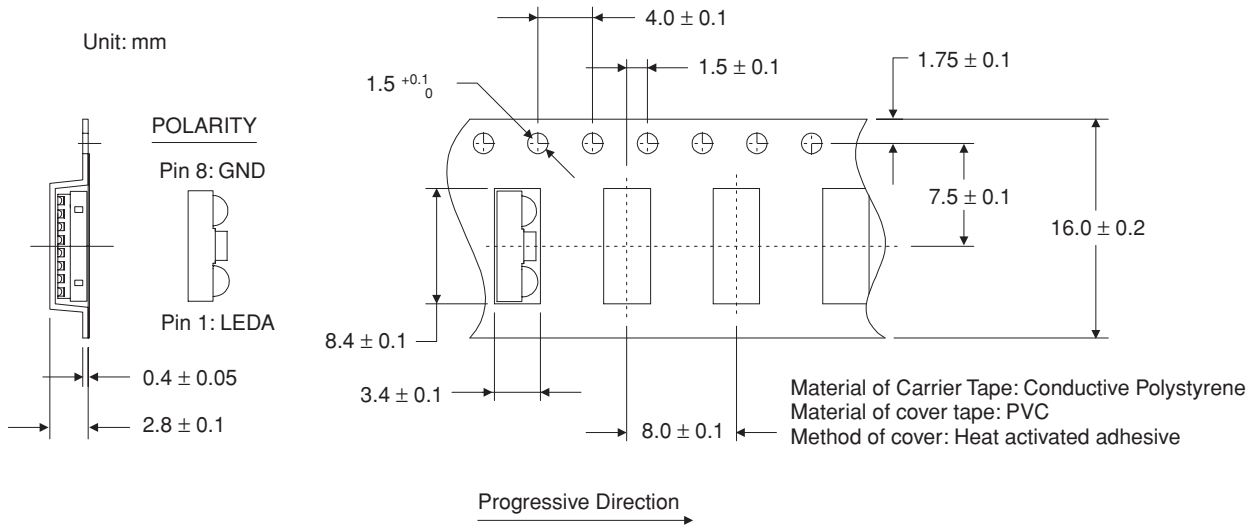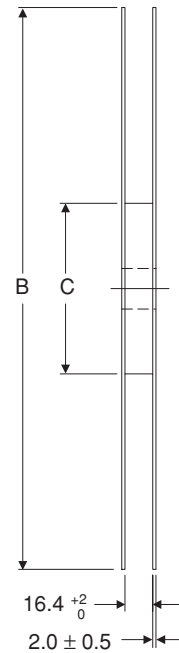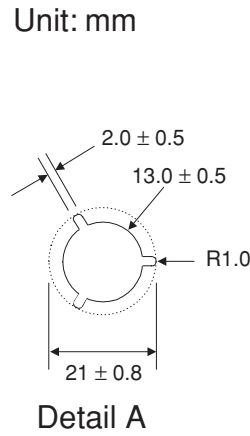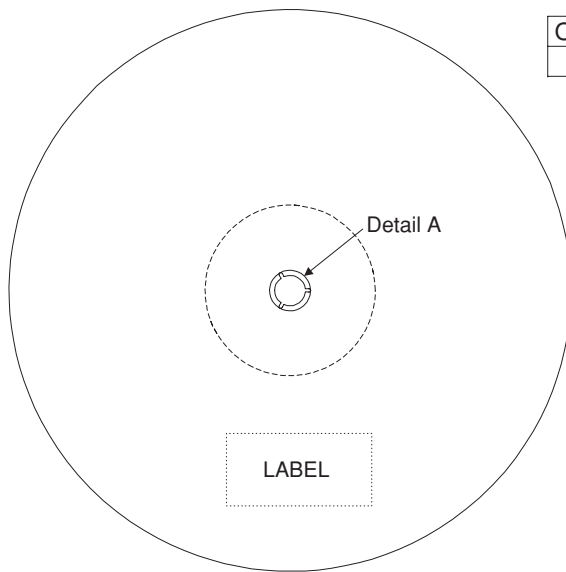**Figure 8. LED current vs. radiant intensity.**

HSDL-3211 Package Dimensions

MOUNTING CENTER

4.0

1.025

2.0

2.05

RECEIVER   EMITTER

2.2   2.5

1.175

2.85

0.8

1.05
1.25

2.55

4.0

8.0

0.35
0.65
0.80

3.0   1.85   2.9

0.4

0.6

3.325

6.65

PIN 1

UNIT: mm
TOLERANCE: ± 0.2 mm
COPLANARITY = 0.1 mm MAX.

6

HSDL-3211 Tape and Reel Dimensions

Unit: mm

POLARITY

Pin 8: GND

Pin 1: LEDA

0.4 ± 0.05

2.8 ± 0.1

4.0 ± 0.1

1.5 ± 0.1

1.75 ± 0.1

$1.5 ^{+0.1}_{0}$

7.5 ± 0.1

16.0 ± 0.2

8.4 ± 0.1

3.4 ± 0.1

8.0 ± 0.1

Material of Carrier Tape: Conductive Polystyrene
Material of cover tape: PVC
Method of cover: Heat activated adhesive

Progressive Direction

Empty | Parts Mounted | Leader

(40mm min) | | (400mm min)

Empty

(40mm min)

Option #	"B"	"C"	Quantity
021	330	80	2500

Unit: mm

Detail A

LABEL

2.0 ± 0.5

13.0 ± 0.5

R1.0

21 ± 0.8

Detail A

B   C

$16.4 ^{+2}_{0}$

2.0 ± 0.5

Note: The carrier tape is compliant to the packaging materials standards for ESD sensitive device, EIA-541

Moisture Proof Packaging
All HSDL-3211 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 4.

Baking Conditions
If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.
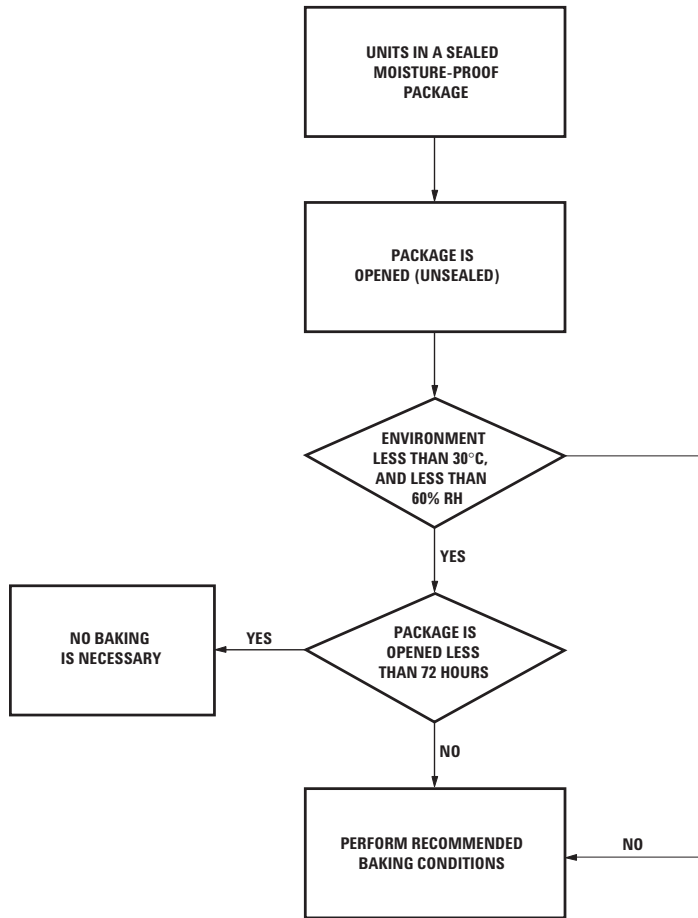
Package	Temp.	Time
In reels	60°C	≥ 48 hours
In bulk	100°C	≥ 4 hours
	125°C	≥ 2 hours
	150°C	≥ 1 hour

Baking should only be done once.

Recommended Storage Conditions
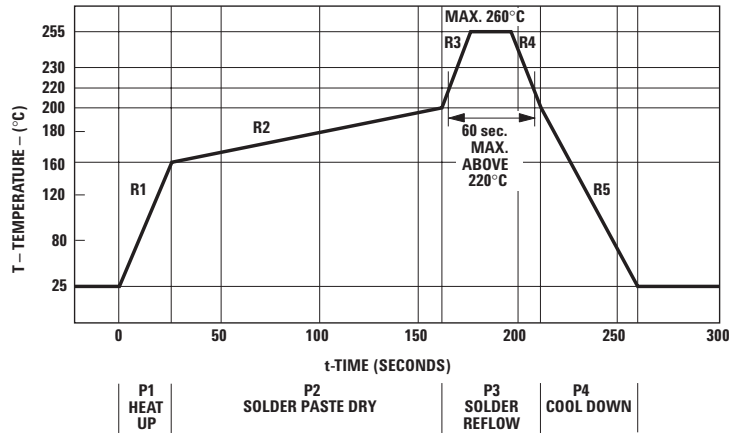
Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering
After removal from the bag, the parts should be soldered within three days if stored at the recommended storage conditions. If times longer than three days are needed, the parts must be stored in a dry box.

Figure 9. Baking conditions chart.

Recommended Reflow Profile

Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 160°C	4°C/s
Solder Paste Dry	P2, R2	160°C to 200°C	0.5°C/s
Solder Reflow	P3, R3	200°C to 255°C (260°C at 10 seconds max)	4°C/s
	P3, R4	255°C to 200°C	-6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and HSDL-3211 castellation pins are heated to a temperature of 160°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3211 castellations.

Process zone P2 should be of sufficient time duration (60 to 120 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 60 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 60 seconds, the intermetallic

growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3211 castellations to change dimensions evenly, putting minimal stresses on the HSDL-3211 transceiver.

Appendix A: SMT Assembly Application Note

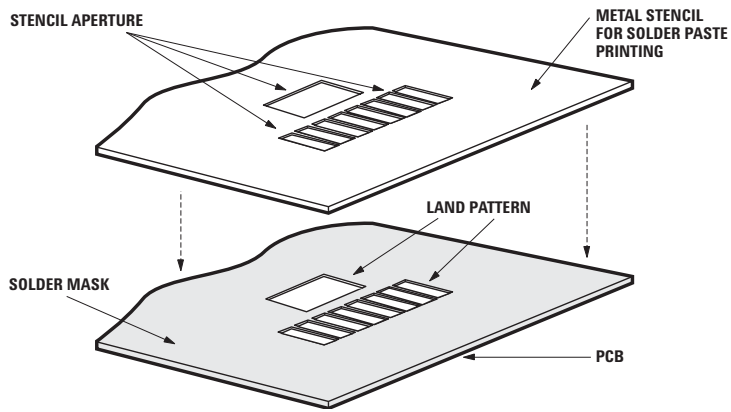### Solder Pad, Mask and Metal Stencil Aperture

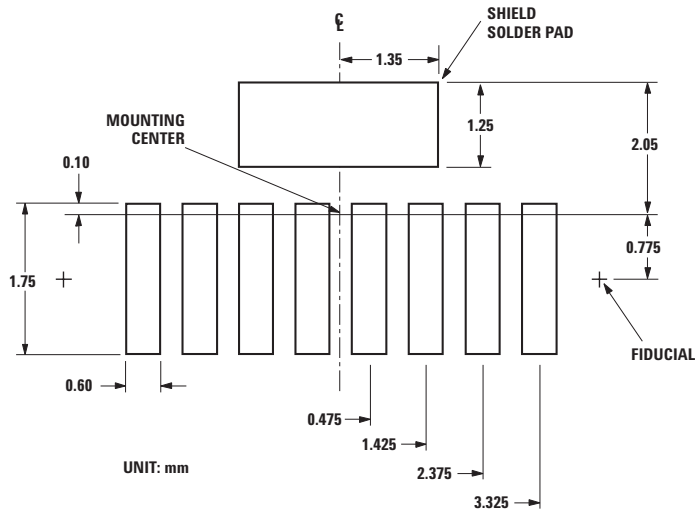**Figure 10. Stencil and PCBA.**

Recommended Land Pattern

Figure 11. Stencil and PCBA.

Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.152 mm (0.006 inches) or a 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used.

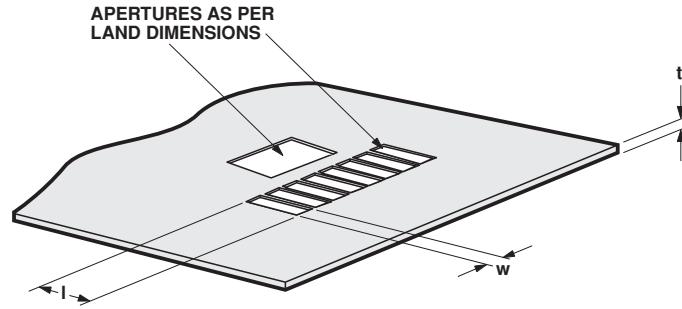Aperture opening for shield pad is 2.7 mm x 1.25 mm as per land pattern.

Figure 12. Solder stencil aperature.

Stencil thickness, t (mm)	Aperture size (mm)	
	length, l	width, w
0.152 mm	2.60 ± 0.05	0.55 ± 0.05
0.127 mm	3.00 ± 0.05	0.55 ± 0.05

Adjacent Land Keepout and Solder Mask Areas

Adjacent land keep-out is the **maximum space** occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

The minimum solder resist strip width required to avoid solder bridging adjacent pads is **0.2 mm.**

It is recommended that two fiducial crosses be place at mid-length of the pads for unit alignment.

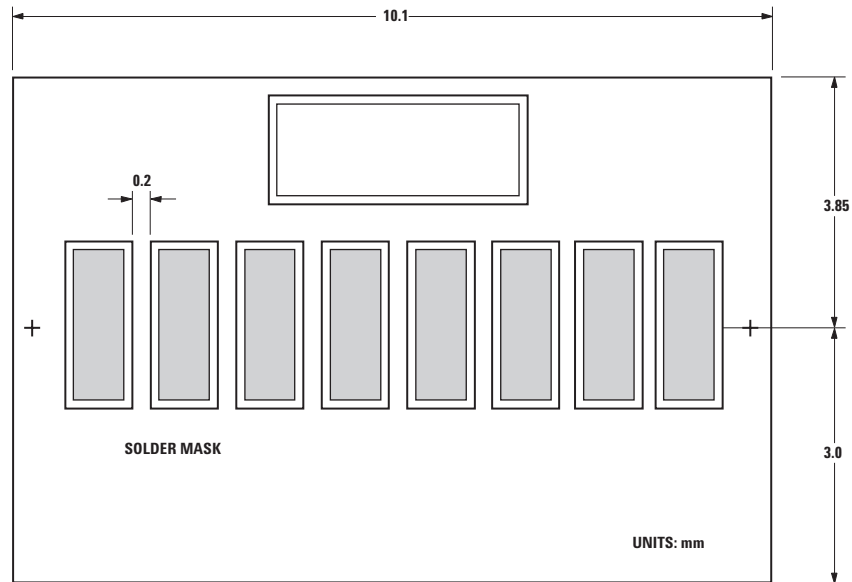**Note:** Wet/Liquid Photo-Imageable solder resist/mask is recommended.

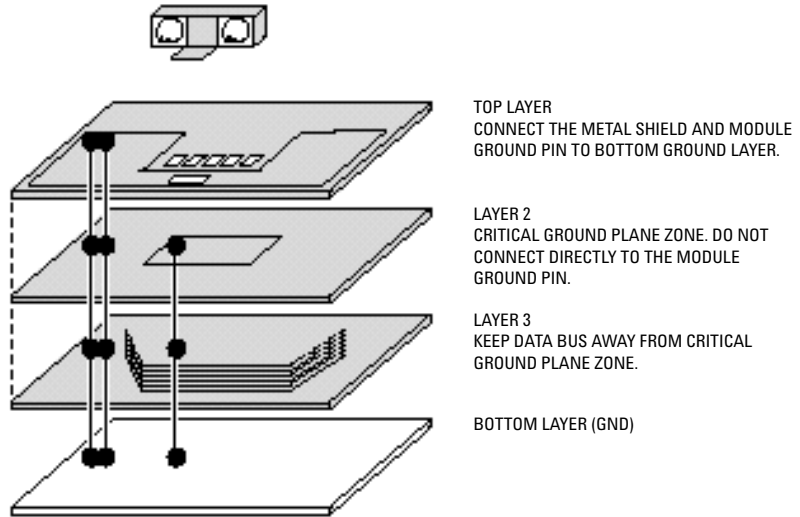Figure 13. Adjacent land keepout and solder mask areas.

Appendix B: PCB Layout Suggestion

The following PCB layout guidelines should be followed to obtain a good PSRR and EM immunity resulting in good electrical performance. Things to note:

1. The ground plane should be continuous under the part, but should not extend under the shield trace.

2. The shield trace is a wide, low inductance trace back to the system ground. CX1, CX2, CX3, and CX4 are optional supply filter capacitors; they may be left out if a clean power supply is used.

3. Vled can be connected to either unfiltered or unregulated power supply. If Vled and Vcc share the same power supply, CX3 need not be used and the connections for CX1 and CX2 should be before the current limiting resistor R1. In a noisy environment, including capacitor CX2 can enhance supply rejection. CX1 is generally a ceramic capacitor of low inductance providing a wide frequency response while CX2 and CX3 are tantalum capacitors of big volume and fast frequency response. The use of a tantalum capacitor is more critical on the Vled line, which carries a high current. CX4 is an optional ceramic capacitor, similar to CX1, for the IOVcc line.

4. Preferably a multi-layered board should be used to provide sufficient ground plane. Use the layer underneath and near the transceiver module as Vcc, and sandwich that layer between ground connected board layers. Refer to the diagram below for an example of a 4 layer board.

TOP LAYER
CONNECT THE METAL SHIELD AND MODULE GROUND PIN TO BOTTOM GROUND LAYER.

LAYER 2
CRITICAL GROUND PLANE ZONE. DO NOT CONNECT DIRECTLY TO THE MODULE GROUND PIN.

LAYER 3
KEEP DATA BUS AWAY FROM CRITICAL GROUND PLANE ZONE.

BOTTOM LAYER (GND)

The area underneath the module at the second layer, and 3 cm in all directions around the module is defined as the critical ground plane zone. The ground plane should be maximized in this zone. Refer to application note AN1114 or the Agilent IrDA Data Link Design Guide for details. The layout below is based on a 2-layer PCB.
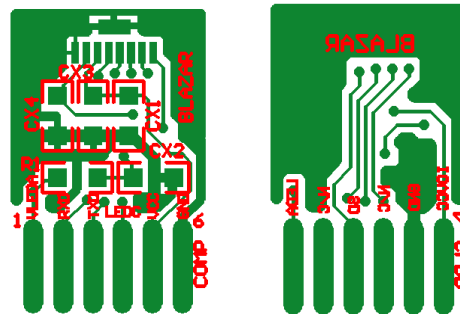

Figure 14. PCB layout suggestion.

Appendix C: General Application Guide for the HSDL-3211

Description
The HSDL-3211, a low-cost and small form factor infrared trans-ceiver, is designed to address the mobile computing market such as PDAs, as well as small-embedded mobile products such as digital cameras and cellular phones. It is fully compliant to IrDA 1.4 low power specification from 9.6 kb/s to 1.152 Mb/s, and supports HP-SIR and TV Remote modes.

The design of the HSDL-3211 also includes the following unique features:

• Low passive component count.

• Shutdown mode for low power consumption requirement.

• Interface to input/output logic circuits as low as 1.8V

Selection of Resistor R1
Resistor R1 should be selected to provide the appropriate peak pulse LED current over different ranges of Vcc as shown in the table below.

Interface to Recommended I/O chips
The HSDL-3211's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required. Data rate from 9.6 kb/s up to 1.152 Mb/s is available at the RXD pin.

The block diagram below shows how the IR port fits into a mobile phone and PDA platform.

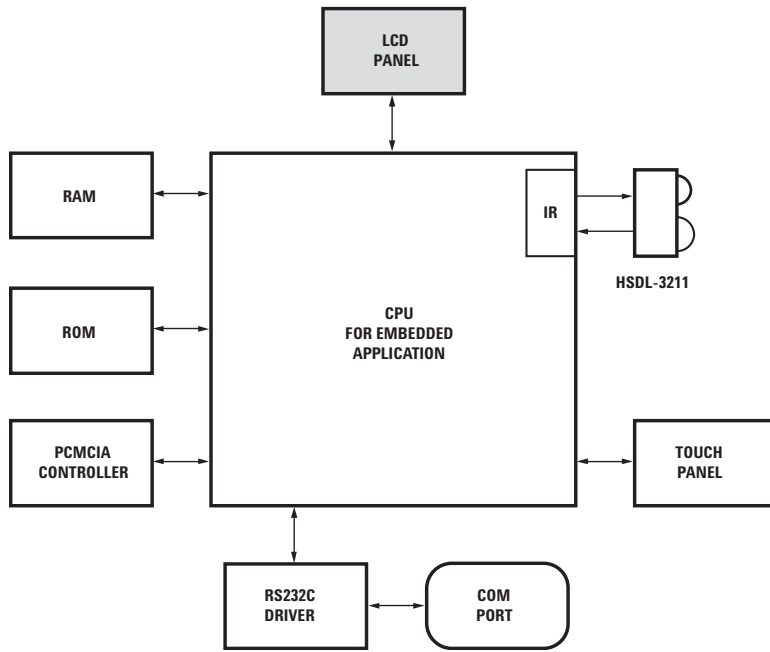| Recommended R1	Vled	Intensity	Minimum Peak Pulse LED Current
5.6Ω	3.0 V	45 mW/sr	150 mA
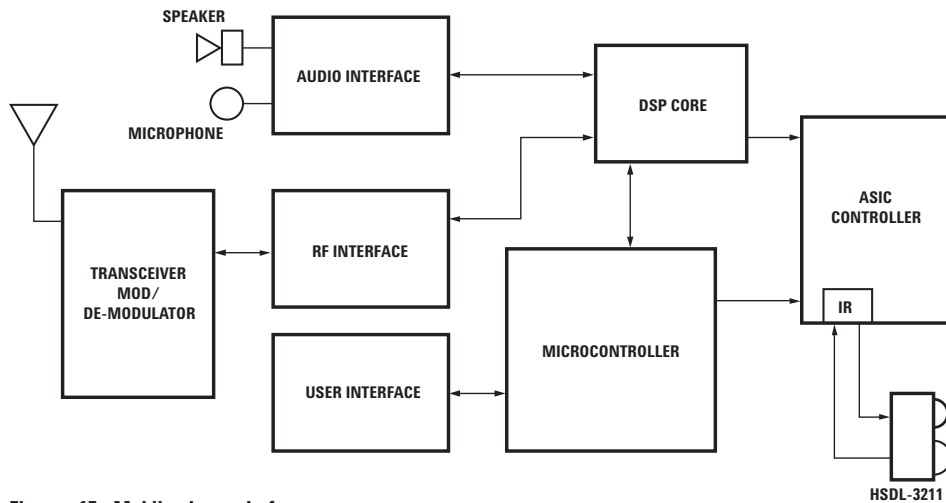
Figures 15. Mobile phone platform.

Figure 16. PDA platform.

The link distance testing was
done using typical HSDL-3211
units with SMC's FDC37C669
and FDC37N769 Super I/O
controllers. An IR link distance
of up to 75 cm was demonstrated
for SIR and MIR at full power.

Appendix D: Window Designs for HSDL-3211

Optical port dimensions for HSDL-3211

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30° and the maximum size corresponds to a cone angle of 60°.

In the figure below, X is the width of the window, Y is the height of the window and Z is the distance from the HSDL-3211 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 5.1mm. The equations for computing the window dimensions are as follows:

$$X = K + 2*(Z+D)*tanA$$

$$Y = 2*(Z+D)*tanA$$

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as

$$Z' = Z + t/n$$

where 't' is the thickness of the window and 'n' is the refractive index of the window material.

The depth of the LED image inside the HSDL-3211, D, is 3.17mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 15° and the maximum is 30°. Assuming the thickness of the window to be negligible, the equations result in the following tables and graphs.
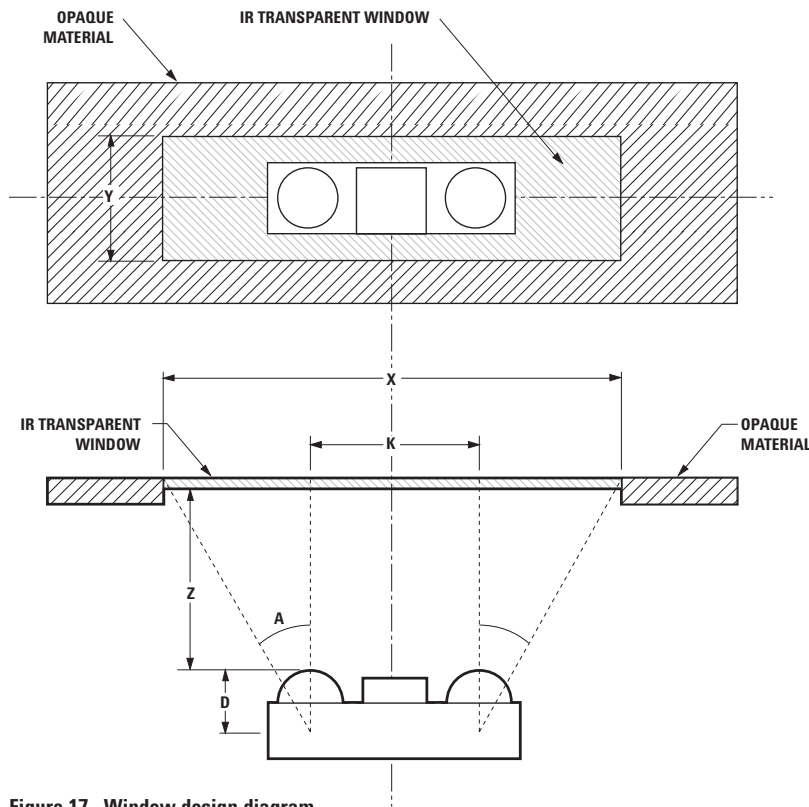

Figure 17. Window design diagram.

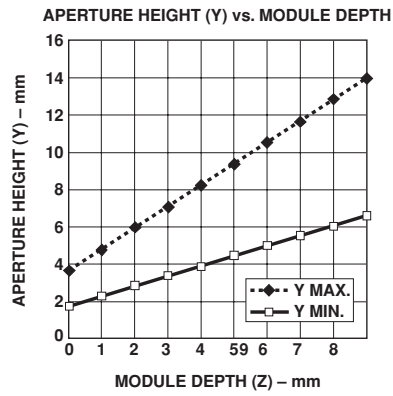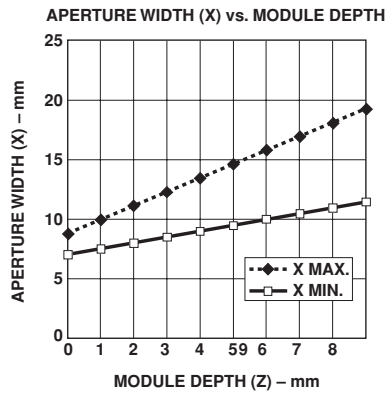| Module Depth (z) mm	Aperture Width (x, mm)		Aperture Height (y, mm)	
	Max.	Min.	Max.	Min.
0	8.76	6.80	3.66	1.70
1	9.92	7.33	4.82	2.33
2	11.07	7.87	5.97	2.77
3	12.22	8.41	7.12	3.31
4	13.38	8.94	8.28	3.84
5	14.53	9.48	9.43	4.38
6	15.69	10.01	10.59	4.91
7	16.84	10.55	11.74	5.45
8	18.00	11.09	12.90	5.99
9	19.15	11.62	14.05	6.52

Figure 18. Aperture width (X) vs. module depth.

Figure 19. Aperture height (Y) vs. module depth.

Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10% or less for best optical performance. Light loss should be measured at 875 nm. The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics.

Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.

Recommended Plastic Materials:

Material #	Light Transmission	Haze	Refractive Index
Lexan 141	88%	1%	1.586
Lexan 920A	85%	1%	1.586
Lexan 940A	85%	1%	1.586

Note: 920A and 940A are more flame retardant than 141.

**Flat Window
(First Choice)**

**Curved Front and Back
(Second Choice)**

**Curved Front, Flat Back
(Do Not Use)**
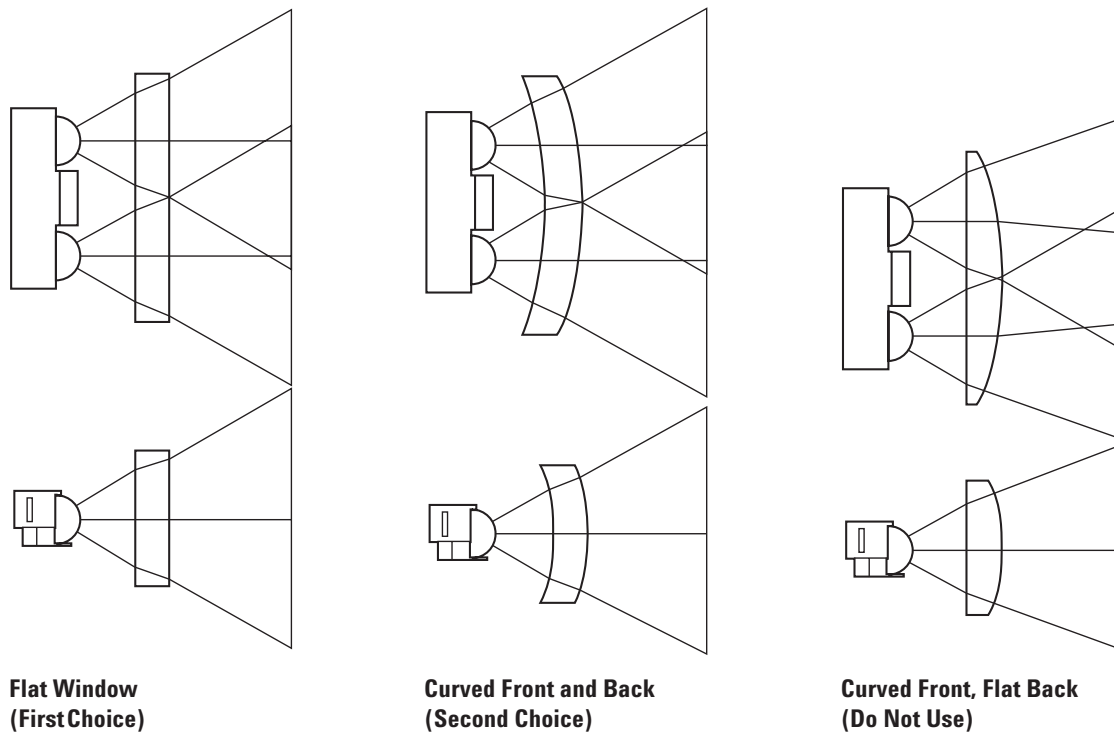
Figure 20. Shape of windows.

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