# MX28F1000

## 1M-BIT (128K x 8) CMOS FLASH MEMORY

## FEATURES

- 131,072 bytes by 8-bit organization
- Fast access time: 90/120/150 ns
- Low power consumption
  - 50mA maximum active current
  - 100μA maximum standby current
- Programming and erasing voltage 12V ± 5%
- Command register architecture
  - Byte Programming (10μs typical)
  - Chip Erase (1 sec typical)
  - Auto chip erase 5 seconds typical (including preprogramming time)
  - Block Erase (16384 bytes by 8 blocks)
- Auto Erase (chip & block) and Auto Program

- $\overline{DATA}$ polling
- Toggle bit
- 10,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Advanced CMOS Flash memory technology
- Compatible with JEDEC-standard byte-wide 32-pin EPROM pinouts
- Package type:
  - 32-pin plastic DIP
  - 32-pin PLCC
  - 32-pin SOP
  - 32-pin TSOP (Type 1)

## GENERAL DESCRIPTION

The MX28F1000 is a 1-mega bit Flash memory organized as 128K bytes of 8 bits each. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F1000 is packaged in 32-pin PDIP, PLCC, SOP and TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX28F1000 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX28F1000 has separate chip enable (CE) and output enable (OE ) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F1000 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.
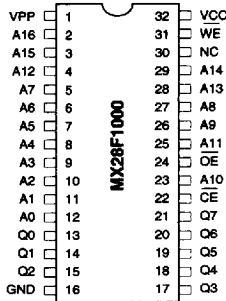
MXIC Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX28F1000 uses a 12.0V ± 5% VPP supply to perform the High

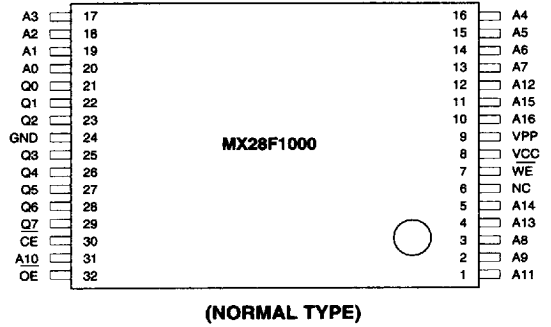Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.
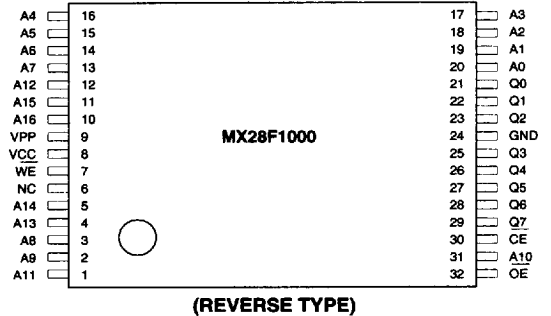
FLASH MEMORY

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## PIN CONFIGURATIONS

### 32 PDIP



### TSOP (TYPE 1)



(NORMAL TYPE)

### 32 SOP





(REVERSE TYPE)
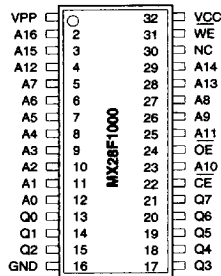
### 32 PLCC
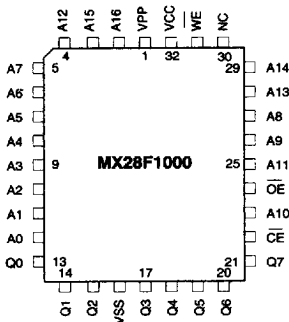


### PIN DESCRIPTION:

| SYMBOL | PIN NAME |
|--------|----------|
| A0~A16 | Address Input |
| Q0~Q7 | Data Input/Output |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write enable Pin |
| VPP | Program Supply Voltage |
| VCC | Power Supply Pin (+5V) |
| GND | Ground Pin |

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## BLOCK DIAGRAM
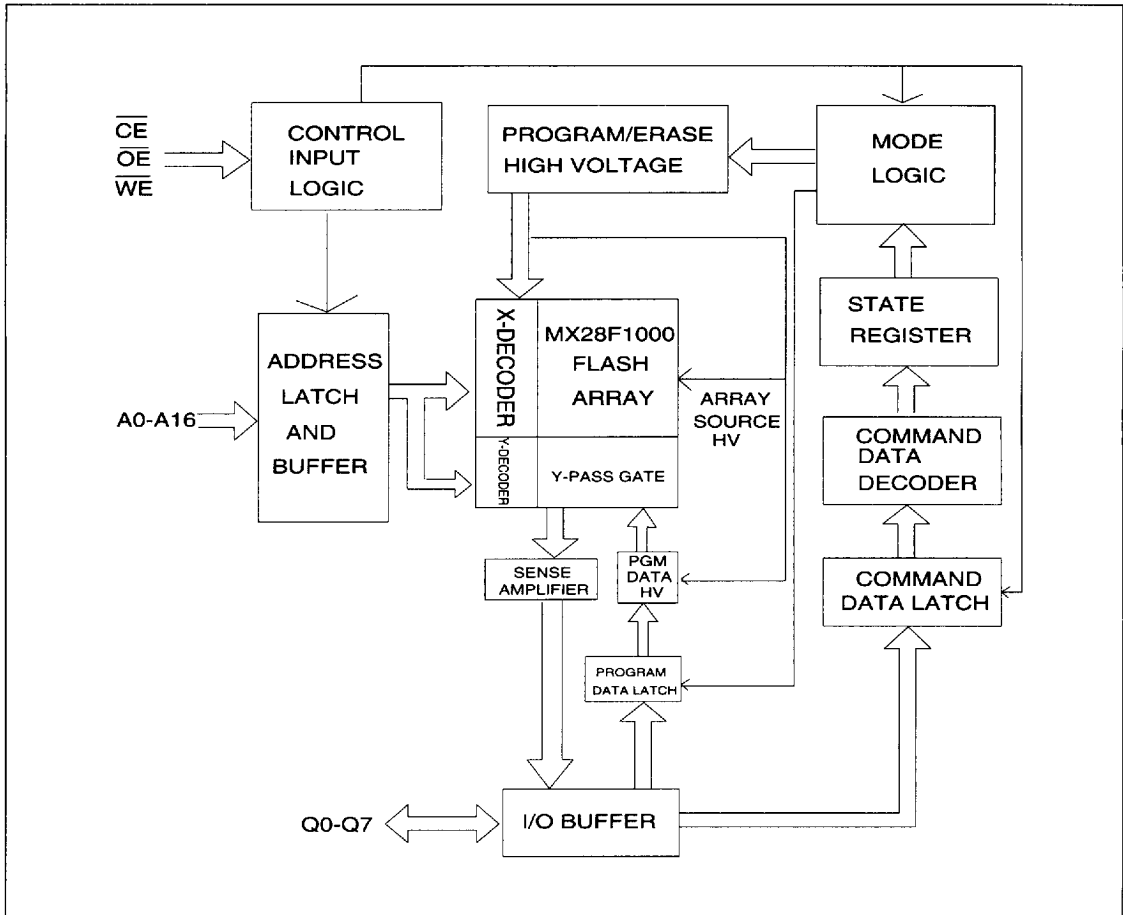
## AUTOMATIC PROGRAMMING

The MX28F1000 is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical room temperature chip programming time of the MX28F1000 is less than 5 seconds.

## AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's High Reliability Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than one second. The device may also be erased using the Automatic Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device.

## AUTOMATIC BLOCK ERASE

The MX28F1000 is block(s) erasable using MXIC's Auto Block Erase algorithm. Block erase modes allow one to 8 blocks of the array to be erased in one erase cycle. Each block comprises 16K bytes memory cells and is selected by addresses A14-A16. The Automatic Block Erase algorithm automatically programs the specified block(s) prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device.

## AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify, and counts the number of sequences. A status bit similar to DATA polling, provides feedback to the user as to the status of the programming operation.

## AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify, and counts the number of sequences. A status bit, similar to DATA polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the MX28F1000 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX28F1000 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

**TABLE 1. COMMAND DEFINITIONS**

| COMMAND | BUS CYCLES | FIRST BUS CYCLE | | | SECOND BUS CYCLE | | |
|---|---|---|---|---|---|---|---|
| | | OPERATION | ADDRESS | DATA | OPERATION | ADDRESS | DATA |
| Read Memory | 1 | Write | X | 00H | | | |
| Read Identified codes | 2 | Write | X | 90H | Read | IA | ID |
| Setup Erase/ Erase (chip) | 2 | Write | X | 20H | Write | X | 20H |
| Setup Erase/ Erase (block) | 2 | Write | X | 60H | Write | EA | 60H |
| Erase verify | 2 | Write | EVA | A0H | Read | X | EVD |
| Setup auto erase/ auto erase (chip) | 2 | Write | X | 30H | Write | X | 30H |
| Setup auto erase/ auto erase (block) | 2 | Write | X | 20H | Write | EA | D0H |
| Setup auto program/ program | 2 | Write | X | 40H | Write | PA | PD |
| Reset | 2 | Write | X | FFH | Write | X | FFH |

**FLASH MEMORY**

**Note:**

IA = Identifier address
EA = Block of memory location to be erased
PA = Address of memory location to be programmed
ID = Data read from location IA during device identification
PD = Data to be programmed at location PA
EVA = Address of memory location to be read during erase verify.
EVD = Data read from location EVA during erase verify.

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## COMMAND DEFINITIONS

When low voltage is applied to the VPP pin, the contents of the command register default to 00H, enabling read-only operation.

Placing high voltage on the VPP pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 1 defines these MX28F1000 register commands. Table 2 defines the bus operations of MX28F1000.

### TABLE 2. MX28F1000 BUS OPERATIONS

| OPERATION | | VPP(1) | A0 | A9 | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | DQ0-DQ7 |
|-----------|---|--------|-----|-----|------|------|------|---------|
| **READ-ONLY** | Read | VPPL | A0 | A9 | VIL | VIL | X | Data Out |
| | Output Disable | VPPL | X | X | VIL | VIH | VIH | Tri-State |
| | Standby | VPPL | X | X | VIH | X | X | Tri-State |
| | Read Silicon ID (Mfr)(2) | VPPL | VIL | VID(3) | VIL | VIL | VIH | Data = C2H |
| | Read Silicon ID (Device)(2) | VPPL | VIH | VID(3) | VIL | VIL | VIH | Data = 11H |
| **READ/WRITE** | Read | VPPH | A0 | A9 | VIL | VIL | VIH | Data Out(4) |
| | Standby(5) | VPPH | X | X | VIH | X | X | Tri-State |
| | Write | VPPH | A0 | A9 | VIL | VIH | VIL | Data In(6) |

**NOTES:**
1. VPPL may be grounded, a no-connect with a resistor tied to ground, or ≤ VCC + 2.0V. VPPH is the programming voltage specified for the device. When VPP = VPPL, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1. All other addresses are low.
3. VID is the Silicon-ID-Read high voltage.(11.5V to 13v)
4. Read operations with VPP = VPPH may access array data or Silicon ID codes.
5. With VPP at high voltage, the standby current equals ICC + IPP (standby).
6. Refer to Table 1 for valid Data-In during a write operation.
7. X can be VIL or VIH.

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# READ COMMAND

While VPP is high, for erasure and programming, memory contents can also be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon VPP power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the VPP power transition. Where the VPP supply is hard-wired to the MX28F1000, the device powers up and remains enabled for reads until the command register contents are changed.

# SILICON-ID-READ COMMAND

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The MX28F1000 contains a Silicon-ID-Read operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of C2H. A read cycle from address 0001H returns the device code of 11H.

# SET-UP CHIP ERASE/ERASE COMMANDS

Set-up Chip Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse.

This two-step sequence of set-up followed by execution

ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the VPP pin. In the absence of this high voltage, memory contents are protected against erasure.

# SET-UP BLOCK ERASE/ERASE COMMANDS

Set-up Block Erase is a command-only operation that stages the device for electrical erasure of all selected block(s) in the array. The set-up erase operation is performed by writing 60H to the command register.

To enter block-erasure, the block erase command 60H must be written again to the command register. The block erase mode allows 1 to 8 blocks of the array to be erased in one internal erase cycle. Internally, there are 8 registers (flags) addressed by A14 to A16. First block address is loaded into internal registers on the 2-nd falling of $\overline{WE}$. Each successive block load cycles, started by the falling edge of $\overline{WE}$, must begin within 30μs from the rising edge of the preceding $\overline{WE}$. Otherwise, the loading period ends and internal block erase cycle starts. When the data on DQ7 is "1" at which time auto erase ends and the device returns to the Read mode.

# ERASE-VERIFY COMMAND

After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the $\overline{WE}$ pulse.

The MX28F1000 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

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In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. The High Reliability Erase algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the MX28F1000.

## SET-UP AUTOMATIC CHIP ERASE/ERASE COMMANDS

The automatic chip erase does not require the device to be entirely pre-programmed prior to excuting the Automatic set-up erase command and Automatic chip erase command. Upon executing the Automatic chip erase command, the device automatically will program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are complete when the data on DQ7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Automatic set-up erase command is a command-only operation that stages the device for automatic electrical erasure of all bytes in the array. Automatic set-up erase is performed by writing 30H to the command register.

To command automatic chip erase, the command 30H must be written again to the command register. The automatic chip erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" at which time the device returns to the Read mode.

## SET-UP AUTOMATIC BLOCK ERASE/ERASE COMMANDS

The automatic block erase does not require the device to be entirely pre-programmed prior to executing the Automatic set-up block erase command and Automatic block erase command. Upon executing the Automatic block erase command, the device automatically will program and verify the block(s) memory for an all-zero data pattern. The system is not required to provide any controls or timing during these operations.

When the block(s) is automatically verified to contain an all-zero pattern, a self-timed block erase and verify begin. The erase and verify operations are complete when the data on DQ7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Block Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Automatic set-up block erase command is a command only operation that stages the device for automatic electrical erasure of selected blocks in the array. Automatic set-up sector erase is performed by writing 20H to the command register.

To enter automatic sector erase, the user must write the command D0H to the command register. Block addresses selected by A14-A16 are loaded into internal register on the 2nd falling edge of $\overline{WE}$. Each successive block load cycles, started by the falling edge of $\overline{WE}$, must begin within 30µs from the rising edge of the preceding $\overline{WE}$. Otherwise, the loading period ends and internal auto block erase cycle starts. When the data on DQ7 is "1" at which time auto erase ends and the device returns to the Read mode.

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## SET-UP AUTOMATIC PROGRAM/PROGRAM COMMANDS

The Automatic Set-up Program is a command-only operation that stages the device for automatic programming. Automatic Set-up Program is performed by writing 40H to the command register.

Once the Automatic Set-up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit at which time the device returns to the Read mode (no program verify command is required).

## RESET COMMAND

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

## WRITE OPERATON STATUS

### TOGGLE BIT-DQ6

The MX28F1000 features a "Toggle Bit" as a method to indicate to the host sytem that the Auto Program/Erase algorithms are either in progress or completed.

While the Automatic Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Automatic Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the second $\overline{WE}$ pulse of the two write pulse sequences.

## DATA POLLING-DQ7

The MX28F1000 also features Data Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the compliment data of the data last written to DQ7. Upon completion of the Automatic Program algorithm an attempt to read the device will produce the true data last written to DQ7. The Data Polling feature is valid after the rising edge of the second $\overline{WE}$ pulse of the two write pulse sequences.

While the Automatic Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The Data Polling feature is valid after the rising edge of the second WE pulse of two write pulse sequences.

The Data Polling feature is active during Automatic Programming/Erasing algorithms and High-reliability Erasing.

## POWER-UP SEQUENCE

The MX28F1000 powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two-step command sequence. Power up sequence is not required.

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## ABSOLUTE MAXIMUM RATINGS

| RATING | VALUE |
|---|---|
| Ambient Operating Temperature | 0°C to 70°C |
| Storage Temperature | -65°C to 125°C |
| Applied Input Voltage | -0.5V to 7.0V |
| Applied Output Voltage | -0.5V to 7.0V |
| VCC to Ground Potential | -0.5V to 7.0V |
| A9 & VPP | -0.5V to 13.5V |

**NOTICE:**
Stresses greater than those listed under ABSOLUTE MAXI-MUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

**NOTICE:**
Specifications contained within the following tables are subject to change.

## CAPACITANCE   TA = 25°C, f = 1.0 MHz

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 14 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 16 | pF | VOUT = 0V |

## READ OPERATION
## DC CHARACTERISTICS   TA = 0°C TO 70°C, VCC = 5V ± 10%, VPP = GND to VCC

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| ILI | Input Leakage Current | | | 10 | µA | VIN = GND to VCC |
| ILO | Output Leakage Current | | | 10 | µA | VOUT = GND to VCC |
| IPP1 | VPP Current | | 1 | 100 | µA | VPP = 5.5V |
| ISB1 | Standby VCC current | | | 1 | mA | $\overline{CE}$ = VIH |
| ISB2 | | | 1 | 100 | µA | $\overline{CE}$ = VCC + 0.3V |
| ICC1 | Operating VCC current | | | 30 | mA | IOUT = 0mA, f=1MHz |
| ICC2 | | | | 50 | mA | IOUT = 0mA, f=8MHz |
| VIL | Input Low Voltage | -0.3(NOTE 1) | | 0.8 | V | |
| VIH | Input High Voltage | 2.4 | | VCC + 0.3 | V | |
| VOL | Output Low Voltage | | | 0.45 | V | IOL = 2.1mA |
| VOH | Output High Voltage | 2.4 | | | V | IOH = -400µA |

**NOTES:**

1. VIL min. = -1.0V for pulse width ≤ 50 ns.
   VIL min. = -2.0V for pulse width ≤ 20 ns.
2. VIH max. = VCC + 1.5V for pulse width ≤ 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

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## AC CHARACTERISTICS  TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = GND to VCC

| SYMBOL | PARAMETER | 28F1000-90 | | 28F1000-12 | | 28F1000-15 | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| tACC | Address to Output Delay | | 90 | | 120 | | 150 | ns | CE=OE=VIL |
| tCE | CE to Output Delay | | 90 | | 120 | | 150 | ns | OE=VIL |
| tOE | OE to Output Delay | | 35 | | 50 | | 55 | ns | CE=VIL |
| tDF | OE High to Output Float (Note1) | 0 | 20 | 0 | 30 | 0 | 35 | ns | CE=VIL |
| tOH | Address to Output hold | 0 | | 0 | | 0 | | ns | CE=OE=VIL |

**TEST CONDITIONS:**

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: ≤ 10ns
- Output load: 1 TTL gate + 100pF (Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

**NOTE:**

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

## READ TIMING WAVEFORMS
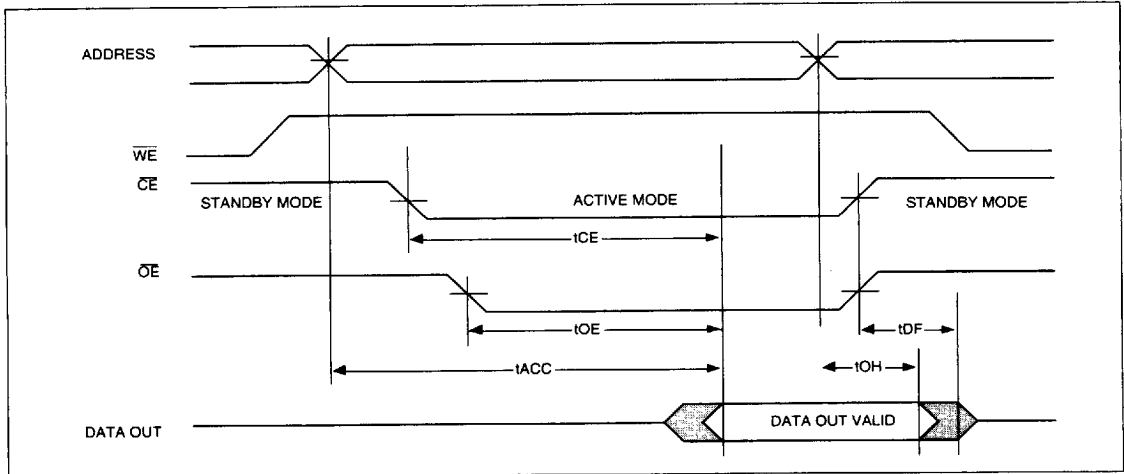
## COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

**DC CHARACTERISTICS**  TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = 12.0V ± 5%

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| ILI | Input Leakage Current | | | 10 | µA | VIN=GND to VCC |
| ILO | Output Leakage Current | | | 10 | µA | VOUT=GND to VCC |
| ISB1 | Standby VCC Current | | | 1 | mA | CE=VIH |
| ISB2 | | | 1 | 100 | µA | CE=VCC ± 0.3V |
| ICC1 (Read) | Operating VCC Current | | | 30 | mA | IOUT=0mA, f=1MHz |
| ICC2 | | | | 50 | mA | IOUT=0mA, F=8MHz |
| ICC3 (Program) | | | | 50 | mA | In Programming |
| ICC4 (Erase) | | | | 50 | mA | In Erase |
| ICC5 (Program Verify) | | | | 50 | mA | In Program Verify |
| ICC6 (Erase Verify) | | | | 50 | mA | In Erase Verify |
| IPP1 (Read) | VPP Current | | | 20 | µA | VPP=12.6V |
| IPP2 (Program) | | | | 50 | mA | In Programming |
| IPP3 (Erase) | | | | 50 | mA | In Erase |
| IPP4 (Program Verify) | | | | 50 | mA | In Program Verify |
| IPP5 (Erase Verify) | | | | 50 | mA | In Erase Verify |
| VIL | Input Voltage | -0.3 (Note 5) | | 0.8 | V | |
| VIH | | 2.4 | | VCC+0.3V (Note 6) | V | |
| VOL | Output Voltage | | | 0.45 | V | IOL=2.1mA |
| VOH | | 2.4 | | | V | IOH=-400µA |

**NOTES:**

1. VCC must be applied before VPP and remove after VPP.
2. VPP must not exceed 14V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while VPP=12V.
4. Do not alter VPP either VIL to 12V or 12V to VIL when CE=VIL.
5. VIL min. = -0.6V for pulse width ≤ 20ns.
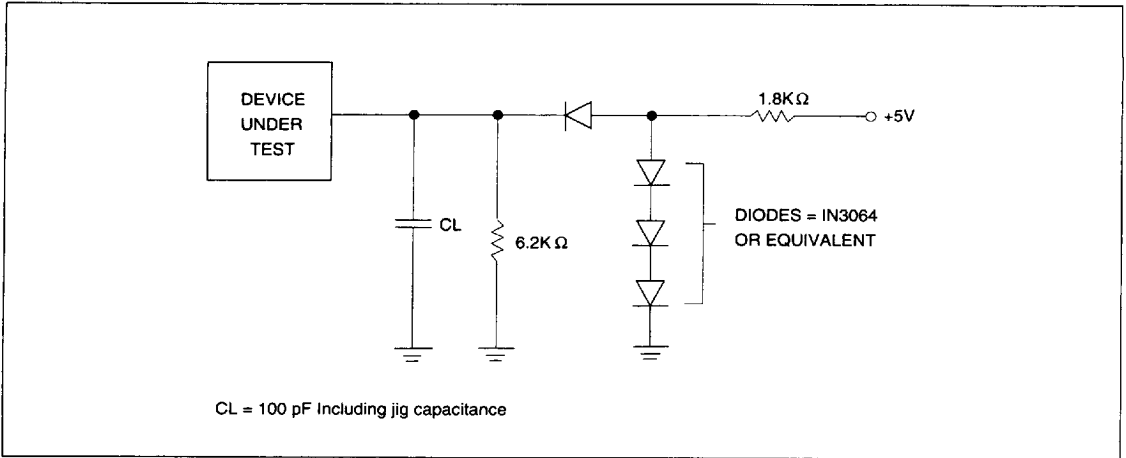6. If VIH is over the specified maximum value, programming operation cannot be guranteed.

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## AC CHARACTERISTICS  TA = 0°C to 70°C, VCC = 5V ± 10%, VPP =12V ± 5%

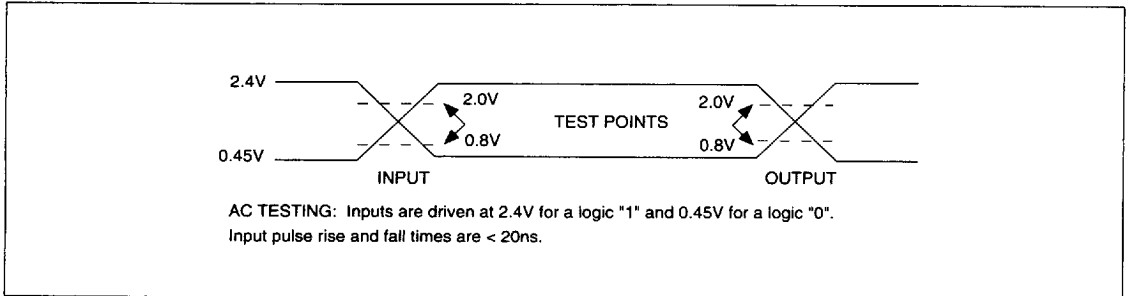| SYMBOL | PARAMETER | 28F1000-90 MIN. | MAX. | 28F1000-12 MIN. | MAX. | 28F1000-15 MIN. | MAX. | UNIT | CONTIONS |
|---|---|---|---|---|---|---|---|---|---|
| tVPS | VPP setup time | 100 | | 100 | | 100 | | ns | |
| tOES | OE setup time | 100 | | 100 | | 100 | | ns | |
| tCWC | Command programming cycle | 90 | | 120 | | 150 | | ns | |
| tCEP | WE programming pulse width | 45 | | 50 | | 60 | | ns | |
| tCEPH1 | WE programming pluse width High | 20 | | 20 | | 20 | | ns | |
| tCEPH2 | WE programming pluse width High | 100 | | 100 | | 100 | | ns | |
| tAS | Address setup time | 0 | | 0 | | 0 | | ns | |
| tAH | Address hold time | 45 | | 50 | | 60 | | ns | |
| tAH1 | Address hold time for DATA POLLING | 0 | | 0 | | 0 | | ns | |
| tDS | Data setup time | 45 | | 50 | | 50 | | ns | |
| tDH | Data hold time | 10 | | 10 | | 10 | | ns | |
| tCESP | CE setup time before DATA polling/toggle bit | 100 | | 100 | | 100 | | ns | |
| tCES | CE setup time | 0 | | 0 | | 0 | | ns | |
| tCESC | CE setup time before command write | 100 | | 100 | | 100 | | ns | |
| tCESV | CE setup time before verify | 6 | | 6 | | 6 | | µs | |
| tVPH | VPP hold time | 100 | | 100 | | 100 | | ns | |
| tDF | Output disable time (Note 3) | | 20 | | 30 | | 35 | ns | |
| tDPA | DATA polling/toggle bit access time | | 90 | | 120 | | 150 | ns | |
| tVA | Verify access time | | 90 | | 120 | | 150 | ns | |
| tAETC | Total erase time in auto chip erase | 5(TYP.) | | 5(TYP.) | | 5(TYP.) | | s | |
| tAETB | Total erase time in auto block erase | 5(TYP.) | | 5(TYP.) | | 5(TYP.) | | s | |
| tAVT | Total programming time in auto verify | 15 | 300 | 15 | 300 | 15 | 300 | µs | |
| tET | Standby time in erase | 10 | | 10 | | 10 | | ms | |
| tBALC | Block address load cycle | 0.3 | 30 | 0.3 | 30 | 0.3 | 30 | µs | |
| tBAL | Block address load time | 100 | | 100 | | 100 | | µs | |
| tCH | CE Hold Time | 0 | | 0 | | 0 | | ns | |
| tCS | CE setup to WE going low | 0 | | 0 | | 0 | | ns | |

**NOTES:**
1. CE and OE must be fixed high during VPP transition from 5V to 12V or from 12V to 5V.
2. Refer to read operation when VPP=VCC about read operation while VPP 12V.
3. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

## SWITCHING TEST CIRCUITS



DEVICE UNDER TEST

CL

6.2KΩ

1.8KΩ

+5V

DIODES = IN3064 OR EQUIVALENT

CL = 100 pF Including jig capacitance

## SWITCHING TEST WAVEFORMS



2.4V

2.0V

0.8V

TEST POINTS

2.0V

0.8V

0.45V

INPUT

OUTPUT

AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 20ns.

5688882 0000610 385

# MX28F1000

## AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are excuted automatically by internal control circuit. Programming completion can be verified by DATA polling after automatic verify

starts. Device outputs $\overline{DATA}$ during programming and DATA after programming on Q7. Q0 to Q5 (Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform) are in high impedance.
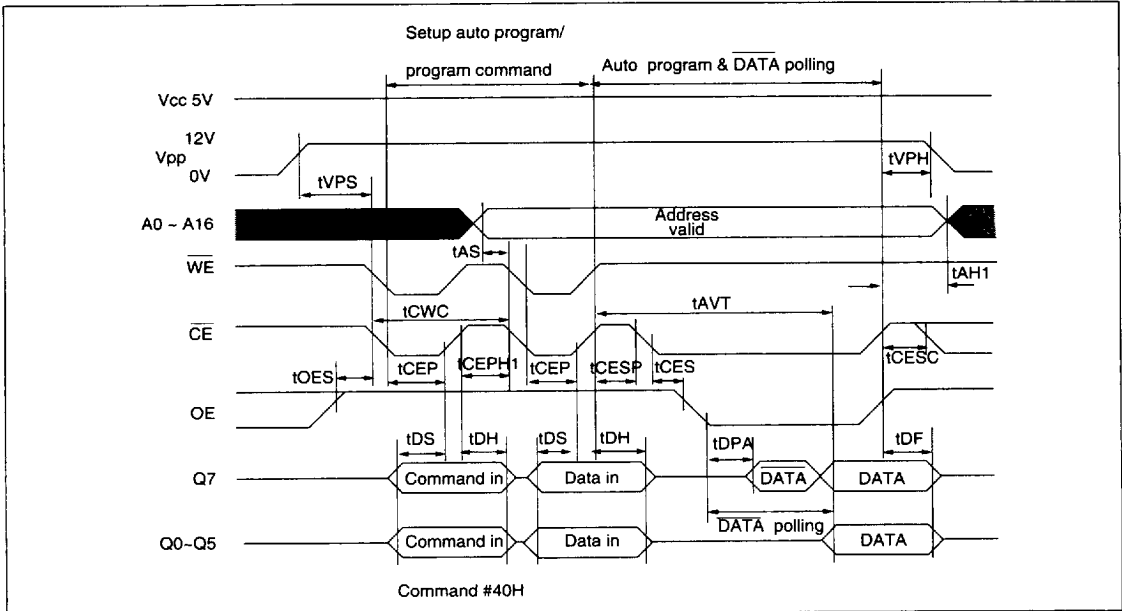




**AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART**
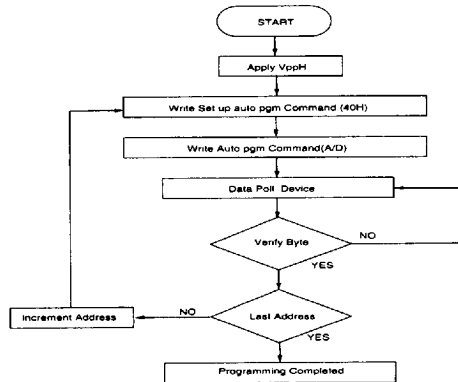
## AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verify is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling after automatic erase starts. Device out-puts 0 during erasure and 1 after erasure on Q7. Q0 to Q5 (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform) are in high impedance.





AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

5688882 0000612 158
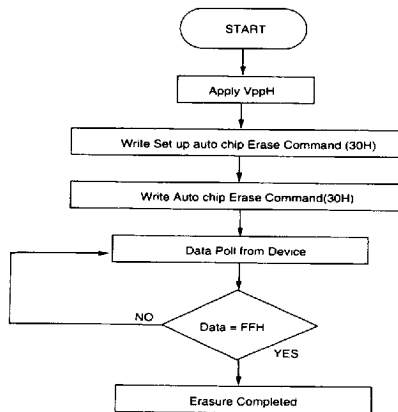
## AUTOMATIC BLOCK ERASE TIMING WAVEFORM

Block data (16Kbyte) indicated by A14 to A16 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by DATA polling after auto-matic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7. Q0 to Q5 (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform) are in high impedance.

5688882 0000613 094

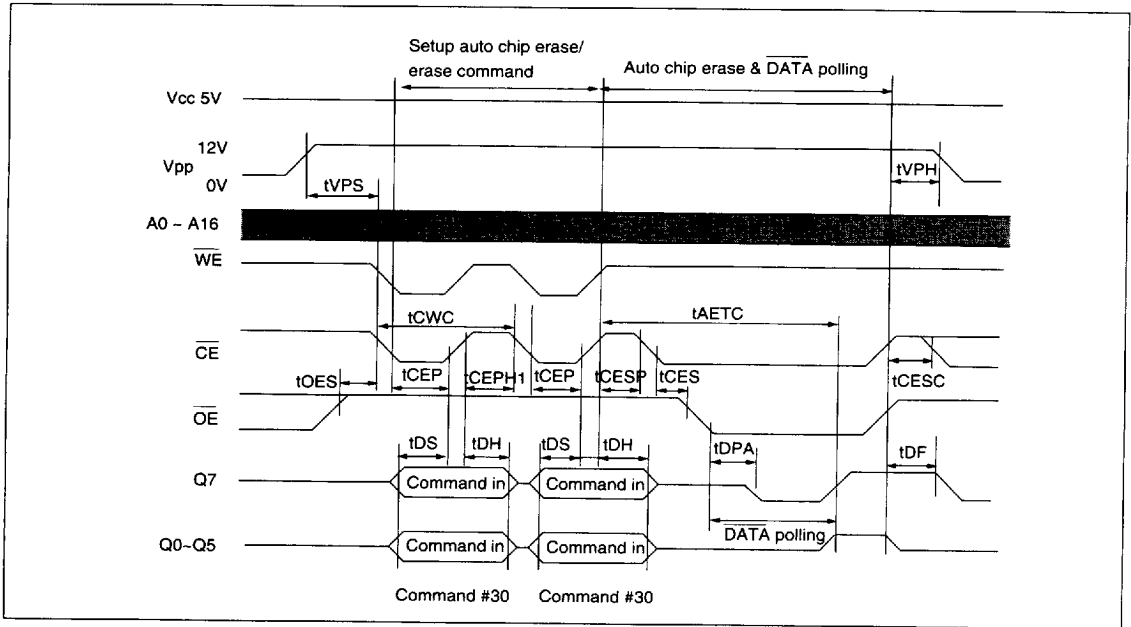**AUTOMATIC BLOCK ERASE ALGORITHM FLOWCHART**

5688882 0000614 T20

**MACRONIX, INC.**
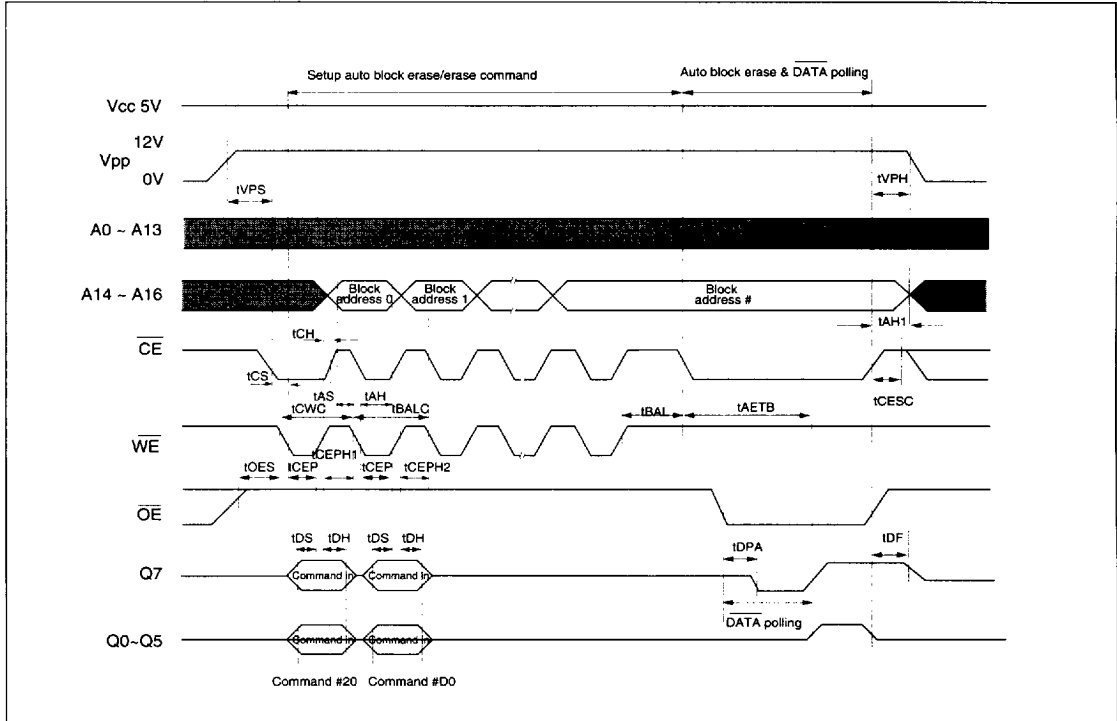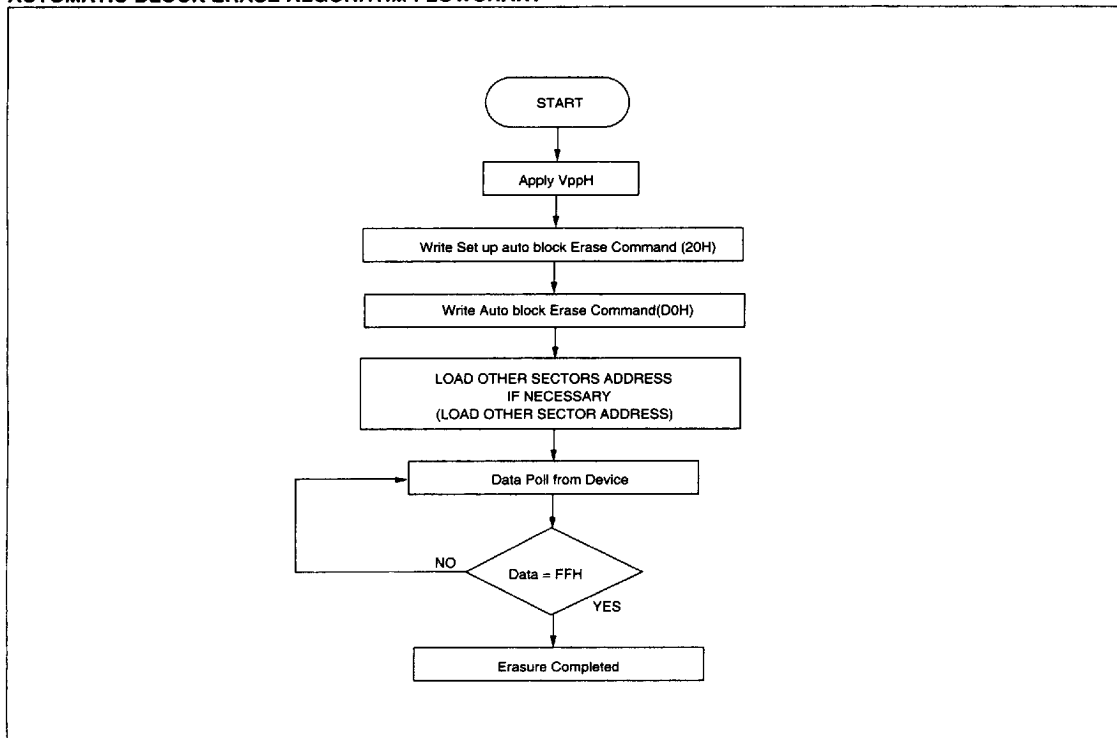
## FAST HIGH-RELIABILITY CHIP ERASE

This device can be applied the fast high-reliability chip erase algorithm shown in the following flowchart. This algorithm allows to obtain faster erase time without any voltage stress to the device nor deterioration in reliability of data.

**FAST HIGH-RELIABILITY CHIP ERASE FLOWCHART**



**CHIP ERASE FLOW**



**FLASH MEMORY**

34-19

5688882  0000615  967

**ERASE VERIFY FLOW**

5688882 0000616 8T3

## FAST HIGH-RELIABILITY CHIP ERASE TIMING WAVEFORM

All data in chip are erased. Control verification and additional erasure externally according to fast high-reliability chip erase flowchart. Successful erasure completion can be verified by $\overline{DATA}$ polling. Device outputs 0 during erasure and 1 after erasure on Q7. Q0 to Q6 are in high impedance state.
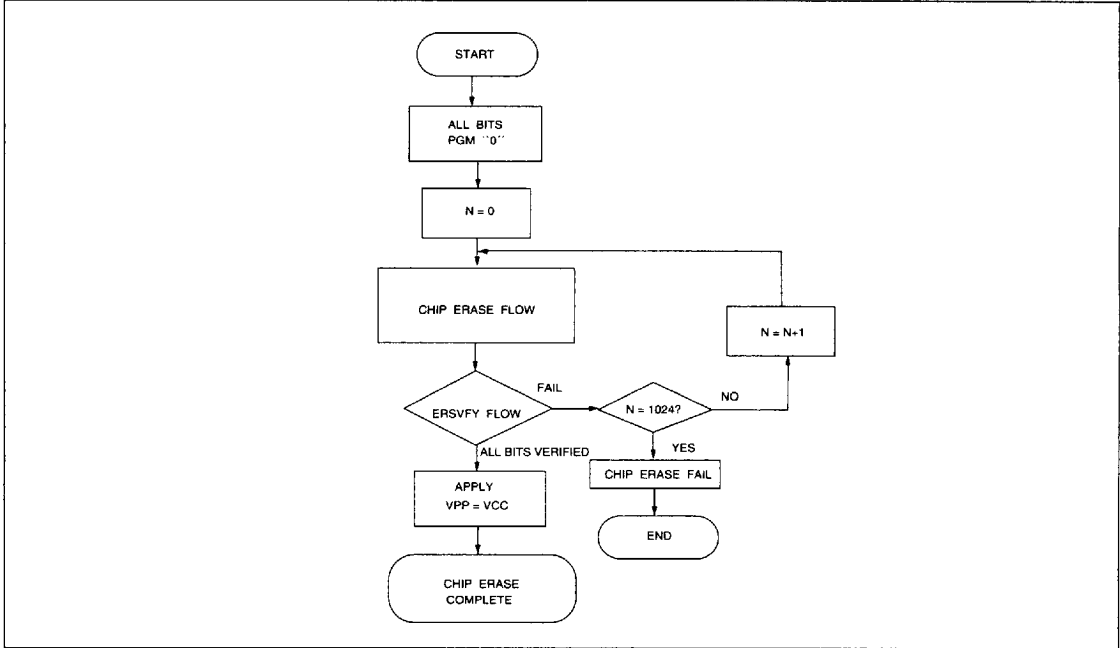
5688882 0000617 73T
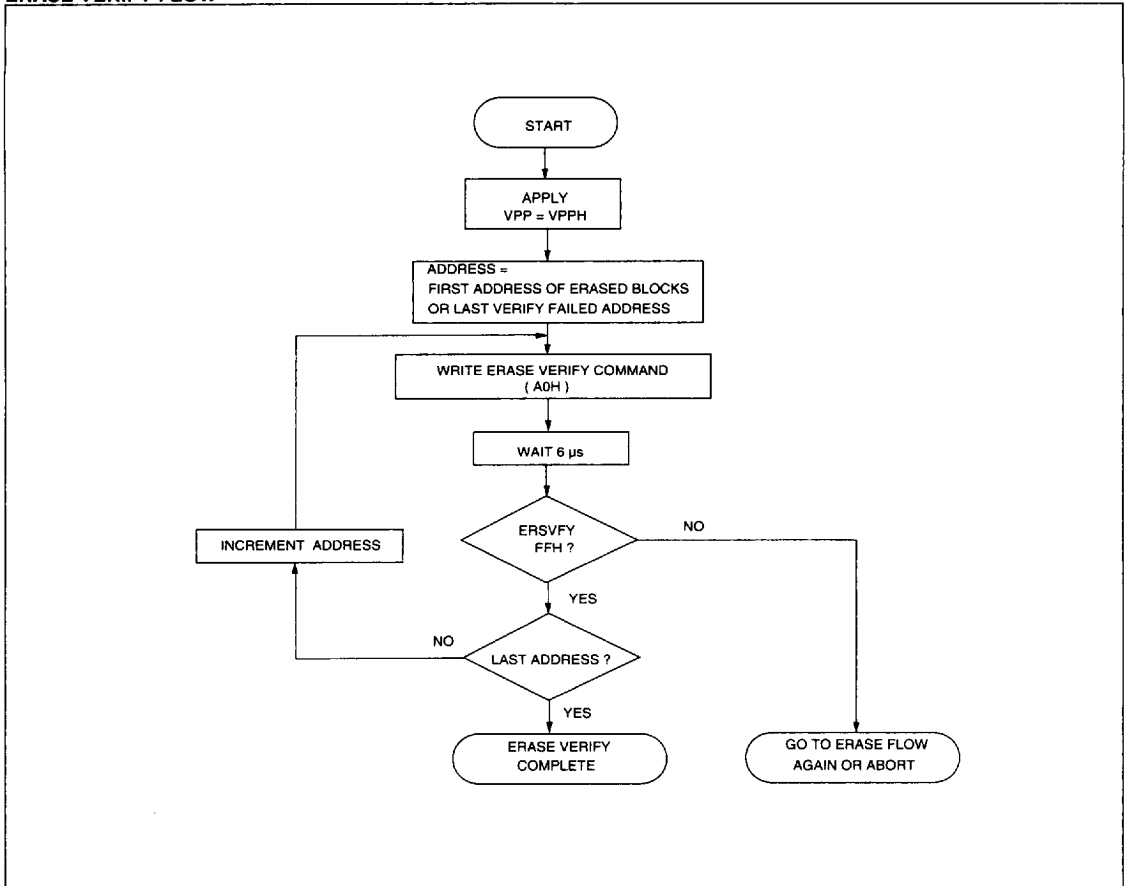
## FAST HIGH-RELIABILITY BLOCK ERASE

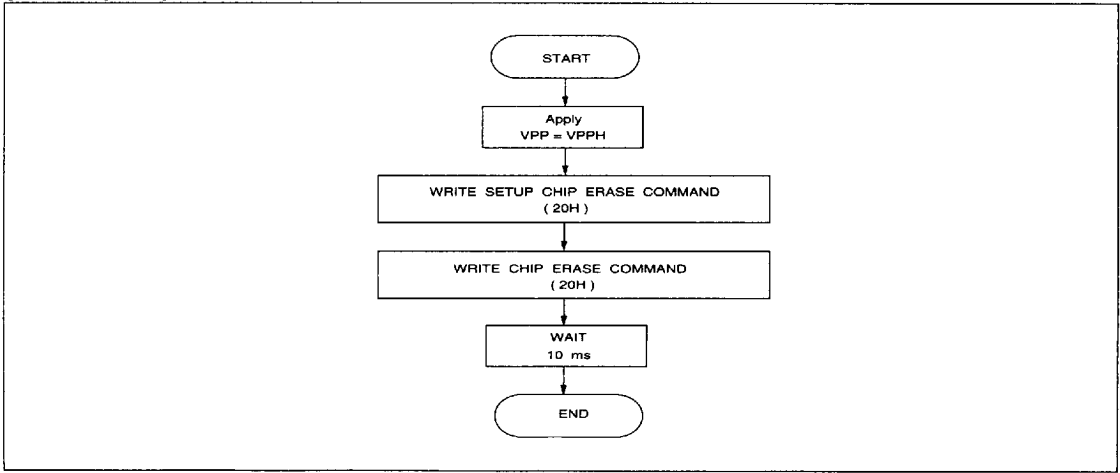This device can be applied to the fast high-reliability block erase algorithm shown in the following flowchart. This algorithm allows to obtain faster erase time by the block (16K byte x 8 block) without any voltage stress to the device nor deterioration in reliability of data.

### FAST HIGH-RELIABILITY BLOCK ERASE FLOWCHART

```
                          START

              For selected block(s),
              All bits PGM "0"

                   N = 0

           BLOCK ERASE FLOW                      N = N+1

                 FAIL
      ERSVFY FLOW ───────  N = 1024?  ──NO──┘
                                       YES
         ALL BITS VERIFIED       BLOCK ERASE FAIL

         APPLY
         VPP = VCC                   END

       BLOCK ERASE
       COMPLETE
```

### BLOCK ERASE FLOW

```
                   START

                  Apply
                VPP = VPPH

        WRITE SETUP BLOCK ERASE COMMAND
                ( 60H )

          WRITE BLOCK ERASE COMMAND
        ( LOAD FIRST SECTOR ADDRESS , 60H )

        LOAD OTHER SECTORS' ADDRESS
               IF NECESSARY
        ( LOAD OTHER SECTOR ADDRESS )

                   WAIT
                  10  ms

                   END
```

5688882 0000618 676

**ERASE VERIFY FLOW**

```
                          ┌─────────────┐
                          │    START    │
                          └──────┬──────┘
                                 │
                          ┌──────┴──────┐
                          │   APPLY     │
                          │  VPP = VPPH │
                          └──────┬──────┘
                                 │
                   ┌─────────────┴──────────────┐
                   │  ADDRESS =                  │
                   │  FIRST ADDRESS OF ERASED    │
                   │  BLOCKS OR LAST VERIFY      │
                   │  FAILED ADDRESS             │
                   └─────────────┬──────────────┘
                                 │
                   ┌─────────────┴──────────────┐
                   │  WRITE ERASE VERIFY COMMAND │
                   │        ( A0H )              │
                   └─────────────┬──────────────┘
                                 │
                          ┌──────┴──────┐
                          │  WAIT 6 µs  │
                          └──────┬──────┘
                                 │
                            ╱────┴────╲          NO
                           ╱  ERSVFY   ╲────────────────────┐
                           ╲  FFH ?    ╱                    │
                            ╲────┬────╱                     │
                                 │ YES                      │
                            ╱────┴────╲                     │
         NO                ╱           ╲                    │
   ┌──────────────────────╱ LAST ADDRESS?╲                 │
   │                       ╲             ╱                  │
   │                        ╲───────────╱                   │
   │                             │ YES                      │
┌──┴────────────┐        ┌───────┴───────┐        ┌─────────┴──────────┐
│  INCREMENT    │        │ ERASE VERIFY  │        │ GO TO ERASE FLOW   │
│  ADDRESS      │        │ COMPLETE      │        │ AGAIN OR ABORT     │
└───────────────┘        └───────────────┘        └────────────────────┘
```

■ 5688882 0000619 502 ■

## FAST HIGH-RELIABILITY BLOCK ERASE TIMING WAVEFORM

Indicated block data (16 Kbyte) are erased. Control verification and additional erasure externally according to fast high-rel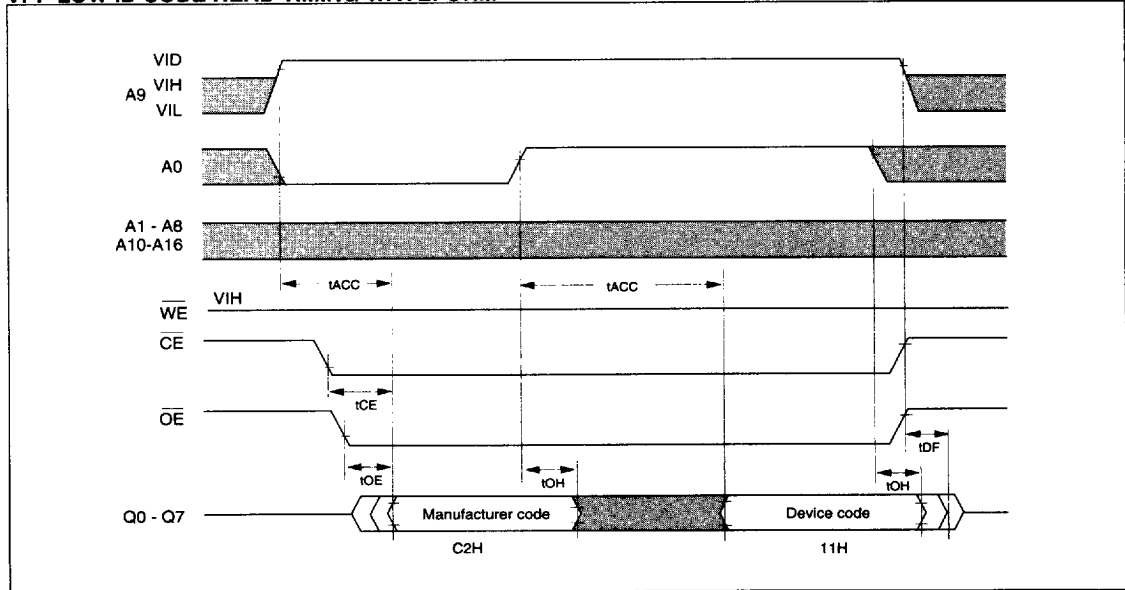iability block erase flowchart. Successful erasure completion can be verified by $\overline{\text{DATA}}$ polling. Device outputs 0 during erasure and 1 after erasure on Q7. Q0 to Q6 are in high impedance.
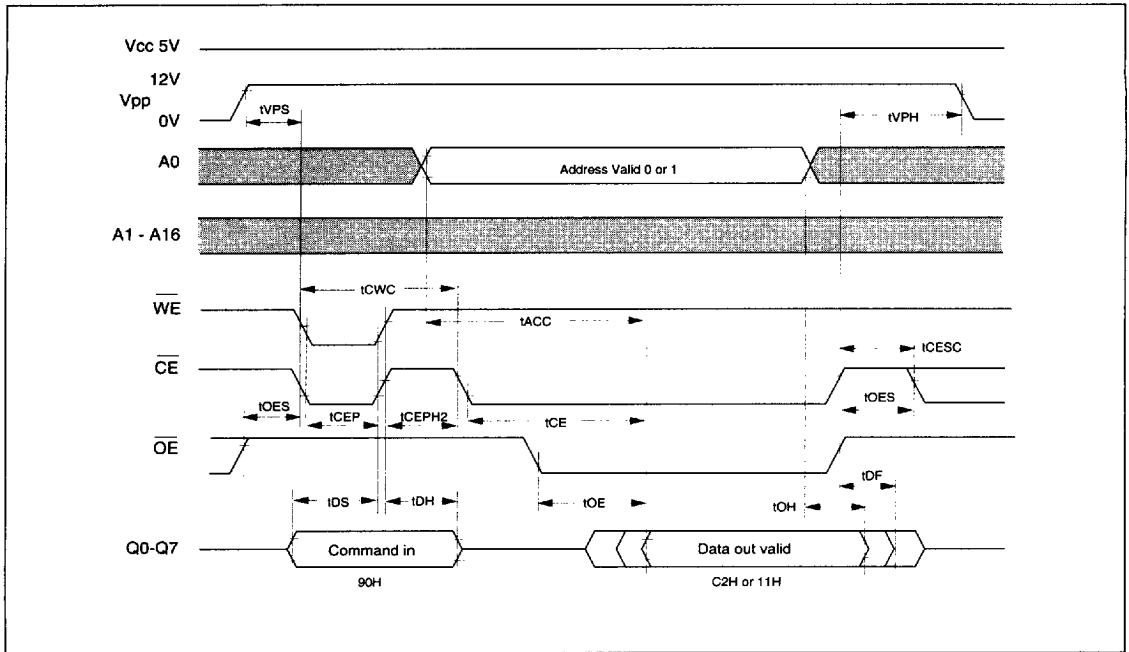
# MX28F1000
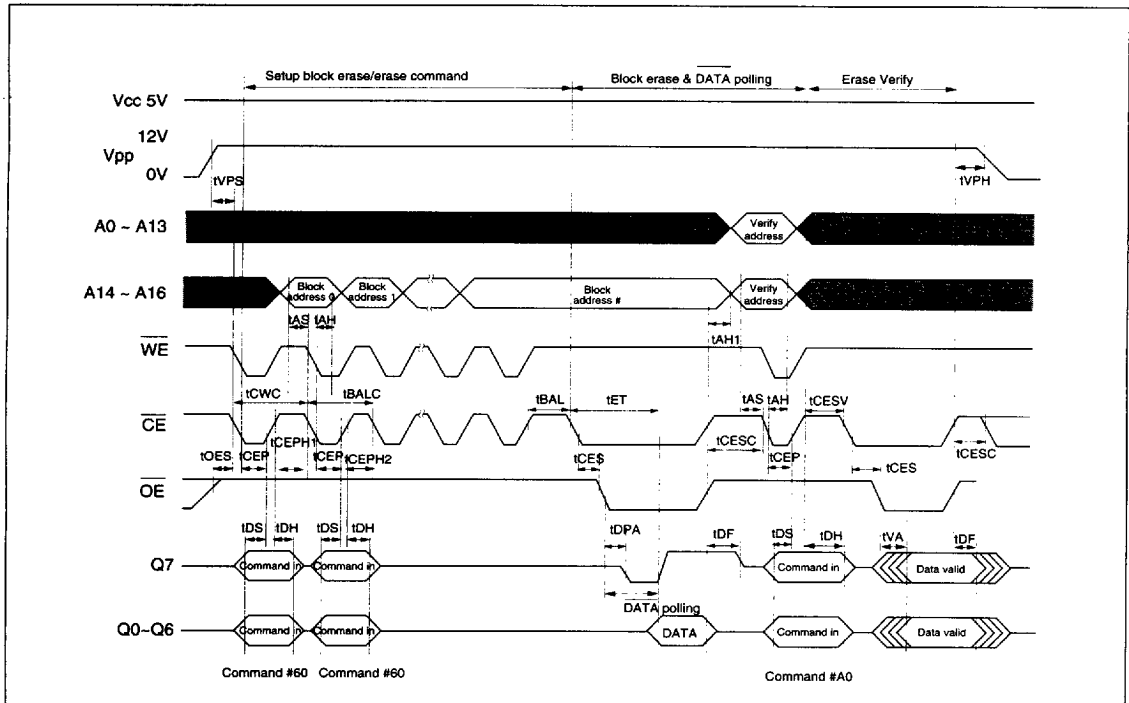
## VPP HIGH READ TIMING WAVEFORM
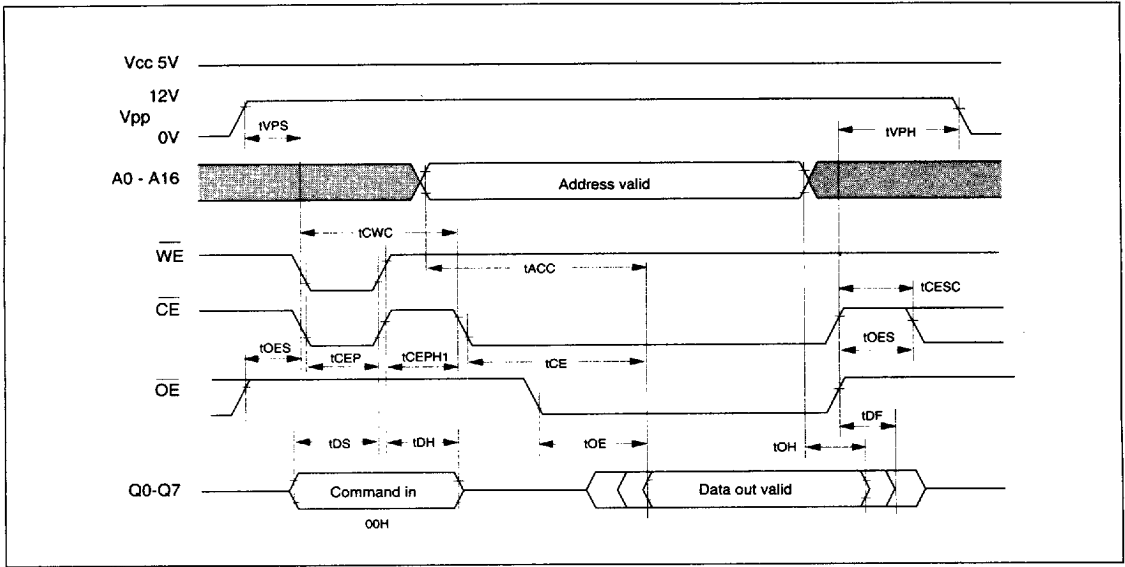


FLASH
MEMORY

## VPP LOW ID CODE READ TIMING WAVEFORM

■ 5688882 0000621 160 ■

**MACRONIX, INC.**

## VPP HIGH ID CODE READ TIMING WAVEFORM



## RESET TIMING WAVEFORM

5688882 0000622 0T7
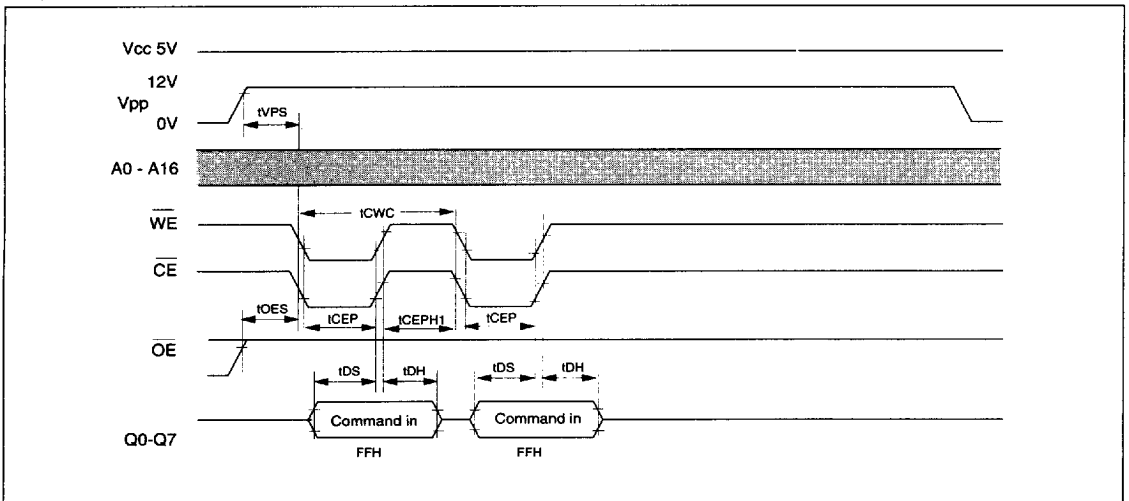
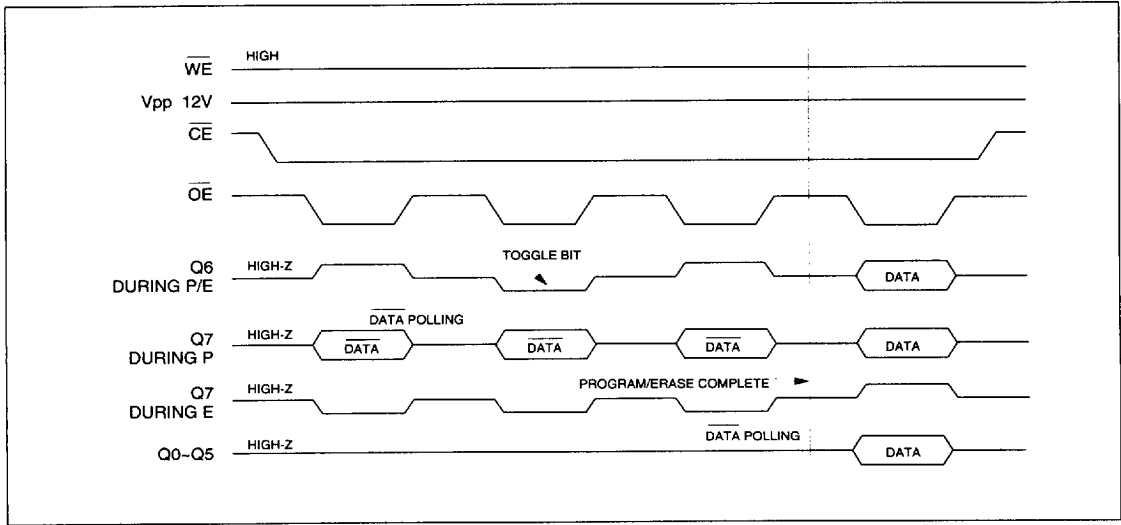## TOGGLE BIT, $\overline{\text{DATA}}$ POLLING TIMING WAVEFORM

Toggle bit appears in Q6, when program/erase is operating. DATA polling appears in Q7 during programming or erase.

5688882 0000623 T33

**MACRONIX, INC.**

## ORDERING INFORMATION

### PLASTIC PACKAGE

| PART NO. | ACCESS TIME (ns) | OPERATING CURRENT MAX.(mA) | STANDBY CURRENT MAX.(μA) | PACKAGE |
|---|---|---|---|---|
| MX28F1000MC-90 | 90 | 50 | 100 | 32 Pin SOP |
| MX28F1000MC-12 | 120 | 50 | 100 | 32 Pin SOP |
| MX28F1000MC-15 | 150 | 50 | 100 | 32 Pin SOP |
| MX28F1000PC-90 | 90 | 50 | 100 | 32 Pin DIP |
| MX28F1000PC-12 | 120 | 50 | 100 | 32 Pin DIP |
| MX28F1000PC-15 | 150 | 50 | 100 | 32 Pin DIP |
| MX28F1000QC-90 | 90 | 50 | 100 | 32 Pin PLCC |
| MX28F1000QC-12 | 120 | 50 | 100 | 32 Pin PLCC |
| MX28F1000QC-15 | 150 | 50 | 100 | 32 Pin PLCC |
| MX28F1000TC-90 | 90 | 50 | 100 | 32 Pin TSOP (Normal Type) |
| MX28F1000TC-12 | 120 | 50 | 100 | 32 Pin TSOP (Normal Type) |
| MX28F1000TC-15 | 150 | 50 | 100 | 32 Pin TSOP (Normal Type) |
| MX28F1000RC-90 | 90 | 50 | 100 | 32 Pin TSOP (Reverse Type) |
| MX28F1000RC-12 | 120 | 50 | 100 | 32 Pin TSOP (Reverse Type) |
| MX28F1000RC-15 | 150 | 50 | 100 | 32 Pin TSOP (Reverse Type) |

5688882 0000624 97T