OXFORD SEMICONDUCTOR

OX16PCI954

Integrated Quad UART and PCI interface

FEATURES

- Four 16C950 High performance UART channels
- 8/32-bit Pass-through Local Bus
- IEEE1284 EPP parallel port
- Multi-function target PCI controller, fully PCI 2.2 and PCI Power Management 1.0 compliant
- UARTs fully software compatible with 16C550-type devices.
- Baud rates up to 15Mbps in asynchronous mode and 60Mbps in external 1x clock mode
- 128-byte deep FIFO per transmitter and receiver
- Flexible clock prescaler from 1 to 31.875
- Automated in-band flow control using programmable Xon/Xoff in both directions
- Automated out-of-band flow control using CTS#/RTS# and/or DSR#/DTR#
- Arbitrary trigger levels for receiver and transmitter FIFO interrupts and automatic in-band and out-of-band flow control
- Infra-red (IrDA) receiver and transmitter operation
- 9-bit data framing as well as 5,6,7 and 8
- 12 multi-purpose IO pins which can be configured as interrupt input pins
- Can be reconfigured using optional non-volatile configuration memory (EEPROM)
- Global Interrupt Status and readable FIFO levels to facilitate implementation of efficient device drivers
- Operation via IO or memory mapping.
- Detection of bad data in the receiver FIFO
- 5.0V operation
- 160 TQFP package

DESCRIPTION

The OX16PCI954 is a single chip solution for PCI-based serial and parallel expansion add-in cards. It is a dual function PCI device, where function 0 offers four ultra-high performance OX16C950 UARTs, and function 1 is configurable to offer either an 8 bit Local Bus or a bi-directional parallel port. Serial port cards with up to 8 ports (or with 4 serial ports and a parallel port) can be designed without redefining any device or timing parameters.

Each channel in the OX16PCI954, the fastest available PC-compatible UART, offers data rates up to 15Mbps and 128-deep transmitter and receiver FIFOs. Deep FIFOs reduce CPU overhead and allow utilisation of higher data rates. Each channel is software compatible with the widely used industry-standard 16C550 devices and compatibles as well as the OX16C95x family of high performance UARTs. In addition to increased performance and FIFO size, the UARTs also provide the full set of OX16C95x enhanced features including automated in-band flow control, readable FIFO levels etc.

The efficient 32-bit, 33MHz target-only PCI interface is compliant with version 2.2 of the PCI Bus Specification and version 1.0 of PCI Power Management Specification. For applications that do not require the internal parallel port or the local Bus, card designers can assign a Subsystem Vendor ID and a Subsystem ID using 32 input pins. If the UARTs are not required, the Local Bus can be extended from 8-bit operation to a full 32-bit pass-through interface.

For full flexibility, all the default register values can be overwritten using an optional Microwire™ serial EEPROM.

To enhance device driver efficiency and reduce interrupt latency, internal UARTs have multi-port features such as shadowed FIFO fill levels, a global interrupt source register and Good-Data Status, readable in four adjacent DWORD registers visible to logical functions in IO space and memory space.

Expansion of serial cards beyond four channels is possible using the 8-bit pass-through Local Bus function. The addressable space can be increased up to 256 bytes, and divided into four chip-select regions. In 32-bit mode the bus can map up to 16kb of Memory address space. This flexible expansion scheme caters for cards with up to 20 serial ports using external 16C950, 16C952, 16C954 or compatible devices, for composite applications such as combined serial and parallel port expansion cards.

The OX16PCI954 also provides an IEEE1284 EPP parallel port which fully supports the existing Centronics interface. The parallel port can be enabled in place of the Local Bus.

PCI LOCAL BUS

Designed for Microsoft Windows NT Windows 98

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CONTENTS

1 PERFORMANCE COMPARISON

Feature	OX16PCI954	16C554 + PLX9050	16C654 + PLX9050
Internal serial channels	4	0	0
Integral 1284 EPP parallel port	yes	no	no
Multi-function PCI device	yes	no	no
Support for PCI Power Management	yes	no	no
Zero wait-state read/write operation	yes[1]	no	no
No. of available Local Bus interrupt pins	12	2	2
DWORD access to UART Interrupt Source Registers & FIFO Levels	yes	no	no
Good-Data status	yes	no	no
Full Plug and Play with external EEPROM	yes	yes	yes
Subsystem Vendor ID & Subsystem ID with no external EEPROM	yes	no	no
External 1x baud rate clock	yes	no	no
Max baud rate in normal mode	15 Mbps	115 Kbps	1.5 Mbps
Max baud rate in 1x clock mode	60 Mbps	n/a	n/a
FIFO depth	128	16	64
Sleep mode	yes	no	yes
Auto Xon/Xoff flow	yes	no	yes
Auto CTS#/RTS# flow	yes	no	yes
Auto DSR#/DTR# flow	yes	no	no
No. of Rx interrupt thresholds	128	4	4
No. of Tx interrupt thresholds	128	1	4
No. of flow control thresholds	128	n/a	4
Transmitter empty interrupt	yes	no	no
Readable status of flow control	yes	no	no
Readable FIFO levels	yes	no	no
Clock prescaler options	248	n/a	2
Rx/Tx disable	yes	no	no
Software reset	yes	no	no
Device ID	yes	no	no
9-bit data frames	yes	no	no
RS485 buffer enable	yes	no	no
Infra-red (IrDA)	yes	no	yes

Table 1: OX16PCI950 performance compared with PLX + generic UART combinations

Note 1: Zero wait-state applies only to internal UARTs

Improvements of the OX16PCI954 over discrete solutions:

Higher degree of integration:
OX16PCI954 offers four internal 16C950 high-performance UARTs and one bi-directional parallel port.

Improved access timing:
Access to internal UARTs require zero or one PCI wait states. A PCI read transaction from an internal UART can complete within five PCI clock cycles and a write transaction to an internal UART can complete within four PCI clock cycles.

Reduces interrupt latency:
OX16PCI954 offers shadowed FIFO levels and Interrupt status registers of internal UARTs, and Interrupt Status of internal UARTs and MIO pins to reduce the device driver interrupt latency.

Power management:
OX16PCI954 complies with PCI Power Management Specification 1.0 and PC98/99 Power Management specifications. Both functions offer the extended capabilities for Power Management. This achieves significant power saving by enabling device drivers to power down the PCI function and the channel clock (in power state D3). Wake-up is requested via PME# from RI in power-state D3 or any modem line and SIN in power-state D2.

Optional EEPROM:
OX16PCI954 can be reconfigured from an external EEPROM. However, this is not required in many applications as default values are provided for typical applications up to 8 serial ports, and in some cases the Subsystem ID and Subsystem Vendor ID can be set via input pins.

Multi-function device:
OX16PCI954 is a multi-function device to enable users to load individual device drivers for internal serial ports, the internal parallel port and peripheral devices connected to the Local Bus.

Quad Internal OX16C950 UARTs
OX16PCI954 contains four ultra-high performance UARTs, which can increase driver efficiency using features such as 128-byte deep transmitter & receiver FIFOs, data rates up to 60Mbps, flexible clock options, automatic flow control, programmable interrupt and flow control trigger levels and readable FIFO levels.

2 BLOCK DIAGRAM

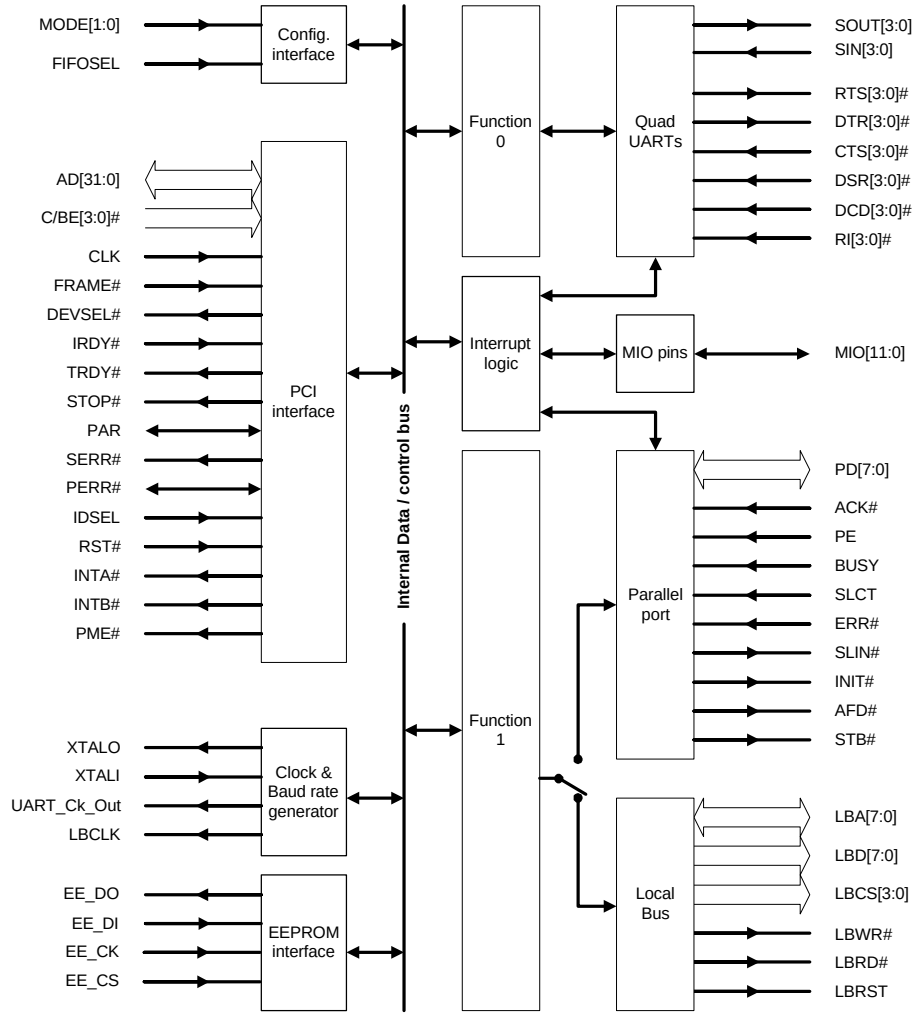
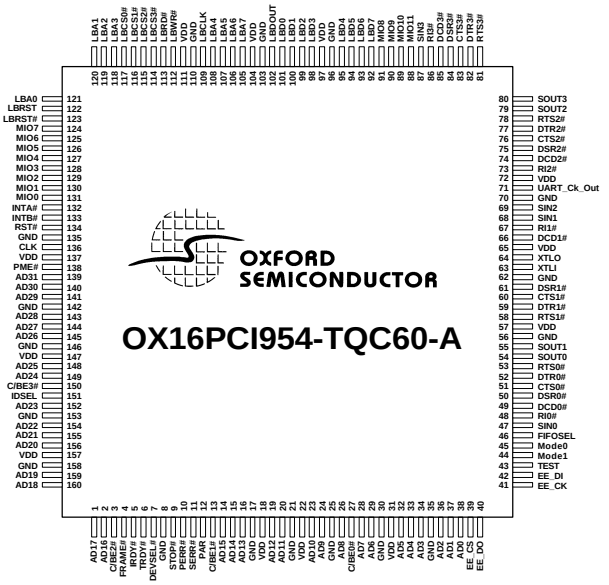


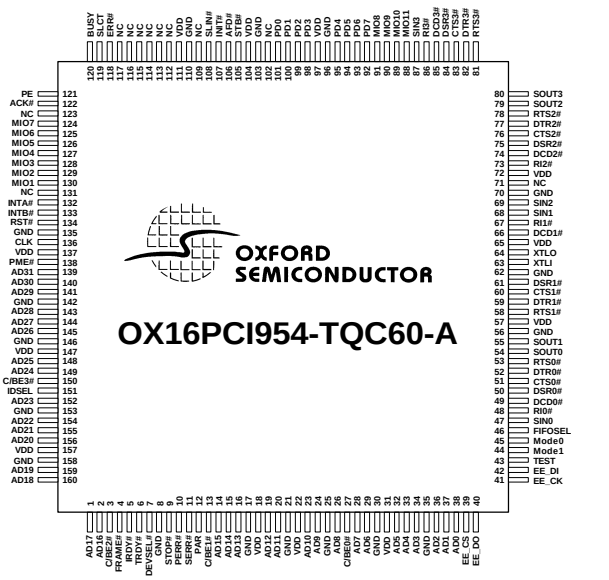
Figure 1: OX16PCI954 Block Diagram

3 PIN INFORMATION

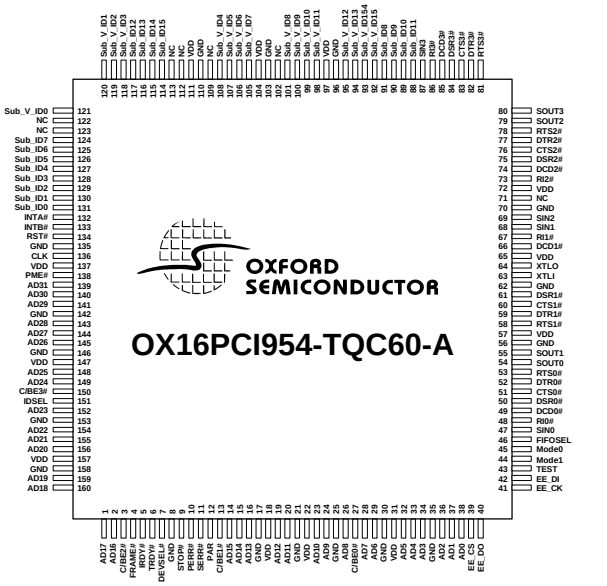
Mode '00': Quad UARTs + 8-bit local bus



Mode '01': Quad UARTs + parallel port



Mode '10': Quad UARTs + pin-assignable Subsystem ID & Subsystem Vendor ID



Mode '11': 32-bit bridge

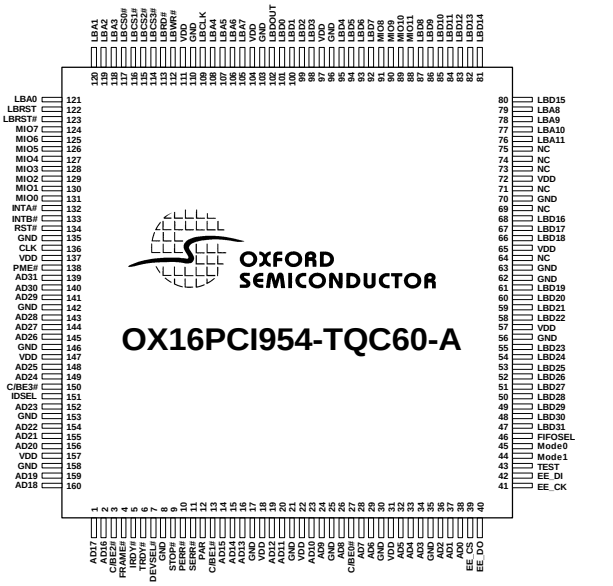


Figure 2: Pinout in all configurable modes (package = 160 TQFP)

4 PIN DESCRIPTIONS

Mode				Dir[1]	Name	Description
00	01	10	11			
PCI interface						
139, 140, 141, 143, 144, 145, 148, 149, 152, 154, 155, 156, 159, 160, 1, 2, 14, 15, 16, 19, 20, 23, 24, 26, 28, 29, 32, 33, 34, 36, 37, 38				P_I/O	AD[31:0]	Multiplexed PCI Address/Data bus
150, 3, 13, 27				P_I	C/BE[3:0]#	PCI Command/Byte enable
136				P_I	CLK	PCI system clock
4				P_I	FRAME#	Cycle Frame
7				P_O	DEVSEL#	Device Select
5				P_I	IRDY#	Initiator ready
6				P_O	TRDY#	Target ready
9				P_O	STOP#	Target Stop request
12				P_I/O	PAR	Parity
11				P_O	SERR#	System error
10				P_I/O	PERR#	Parity error
151				P_I	IDSEL	Initialization device select
134				P_I	RST#	PCI system reset
132,133				P_OD	INTA#, INTB#	PCI interrupts
138				P_OD	PME#	Power management event
Serial port pins						
46			N/A	I	FIFOSEL	FIFO select. For backward compatibility with 16C550, 16C650 and 16C750 devices the UARTs' FIFO depth is 16 when FIFOSEL is low. The FIFO size is increased to 128 when FIFOSEL is high. The unlatched state of this pin is readable by software. The FIFO size may also be set to 128 by setting FCR[5] when LCR[7] is set, or by putting the device into enhanced mode.
80, 79, 55, 54			N/A	O	SOUT[3:0]	UART serial data outputs
					IrDA_Out[3:0]	UART IrDA data output when MCR[6] of the corresponding channel is set in enhanced mode
87, 69, 68, 47			N/A	I	SIN[3:0]	UART serial data inputs
				I	IrDA_In[3:0]	UART IrDA data input when IrDA mode is enabled (see above)
85, 74, 66, 49			N/A	I	DCD[3:0]#	Active-low modem data-carrier-detect input
82, 77, 59, 52			N/A	O	DTR[3:0]#	Active-low modem data-terminal-ready output. If automated DTR# flow control is enabled, the DTR# pin is asserted and deasserted if the receiver FIFO reaches or falls below the programmed thresholds, respectively.
				O	485_En[3:0]	In RS485 half-duplex mode, the DTR# pin may be programmed to reflect the state of the the transmitter empty bit to automatically control the direction of the RS485 transceiver buffer (see register ACR[4:3])
				O	Tx_Clk_Out[3:0]	Transmitter 1x clock (baud rate generator output). For isochronous applications, the 1x (or Nx) transmitter clock may be asserted on the DTR# pins (see register CKS[5:4])

Mode				Dir[1]	Name	Description
00	01	10	11			
Serial port pins						
81, 78, 58, 53			N/A	O	RTS[3:0]#	Active-low modem request-to-send output. If automated RTS# flow control is enabled, the RTS# pin is deasserted and reasserted whenever the receiver FIFO reaches or falls below the programmed thresholds, respectively.
83, 76, 60, 51			N/A	I	CTS[3:0]#	Active-low modem clear-to-send input. If automated CTS# flow control is enabled, upon deassertion of the CTS# pin, the transmitter will complete the current character and enter the idle mode until the CTS# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the CTS# pin.
84, 75, 61, 50			N/A	I	DSR[3:0]#	Active-low modem data-set-ready input. If automated DSR# flow control is enabled, upon deassertion of the DSR# pin, the transmitter will complete the current character and enter the idle mode until the DSR# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the DSR# pin
				I	Rx_Clk_In[3:0]	External receiver clock for isochronous applications. The Rx_Clk_In is selected when CKS[1:0] = '01'.
86, 73, 67, 48			N/A	I	RI[3:0]#	Active-low modem Ring-Indicator input
				I	Tx_Clk_In[3:0]	External transmitter clock. This clock can be used by the transmitter (and indirectly by the receiver) when CKS[6]='1'.
64			N/A	O	XTLO	Crystal oscillator output
63			N/A	I	XTLI	Crystal oscillator input or external clock pin. Maximum frequency 60MHz
8-bit local bus						
71	N/A		See 32-bit Local bus	O	UART_Clk_Out	Buffered crystal output. This clock can drive external UARTs connected to the local bus. Can be enabled / disabled by software.
122	N/A			O	LBRST	Local bus active-high reset
123	N/A			O	LBRST#	Local bus active-low reset
102		N/A		O	LBDOUT	Local bus data out enable. This pin can be used by external transceivers; it is high when LBD[7:0] are in output mode and low when they are in input mode.
109	N/A			O	LBCLK	Buffered PCI clock. Can be enabled / disabled by software
114-7	N/A			O	LBCS[3:0]#	Local bus active-low Chip-Select (Intel mode)
				O	LBDS[3:0]#	Local bus active-low Data-Strobe (Motorola mode)
112	N/A			O	LBWR#	Local Bus active-low write-strobe (Intel mode)
				O	LBRDWR#	Local Bus Read-not-Write control (Motorola mode)
113	N/A			O	LBRD#	Local Bus active-low read-strobe (Intel mode)
				Z	Hi-Z	Permanent high impedance (Motorola mode)
105-8 118-21	N/A			O	LBA[7:0]	Local bus address signals
92-5 98-101	N/A			I/O	LBD[7:0]	Local bus data signals

Mode				Dir[1]	Name	Description
00	01	10	11			
Parallel port						
N/A	122	N/A		I	ACK#	Acknowledge (SPP mode). ACK# is asserted (low) by the peripheral to indicate that a successful data transfer has taken place.
				I	INTR#	Identical function to ACK# (EPP mode).
N/A	121	N/A		I	PE	Paper Empty. Activated by printer when it runs out of paper.
N/A	120	N/A		I	BUSY	Busy (SPP mode). BUSY is asserted (high) by the peripheral when it is not ready to accept data
				I	WAIT#	Wait (EPP mode). Handshake signal for interlocked IEEE 1284 compliant EPP cycles.
N/A	108	N/A		OD	SLIN#	Select (SPP mode). Asserted by host to select the peripheral
				O	ADDRSTB#	Address strobe (EPP mode) provides address read and write strobe
N/A	119	N/A		I	SLCT	Peripheral selected. Asserted by peripheral when selected.
N/A	118	N/A		I	ERR#	Error. Held low by the peripheral during an error condition.
N/A	107	N/A		OD	INIT#	Initialize (SPP mode). Commands the peripheral to initialize.
				O	INIT#	Initialize (EPP mode). Identical function to SPP mode.
N/A	106	N/A		OD	AFD#	Auto Feed (SPP mode, open-drain)
				O	DATASTB#	Data strobe (EPP mode) provides data read and write strobe
N/A	105	N/A		OD	STB#	Strobe (SPP mode). Used by peripheral to latch data currently available on PD[7:0]
				O	WRITE#	Write (EPP mode). Indicates a write cycle when low and a read cycle when high
N/A	Bus	N/A		I/O	PD[7:0]	Parallel data bus
32-bit Local bus						
See 8-bit local bus	N/A	122		O	LBRST	Local bus active-high reset
	N/A	123		O	LBRST#	Local bus active-low reset
	N/A	102		O	LBDOUT	Local bus data out enable. This pin can be used by external transceivers; it is high when LBD[7:0] are in output mode and low when they are in input mode.
	N/A	109		O	LBCLK	Buffered PCI clock. Can be enabled / disabled by software
	N/A	114-7		O	LBCS[3:0]#	Local bus active-low Chip-Select (Intel mode)
				O	LBDS[3:0]#	Local bus active-low Data-Strobe (Motorola mode)
	N/A	112		O	LBWR#	Local Bus active-low write-strobe (Intel mode)
				O	LBRDWR#	Local Bus Read-not-Write control (Motorola mode)
	N/A	113		O	LBRD#	Local Bus active-low read-strobe (Intel mode)
				Z	Hi-Z	Permanent high impedance (Motorola mode)
	N/A	76-9, 105-8, 118-121		O	LBA[12:0]	Local bus address signals
	N/A	47-55, 58-61, 66-68, 80-87, 92-95,98-101		I/O	LBD[31:0]	Local bus data signals

Mode				Dir[1]	Name	Description
00	01	10	11			
Subsystem ID & Subsystem Vendor ID pins						
N/A		N/A		I	Sub_ID[15:0]	Subsystem ID. After reset the subsystem ID of Function 0 will default to the value assigned to these pins
N/A		N/A		I	Sub_V_ID[15:0]	Subsystem Vendor ID. After reset the subsystem vendor ID of Function 0 will default to the value assigned to these pins.
Multi-purpose & External interrupt pins						
131	N/A	N/A	131	I/O	MIO0	Multi-purpose I/O 0. Can drive high or low, or assert a PCI interrupt
N/A	131	N/A	N/A	Z	Hi-Z	Permanent high impedance
130	130	N/A	130	I/O	MIO1	Multi-purpose I/O 1. Can drive high or low, or assert a PCI interrupt
				Z	Hi-Z	Permanent high-impedance when LCC[6:5] ≠ '00'
129	129	N/A	129	I/O	MIO2	Multi-purpose I/O 2. When LCC[7] = 0, this pin can drive high or low, or assert a PCI interrupt.
				I	PME_In	Input power management event. When LCC[7] is set this input pin can assert a function 1 PME#
124-128 88-91		N/A	124-8, 88-91	I/O	MIO[3:11]	Multi-purpose I/O pins. Can drive high or low, or assert a PCI interrupt
EEPROM pins						
41				O	EE_CK	EEPROM clock
39				O	EE_CS	EEPROM active-high Chip Select
42				IU	EE_DI	EEPROM data in. When the serial EEPROM is connected, this pin should be pulled up using 1-10k resistor. When the EEPROM is not used the internal pullup is sufficient.
40				O	EE_DO	EEPROM data out.
Miscellaneous pins						
43				IU	TEST	Must be connected to GND
44,45				I	Mode[1:0]	Mode selector: 00: Function 0 is Quad UART, Function 1 is 8-bit local bus 01: Function 0 is Quad UART, Function 1 is parallel port 10: Function 0 is Quad UART, Function 1 is unusable as the local bus pins are used to assign Subsystem ID and Subsystem Vendor ID to function 0 11: Function 0 is unusable, Function 1 is 32-bit local bus
Power and ground[2]						
18, 31, 57, 72, 97, 111, 147, 157				V	AC VDD	Supplies power to output buffers in switching (AC) state
22, 65, 104, 137				V	DC VDD	Power supply. Supplies power to core logic, input buffers and output buffers in steady state
8, 17, 25, 30, 35, 56, 70, 96, 110, 142, 146, 153, 158				G	AC GND	Supplies GND to output buffers in switching (AC) state
21, 62, 103, 135				G	DC GND	Ground (0 volts). Supplies GND to core logic, input buffers and output buffers in steady state

Table 2: Pin Descriptions

Note 1: Direction key:

I	Input	P_I	PCI input
IU	Input with internal pull-up	P_O	PCI output
O	Output	P_I/O	PCI bi-directional
I/O	Bi-directional	P_OD	PCI open drain
OD	Open drain		
NC	No connect	G	Ground
Z	High impedance	V	5.0V power

Note 2: Power & Ground

There are two GND and two VDD rails internally. One set of rails supply power and ground to output buffers while in switching state (called AC power) and another rail supply the core logic, input buffers and output buffers in steady-state (called DC rail). The rails are not connected internally. This precaution reduces the effects of simultaneous switching outputs and undesirable RF radiation from the chip. Further precaution is taken by segmenting the GND and VDD AC rails to isolate the PCI, Local Bus and UART pins.

5 CONFIGURATION & OPERATION

The OX16PCI954 is a multi-function, target-only PCI device, compliant with the PCI Local Bus Specification, Revision 2.2 and PCI Power Management Specification, Revision 1.0.

The OX16PCI954 affords maximum configuration flexibility by treating the internal UARTs, Local bus and the parallel port as separate logical functions. Each function has its own configuration space and is therefore recognised and configured by the PCI BIOS seperately. The functions used are configured by the Mode[1:0] pins as shown in Table 3.

The OX16PCI954 is configured by system start-up software during the bootstrap process that follows bus reset. The system scans the bus and reads the vendor and device identification codes from any devices it finds. It then loads device-driver software according to this information and configures the I/O, memory and interrupt resources. Device drivers can then access the functions at the assigned addresses in the usual fashion, with the improved data throughput provided by PCI.

Each function operates as though it was a separate device; however there are a set of Local configuration registers that can be used to enable signals and interrupts, configure timings, and improve the efficiency of multi-port drivers. This architecture enables separate drivers to be installed for each function. Generic port drivers can be hooked to use the functions individually, or more efficient multi-port drivers can hook both functions, accessing the Local Configuration Registers from either.

All registers default after reset to suitable values for typical applications such a 4/8 port serial, or combo 4-port serial/1-port parallel add-in cards. However, all identification, control and timing registers can be redefined using an optional serial EEPROM.

Mode [1:0]	Configuration
00	Function 0 is Quad UART, Function 1 is 8-bit local bus
01	Function 0 is Quad UART, Function 1 is parallel port
10	Function 0 is Quad UART, Function 1 is unusable as the local bus pins are used to assign Subsystem ID and Subsystem Vendor ID to function 0
11	Function 0 is unusable, Function 1 is 32-bit local bus

Table 3: Mode configuration

6 PCI TARGET CONTROLLER

6.1 Operation

The OX16PCI954 responds to the following PCI transactions:-

- Configuration access: The OX16PCI954 responds to type 0 configuration reads and writes if the IDSEL signal is asserted and the bus address is selecting the configuration registers for function 0 or 1. The device will respond to the configuration transaction by asserting DEVSEL#. Data transfer then follows. Any other configuration transaction will be ignored by the OX16PCI954.

- IO reads/writes: The address is compared with the addresses reserved in the I/O Base Address Registers (BARs). If the address falls within one of the assigned ranges, the device will respond to the IO transaction by asserting DEVSEL#. Data transfer follows this address phase. For the UARTs and 8-bit Local Bus controller, only byte accesses are possible. For IO accesses to these regions, the controller compares AD[1:0] with the byte-enable signals as defined in the PCI specification. The access is always completed; however if the correct BE signal is not present the transaction will have no effect

- Memory reads/writes: These are treated in the same way as I/O transactions, except that the memory ranges are used. Memory access to single-byte regions is always expanded to DWORDs in the OX16PCI954. In other words, OX16PCI954 reserves a DWORD per byte in single-byte regions. The device allows the user to define the active byte lane using LCC[4:3] so that in Big-Endian systems the hardware can swap the byte lane automatically. For Memory mapped access in single-byte regions, the OX16PCI954 compares the asserted byte-enable with the selected byte-lane in LCC[4:3] and completes the operation if a match occurs, otherwise the access will complete normally on the PCI bus, but it will have no effect on either the internal UARTs or the local bus controller.

- All other cycles (64-bit, special cycles, reserved encoding etc.) are ignored.

The OX16PCI954 will complete all transactions as disconnect-with-data, ie the device will assert the STOP# signal alongside TRDY#, to ensure that the Bus Master does not continue with a burst access. The exception to this is Retry, which will be signalled in response to any access while the OX16PCI954 is reading from the serial EEPROM.

The OX16PCI954 performs medium-speed address decoding as defined by the PCI specification. It asserts the DEVSEL# bus signal two clocks after FRAME# is first sampled low on all bus transaction frames which address the chip. The internal UARTs are accessed with zero wait states inserted. Fast back-to-back transactions are supported by the OX16PCI954 as a target, so a bus master can perform faster sequences of write transactions to the UARTs or local bus when an inter-frame turn-around cycle is not required.

The device supports any combination of byte-enables to the PCI Configuration Registers, the Local Configuration registers (see Base Address 2 and 3) and the Local Bus controller in 32-bit mode. If a byte-enable is not asserted, that byte is unaffected by a write operation and undefined data is returned upon a read.

The OX16PCI954 performs parity generation and checking on all PCI bus transactions as defined by the standard. Note this is entirely unrelated to serial data parity which is handled within the UART functional modules themselves. If a parity error occurs during the PCI bus address phase, the device will report the error in the standard way by asserting the SERR# bus signal. However if that address/command combination is decoded as a valid access, it will still complete the transaction as though the parity check was correct.

The OX16PCI954 does not support any kind of caching or data buffering in addition to that already provided within the UARTs by the transmit and receive data FIFOs. In general, registers in the UARTs and on the local bus can not be pre-fetched because there may be side-effects on read.

6.2 Configuration space

The OX16PCI954 is a dual-function device, where each logical function has its own configuration space. All required fields in the standard header are implemented, plus the Power Management Extended Capability register set. The format of the configuration space is shown in Table 4 overleaf.

In general, writes to any registers that are not implemented are ignored, and all reads from unimplemented registers return 0.

6.2.1 PCI Configuration Space Register map

Configuration Register Description 31	16	15	0	Offset Address
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST[1]	Header Type	Reserved	Reserved	0Ch
Base Address Register 0 (BAR0)				10h
Base Address Register 1 (BAR 1)				14h
Base Address Register 2 (BAR 2) – Local Configuration Registers in IO space				18h
Base Address Register 3 (BAR3) – Local Configuration Registers in Memory space				1Ch
Reserved				20h
Reserved				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Reserved			Cap_Ptr	34h
Reserved				38h
Reserved	Reserved	Interrupt Pin	Interrupt Line	3Ch
Power Management Capabilities (PMC)		Next Ptr	Cap_ID	40h
Reserved	Reserved	PMC Control/Status Register (PMCSR)		44h

Table 4: PCI Configuration space

Register name	Reset value						Program read/write	
	Function 0		Function 1				EEPROM	PCI
	UARTs	Disabled	8-bit bus	32-bit bus	parallel port	Disabled		
Vendor ID	0x1415		0x1415				W	R
Device ID	0x9501	0x9500	0x9511	0x9512	0x9513	0x9510	W	R
Command	0x0000		0x0000				-	R/W
Status	0x0290		0x0290				W (bit 4)	R/W
Revision ID	0x00		0x00				-	R
Class code	0x070006		0x068000	0x068000	0x070101	0x068000	W	R
Header type	0x80		0x80				-	R
BAR 0	0x00000001		0x00000001				-	R/W
BAR 1	0x00000000		0x00000000		00000001	00000000	-	R/W
BAR 2	0x00000001		0x00000001				-	R/W
BAR 3	0x00000000		0x00000000				-	R/W
Subsystem VID	0x1415		0x1415				W	R
Subsystem ID	0x0000		0x0000				W	R
Cap ptr.	0x40		0x40				-	R
Interrupt line	0x00		0x00				-	R/W
Interrupt pin	0x01		0x02				W	R
Cap ID	0x01		0x01				-	R
Next ptr.	0x00		0x00				-	R
PM capabilities	0x6C01		0x6C01				W	R
PMC control/ status register	0x0000		0x0000				-	R/W

Table 5: PCI configuration space default values

6.3 Accessing logical functions

Access to the UARTs, local bus and parallel port is achieved via standard I/O and memory mapping, at addresses defined by the Base Address Registers (BARs) in configuration space. The BARs are configured by the system to allocate blocks of I/O and memory space to the logical functions, according to the size required by the function. The addresses allocated can then be used to access the functions. The mapping of these BARs is shown inTable 6.

BAR	Function 0	Function 1	
		Local bus	Parallel port
0	Internal UARTs (I/O mapped)	Local bus (I/O mapped)	Parallel port base registers
1	Internal UARTs (memory mapped)	Local bus (memory mapped)	Parallel port extended registers
2	Local configuration registers (I/O mapped)		
3	Local configuration registers (memory mapped)		
4	Unused		
5	Unused		

Table 6: Base Address Register definition

6.3.1 PCI access to internal UARTs

IO and memory space

BAR 0 and BAR 1 of function 0 are used to access the internal UARTs. The function reserves a 32-byte block of I/O space and a 4K byte block of memory space. Once the I/O access enable and Memory access enable bits in the Command register (configuration space) are set, the UARTs can be accessed following the mapping shown in Table 7.

UART Address (hex)	PCI Offset from Base Address 0 for Function0 in IO space (hex)			
	UART0	UART1	UART2	UART3
000	00	08	10	18
001	01	09	11	19
002	02	0A	12	1A
003	03	0B	13	1B
004	04	0C	14	1C
005	05	0D	15	1D
006	06	0E	16	1E
007	07	0F	17	1F
UART Address	**PCI Offset from Base Address 1 for Function0 in Memory space (hex)**			
000	00	20	40	60
001	04	24	44	64
002	08	28	48	68
003	0C	2C	4C	6C
004	10	30	50	70
005	14	34	54	74
006	18	38	58	78
007	1C	3C	5C	7C

Table 7: PCI address map for internal UARTs (I/O and memory)

Note 1: Since 4K of memory space is reserved and the full bus address is not used for decoding, there are a number of aliases of the UARTs in the allocated memory region

6.3.2 PCI access to 8-bit local bus

When the local bus is enabled (Mode 00), access to the bus works in similar fashion to the internal UARTs. The function reserves a block of I/O space and a block of memory space. The I/O block size is user definable in the range of 4 to 256 bytes; the memory range is fixed at 4K bytes.

I/O space

In order to minimise the usage of IO space, the block size for BAR0 of Function1 is user definable in the range of 4 to 256 bytes. Having assigned the address range, the user can define two adjacent address bits to decode up to four chip selects internally. This facility allows glueless implementation of the local bus connecting to four external peripheral chips. The address range and the lower address bit for chip-select decoding (Lower-Address-CS-Decode) are defined in the Local Bus Configuration register (see LT2[26:20] in section 6.4).

The 8-bit Local Bus has eight address lines (LBA[7:0]) which correspond to the maximum IO address space. If the maximum allowable block size is allocated to the IO space (i.e. 256 bytes), then as access in IO space is byte aligned, LBA[7:0] equal PCI AD[7:0] respectively. When the user selects an address range which is less than 256 bytes, the corresponding upper address lines will be set to logic zero.

The region can be divided into four chip-select regions when the user selects the second uppermost non-zero address bit for chip-select decoding. For example if 32-bytes of IO space are reserved, the local bus address lines A[4:0] are active and the remaining address lines are set to zero. To generate four chip-selects the user should select A3 as the Lower-Address-CS-Decode. In this case A[4:3] will be used internally to decode chip-selects, asserting LBCS0# when the address offset is 00-07h, LBCS1# when

offset is 08-0Fh, LBCS2# when offset is 10-17h, and LBCS3# when offset is 18- 1Fh.

The region can be divided into two chip-select regions by selecting the uppermost address bit to decode chip selects. In the above example, the user can select A4 as the Lower-Address-CS-Decode, thus using A[5:4] internally to decode chip selects. As in this example LBA5 is always zero, only chip-select lines LBCS0# and LBCS1# will be decoded into, asserting LBCS0# when address offset is 00-0Fh and LBCS1# when offset is 10-1Fh.

The region can be allocated to a single chip-select region by assigning an address bit beyond the selected range to Lower-Address-CS-Decode (but not above A8). In the above example, if the user selects A5 as the Lower-Address-CS-Decode, A[6:5] will be used to internally decode chip-selects. As in this example LBA[7:5] are always zero, only the chip select line LBCS0# may be selected. In this case address offset 00-1Fh asserts LBCS0# and the other chip-select lines remain inactive permanently.

With default values, the address map for local bus IO address accesses is the same as for internal UARTs.

Memory Space:
The memory base address registers have an allocated fixed size of 4K bytes in the address space. Since the Local Bus has 8 address lines and the OX16PCI954 only implements DWORD aligned accesses in memory space, the 256 bytes of addressable space per chip select is expanded to 1K. Unlike an I/O access, for a memory access the upper address lines are always active and the internal chip-select decoding logic ignores the user setting for Lower-Address-CS-Decode (LT2[26:23]) and uses PCI AD[11:10] to decode into 4 chip-select regions. When the Local Bus is accessed in memory space, A[9:2] are asserted on LBA[7:0]. The chip-select regions are defined below.

Local Bus Chip-Select (Data-Strobe)	PCI Offset from BAR 1 in Function1 (Memory space)	
	Lower Address	Upper Limit
LBCS0# (LBDS0#)	000h	3FCh
LBCS1# (LBDS1#)	400h	7FCh
LBCS2# (LBDS2#)	800h	BFCh
LBCS3# (LBDS3#)	C00h	FFCh

Table 8: PCI address map for local bus (memory)

Note: The description given for I/O and memory accesses is for an Intel-type configuration for the Local Bus. For Motorola-type configuration, the chip select pins are redefined to data strobe pins. In this mode the Local Bus offers up to 8 address lines and four data-strobe pins.

6.3.3 PCI access to parallel port

When the parallel port is enabled (Mode 01), access to the port works via BAR definitions as usual, except that there are two I/O BARs corresponding to the two sets of registers defined to operate an IEEE1284 EPP and bi-directional Parallel Port.

The user can change the I/O space block size of BAR0 by over-writing the default values in LT2[25:20] using the serial EEPROM (see section 6.4). For example the user can reduce the allocated space for BAR0 to 4-bytes by setting LT2[22:20] to '001'. The I/O block size allocated to BAR1 is fixed at 8-Bytes.

Legacy parallel ports expect the upper register set to be mapped 0x400 above the base block, therefore if the BARs are fixed with this relationship, generic parallel port drivers can be used to operate the device in all modes.
Example: BAR0 = 0x00000379 (8 bytes at address 0x378)
BAR1 = 0x00000779 (8 bytes at address 0x778)
If this relationship is not used, custom drivers will be needed.

6.3.4 PCI access to 32-bit local bus

Access to the Local Bus in 32-bit mode is similar to 8-bit mode (see section 6.3.2) with the following exceptions:

- The local Bus offers a 32-bit bi-directional data bus and 12 bit address bus
- The PCI address signals 'AD[13:2]' are asserted on LBA[11:0]
- Block size in memory space is programmable by LT2[28:27] (see section 6.4)
- The Lower-Address-CS-Decode (LT2[26:23]) parameter is used to decode up to 4 chip selects

The block size allocation for chip-select regions is defined in Table 9.

Number of Chip selects	Memory block size (Kbytes)	LT2[28:27]	LT2[26:23]
1	16	'01'	'1010'
2	16	'01'	'1001'
4	16	'01'	'1000'
1	4	'00'	'1000'
2	4	'00'	'0111'
4	4	'00'	'0110'

Table 9: PCI access to 32-bit local bus (memory)

6.4 Accessing Local configuration registers

The local configuration registers are a set of device specific registers which can be accessed from either function. They are mapped to the I/O and memory addresses set up in BAR2 and BAR3 of each function, with the offsets defined for each register. Access is limited to byte only for I/O accesses; memory accesses can also be word or dword accessed, however on little-endian systems such as Intel 80x86 the byte order will be reversed.

6.4.1 Local Configuration and Control register 'LCC' (Offset 0x00)

This register defines control of ancillary functions such as Power Management, external clock reference signals and the serial EEPROM. The individual bits are described below.

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
1:0	Mode. These bits return the state of the Mode[1:0] pins.	-	R	XX
2	Enable UART clock output. When this bit is set, the buffered UART clock output pin (UART_CLK_Out) is active. When low UART_CLK_Out is permanently low.	W	RW	0
4:3	Endian Byte-Lane Select for memory access to 8-bit peripherals. 00 = Select Data[7:0] 10 = Select Data[23:16] 01 = Select Data[15:8] 11 = Select Data[31:24] Memory access to OX16PCI954 is always DWORD aligned. When accessing 8-bit regions like the internal UARTs, the 8-bit Local Bus and the parallel port, this option selects the active byte lane. As both PCI and PC architectures are little endian, the default value will be used by systems, however, some non-PC architectures may need to select the byte lane. These bits are ignored in 32-bit Local Bus.	W	RW	00
6:5	Power-down filter time. These bits define a value of an internal filter time for power-down interrupt request in power management circuitry in Function0. Once Function0 is ready to go into power down mode, OX16PCI954 will wait for the specified filter time and if Function0 is still in power-down request mode, it can assert a PCI interrupt (see section 6.6). 00 = power-down request disabled 10 = 129 seconds 01 = 4 seconds 11 = 518 seconds	W	RW	00
7	Function1 MIO2_PME Enable. A value of '1' enables MIO2 pin to set the PME_Status in PMCSR register, and hence assert the PME# pin if enabled. A value of '0' disables MIO2 from setting the PME_Status bit (see section 6.6).	W	RW	0
23:8	Reserved. These bits are used for test purposes. The device driver must write zeros to these bits.	-	R	0000h
24	EEPROM Clock. For PCI read or write to the EEPROM , toggle this bit to generate an EEPROM clock (EE_CK pin).	-	W	0
25	EEPROM Chip Select. When 1 the EEPROM chip-select pin EE_CS is activated (high). When 0 EE_CS is de-active (low).	-	W	0
26	EEPROM Data Out. For writes to the EEPROM, this output bit is the input-data of the EEPROM. This bit is output on EE_DO and clocked into the EEPROM by EE_CK.	-	W	0
27	EEPROM Data In. For reads from the EEPROM, this input bit is the output-data of the EEPROM connected to EE_DI pin.	-	R	X
28	EEPROM Valid. A 1 indicates that a valid EEPROM program is present	-	R	X
29	Reload configuration from EEPROM. Writing a 1 to this bit re-loads the configuration from EEPROM. This bit is self-clearing after EEPROM read	-	W	0
30	Reserved	-	-	0
31	Reserved	-	R	0

6.4.2 Multi-purpose I/O Configuration register 'MIC' (Offset 0x04)

This register configures the operation of the multi-purpose I/O pins 'MIO[11:0] as follows.

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
1:0	MIO0 Configuration Register (Mode[1:0]≠'01'). 00 -> MIO0 is a non-inverting input pin 01 -> MIO0 is an inverting input pin 10 -> MIO0 is an output pin driving '0' 11 -> MIO0 is an output pin driving '1' Unused (Mode[1:0]='01'). When Parallel Port is enabled, MIO[0] pin is unused and will remain in forcing output mode.	W	RW	00
3:2	MIO1 Configuration Register (LCC[6:5]='00'). 00 -> MIO1 is a non-inverting input pin 01 -> MIO1 is an inverting input pin 10 -> MIO1 is an output pin driving '0' 11 -> MIO1 is an output pin driving '1' Unused (LCC[6:5] ≠'00'). When power-down mode in Function0 is enabled, MIO1 pin is unused and will remain in forcing output mode.	W	RW	00
5:4	MIO2 Configuration Register (LCC[7]='0'). 00 -> MIO2 is a non-inverting input pin 01 -> MIO2 is an inverting input pin 10 -> MIO2 is output pin driving '0' 11 -> MIO2 is output pin driving '1' PME_Input (LCC[7]='1'). When LCC[7] is set, MIO2 pin is re-defined to PME_Input. It's polarity will be controlled by MIC[4]. It sets the sticky PME_Status bit in Function1.	W	RW	00
7:6	MIO3 Configuration Register. 00 -> MIO3 is a non-inverting input pin 01 -> MIO3 is an inverting input pin 10 -> MIO3 is an output pin driving '0' 11 -> MIO3 is an output pin driving '1'	W	RW	00
9:8	MIO4 Configuration Register. 00 -> MIO4 is a non-inverting input pin 01 -> MIO4 is an inverting input pin 10 -> MIO4 is an output pin driving '0' 11 -> MIO4 is an output pin driving '1'	W	RW	00
11:10	MIO5 Configuration Register. 00 -> MIO5 is a non-inverting input pin 01 -> MIO5 is an inverting input pin 10 -> MIO5 is an output pin driving '0' 11 -> MIO5 is an output pin driving '1'	W	RW	00
13:12	MIO6 Configuration Register. 00 -> MIO6 is a non-inverting input pin 01 -> MIO6 is an inverting input pin 10 -> MIO6 is an output pin driving '0' 11 -> MIO6 is an output pin driving '1'	W	RW	00
15:14	MIO7 Configuration Register. 00 -> MIO7 is a non-inverting input pin 01 -> MIO7 is an inverting input pin 10 -> MIO7 is an output pin driving '0' 11 -> MIO7 is an output pin driving '1'	W	RW	00

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
17:16	MIO8 Configuration Register. 00 -> MIO8 is a non-inverting input pin 01 -> MIO8 is an inverting input pin 10 -> MIO8 is an output pin driving '0' 11 -> MIO8 is an output pin driving '1'	W	RW	00
19:18	MIO9 Configuration Register. 00 -> MIO9 is a non-inverting input pin 01 -> MIO9 is an inverting input pin 10 -> MIO9 is an output pin driving '0' 11 -> MIO9 is an output pin driving '1'	W	RW	00
21:20	MIO10 Configuration Register. 00 -> MIO10 is a non-inverting input pin 01 -> MIO10 is an inverting input pin 10 -> MIO10 is an output pin driving '0' 11 -> MIO10 is an output pin driving '1'	W	RW	00
23:22	MIO11 Configuration Register. 00 -> MIO11 is a non-inverting input pin 01 -> MIO11 is an inverting input pin 10 -> MIO11 is an output pin driving '0' 11 -> MIO11 is an output pin driving '1'	W	RW	00
31:24	Reserved	-	R	00h

6.4.3 Local Bus Timing Parameter register 1 'LT1' (Offset 0x08):

The Local Bus Timing Parameter registers (LT1 and LT2) define the operation and timing parameters used by the Local Bus. The timing parameters are programmed in 4-bit registers to define the assertion/de-assertion of the Local Bus control signals. The value programmed in these registers defines the number of PCI clock cycles after a Reference Cycle when the events occur, where the reference Cycle is defined as two clock cycles after the master asserts the IRDY# signal. The following arrangement provides a flexible approach for users to define the desired bus timing of their peripheral devices. The timings refer to I/O or Memory mapped access to BAR0 and BAR1 of Function1.

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
3:0	Read Chip-select Assertion (Intel-type interface). Defines the number of clock cycles after the Reference Cycle when the LBCS[3:0]# pins are asserted (low) during a read operation from the Local Bus.[1] These bits are unused in Motorola-type interface.	W	RW	0h
7:4	Read Chip-select De-assertion (Intel-type interface). Defines the number of clock cycles after the Reference Cycle when the LBCS[3:0]# pins are de-asserted (high) during a read from the Local Bus. [1] These bits are unused in Motorola-type interface.	W	RW	3h (2h for parallel port)
11:8	Write Chip-select Assertion (Intel-type interface). Defines the number of clock cycles after the Reference Cycle when the LBCS[3:0]# pins are asserted (low) during a write operation to the Local Bus. [1] These bits are unused in Motorola-type interface.	W	RW	0h

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
15:12	Write Chip-select De-assertion (Intel-type interface). Defines the number of clock cycles after the reference cycle when the LBCS[3:0]# pins are de-asserted (high) during a write operation to the Local Bus. [1] Read-not-Write De-assertion during write cycles (Motorola-type interface). Defines the number of clock cycles after the reference cycle when the LBRDWR# pin is de-asserted (high) during a write to the Local Bus. [1]	W	RW	2h
19:16	Read Control Assertion (Intel-type interface). Defines the number of clock cycles after the Reference Cycle when the LBRD# pin is asserted (low) during a read from the Local Bus. [1] Read Data-strobe Assertion (Motorola-type interface). Defines the number of clock cycles after the Reference Cycle when the LBDS[3:0]# pins are asserted (low) during a read from the Local Bus. [1]	W	RW	0h (1h for parallel port)
23:20	Read Control De-assertion (Intel-type interface). Defines the number of clock cycles after the Reference Cycle when the LBRD# pin is de-asserted (high) during a read from the Local Bus. [1] Read Data-strobe De-assertion (Motorola-type interface). Defines the number of clock cycles after the Reference Cycle when the LBDS[3:0]# pins are de-asserted (high) during a read from the Local Bus. [1]	W	RW	3h (2h for parallel port)
27:24	Write Control Assertion (Intel-type interface). Defines the number of clock cycles after the Reference Cycle when the LBWR# pin is asserted (low) during a write to the Local Bus. [1] Write Data-strobe Assertion (Motorola-type interface). Defines the number of clock cycles after the Reference Cycle when the LBDS[3:0]# pins are asserted (low) during a write to the Local Bus. [1]	W	RW	0h (1h for parallel port)
31:28	Write Control De-assertion (Intel-type interface). Defines the number of clock cycles after the Reference Cycle when the LBWR# pin is de-asserted (high) during a write to the Local Bus. [1] Write Data-strobe De-assertion (Motorola-type interface). Defines the number of clock cycles after the Reference Cycle when the LBDS[3:0]# pins are de-asserted (high) during a write cycle to the Local Bus. [1]	W	RW	2h

Note 1: Only values in the range of 0h to Ah (0-10 decimal) are valid. Other values are reserved. These parameters apply to both 8-bit and 32-bit Local Bus configurations. See notes in the following page.

6.4.4 Local Bus Timing Parameter register 2 'LT2' (Offset 0x0C):

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
3:0	Write Data Bus Assertion. This register defines the number of clock cycles after the Reference Cycle when the LBD pins actively drive the data bus during a write operation to the Local Bus. [1]	W	RW	0h
7:4	Write Data Bus De-assertion. This register defines the number of clock cycles after the Reference Cycle when the LBD pins go high-impedance during a write operation to the Local Bus. [1,2]	W	RW	Fh
11:8	Read Data Bus Assertion. This register defines the number of clock cycles after the Reference Cycle when the LBD pins actively drive the data bus at the end of a read operation from the Local Bus. [1]	W	RW	4h (2h for parallel port)
15:12	Read Data Bus De-assertion. This register defines the number of clock cycles after the Reference Cycle when the LBD pins go high-impedance during at the beginning of a read cycle from the Local Bus. [1]	W	RW	0h
19:16	Reserved.	-	R	0h
22:20	IO Space Block Size of BAR0 in Function1. 000 = Reserved 100 = 32 Bytes 001 = 4 Bytes 101 = 64 Bytes 010 = 8 Bytes 110 = 128 Bytes 011 = 16 Bytes 111 = 256 Bytes	W	R	'100' (='010' for parallel port)
26:23	Local Bus Chip–select Parameter 'Lower-Address-CS-Decode'. [2] IO space in 8-bit Local Bus / Memory space and IO space in 32-bit Local Bus 0000 = A2 1000 = Res / 0000 = A4 1000 = A12 0001 = A3 1001 = Res / 0001 = A5 1001 = A13 0010 = A4 1010 = Res / 0010 = A6 1010 = A14 0011 = A5 1011 = Res / 0011 = A7 1011 = Res 0100 = A6 1100 = Res / 0100 = A8 1100 = Res 0101 = A7 1101 = Res / 0101 = A9 1101 = Res 0110 = A8 1110 = Res / 0110 = A10 1110 = Res 0111 = A9 1111 = Res / 0111 = A11 1111 = Res	W	RW	'0001' (='0010' for parallel port)
28:27	Memory Space Block Size of BAR1 in Function1 (Mode[1:0]='11', i.e. 32-bit Local Bus). 00 = 4 Kbytes 10 = Reserved 01 = 16 Kbytes 11 = Reserved When 8-bit Local Bus or Parallel Port is selected (Mode[1:0]='00' or '01'), the Memory Block size is fixed at 4K and these bits are ignored.	W	R	00
29	Local Bus Software Reset. When this bit is a 1 the Local Bus reset pin is activated. When this bit is a 0 the Local Bus reset pin is de-activated. [3]	-	RW	0
30	Local Bus Clock Enable. When this bit is a 1 the Local Bus clock (LBCK) pin is enabled. When this bit is a 0 LBCK pin is permanently low. The Local Bus Clock is a buffered PCI clock.	W	RW	0
31	Bus Interface Type. When low (=0) the Local Bus is configured to Intel-type operation, otherwise it is configured to Motorola-type operation. Note that when Mode[1:0] is '01', this bit is hard wired to 0.	W	RW	0

Note 1: Only values in the range of 0 to Ah (0-10 decimal) are valid. Other values are reserved as writing higher values causes the PCI interface to retry all accesses to the Local Bus as it is unable to complete the transaction in 16 PCI clock cycles.

Note 2: The Lower-Address-CS-Decode parameter is described in sections 6.3.2 & 6.3.4. These bits are unused for Memory access to the 8-bit Local Bus which uses a fixed decoding to allocate 1K regions to 4 chip selects. For further information on the Local bus, see section 8.

Note 3: Local Bus, UARTs and the Parallel Port are all reset with PCI reset. In Addition, the user can issue the Software Reset Command.

LT2[15:0] enable the card designer to control the data bus during the idle periods. The default values will configure the Local Bus data pins to remain forcing (LT2[7:4] = Fh). LT[15:8] is programmed to place the bus in high-impedance at the beginning of a read cycle and set it back to forcing at the end of the read cycle. For systems that require the data bus to stay in high-impedance, the card designer should write an appropriate value in the range of 0h to Ah to LT2[7:4]. This will place the data bus in high impedance at the end of the write cycle. Whenever the value programmed in LT2[7:4] does not equal Fh, the Local Bus controller will ignore the setting of LT2[15:8] as the data bus will be high-impedance outside write cycles. In this case the card designer should place external pull-ups on the data bus pins LBD[7:0] (or LBD[32:0] in 32-bit mode).

While the configuration data is read from the external EEPROM, the LBD pins remain in the high-impedance state.
The timing registers define the Local Bus timing parameters based on signal changes relative to a reference cycle which is defined as two PCI clock cycles after IRDY# is asserted for the first time in a frame. The following parameters are fixed relative to the reference cycle.

The Local Bus address pins (LBA[7:0] in 8-bit Local Bus, LBA[15:0] in 32-bit Local Bus) are asserted during the reference cycle. In a write operation, the Local Bus data is available during the reference cycle, however I/O buffers change direction as programmed in LT2[3:0].

In a Motorola type bus write operation, the Read-not-Write pin (LBRDWR#) is asserted (low) during the reference cycle. In a read cycle this pin remains high throughout the duration of the operation.

The default settings in LT1 & LT2 registers provide one PCI clock cycle for address and chip-select to control signal set-up time, one clock cycle for address and chip-select from control signal hold time, two clock cycles of pulse duration for read and write control signals and one clock cycle for data bus hold time. These parameters are acceptable for using external OX16C950, OX16C952 and OX16C954 devices connected to the Local Bus, in Intel mode. Some redefinition will be required if the bus is to be operated in Motorola mode.

The user should take great care when programming the Local Bus timing parameters. For example defining a value for chip-select assertion which is larger that the value defined for chip-select de-assertion or defining a chip-select assertion value which is greater than control signal assertion will result in obvious invalid local Bus cycles.

6.4.5 UART Receiver FIFO Levels 'URL' (Offset 0x10)

The receiver FIFO level of all internal UARTs are shadowed in Local configuration registers as follows:

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
7:0	UART0 Receiver FIFO Level (RFL[7:0])	-	R	0x00h
15:8	UART1 Receiver FIFO Level (RFL[7:0])	-	R	0x00h
23:16	UART2 Receiver FIFO Level (RFL[7:0])	-	R	0x00h
31:24	UART3 Receiver FIFO Level (RFL[7:0])	-	R	0x00h

6.4.6 UART Transmitter FIFO Levels 'UTL' (Offset 0x14)

The transmitter FIFO level of all internal UARTs are shadowed in Local configuration registers as follows:

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
7:0	UART0 Transmitter FIFO Level (TFL[7:0])	-	R	0x00h
15:8	UART1 Transmitter FIFO Level (TFL[7:0])	-	R	0x00h
23:16	UART2 Transmitter FIFO Level (TFL[7:0])	-	R	0x00h
31:24	UART3 Transmitter FIFO Level (TFL[7:0])	-	R	0x00h

6.4.7 UART Interrupt Source Register 'UIS' (Offset 0x18)

The UART Interrupt Source register is described below:

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
5:0	UART0 Interrupt Source Register (ISR[5:0])	-	R	01h
11:6	UART1 Interrupt Source Register (ISR[5:0])	-	R	01h
17:12	UART2 Interrupt Source Register (ISR[5:0])	-	R	01h
23:18	UART3 Interrupt Source Register (ISR[5:0])	-	R	01h
26:24	Reserved	-	R	00h
27	UART0 Good-Data Status	-	R	1
28	UART1 Good-Data Status	-	R	1
29	UART2 Good-Data Status	-	R	1
30	UART3 Good-Data Status	-	R	1
31	Global Good-Data Status. This bit is the logical AND of bits 27 to 30, i.e. it is set if Good-Data Status of all internal UARTs is set.	-	R	1

Good-Data status for a given internal UART is set when all of the following conditions are met:

- ISR reads a level0 (no-interrupt pending), a level 2a (receiver data available, a level 2b (receiver time-out) or a level 3 (transmitter THR empty) interrupt
- LSR[7] is clear so there is no parity error, framing error or break in the FIFO
- LSR[1] is clear so no over-run error has occurred

If the device driver software reads the receiver FIFO levels (URL) followed by this register, then if Good-Data status for a given channel is set, the driver can remove the number of bytes indicated by the FIFO level without the need to read the line status register for that channel. This feature enhances the driver efficiency.

For a given channel, if the Good-Data status bit is *not* set, then the software driver should examine the corresponding ISR bits. For example if bit 29 is low, then the driver should examine bits 17 down to 12 to obtain the ISR[5:0] for UART2. If the ISR indicates a level 4 or higher interrupt, the interrupt is due to a change in the state of modem lines or detection of flow control characters. The device driver-software should then take appropriate measures as would in any other 550/950 driver. When ISR indicates a level 1 (receiver status) interrupt then the driver can examine the Line Status Register (LSR) of the relevant channel. Since reading the LSR clears LSR[7], the device driver-software should either flush or empty the contents of the receiver FIFO, otherwise the Good-Data status will no longer be valid.

The UART Receiver FIFO Level (URL), UART Transmitter FIFO Level (UTL), UART Interrupt Source register (UIS) and Global Interrupt Status register (GIS) are allocated adjacent address offsets (10h to 1Ch) in the Base Address Register. The device driver-software can read all of the above registers in single burst read operation. The location offset of the registers are such that the FIFO levels are usually read before the status registers so that the status of the N characters indicated in the receiver FIFO levels are valid.

6.4.8 Global Interrupt Status and Control Register 'GIS' (Offset 0x1C)

Bits	Description	Read/Write		Reset
		EEPROM	PCI	
3:0	These bits reflect the state of UART3 to UART0 internal interrupt lines, respectively.[1]	-	R	0x0h
4	MIO0 (Mode[1:0]≠'01'). This bit reflects the state of the internal MIO[0]. The internal MIO[0] reflects the non-inverted or inverted state of MIO0 pin.[2]	-	R	X
	Parallel Port Interrupt (Mode[1:0]='01'). This bit reflects the state of the Parallel Port internal interrupt line.	-	R	0
5	MIO1 (LCC[6:5]='00'). This bit reflects the state of the internal MIO[1]. The internal MIO[1] reflects the non-inverted or inverted state of MIO1 pin.[2]		R	X
	Function0 Power-down Interrupt (LCC[6:5] ≠'00'). In this mode this is a sticky bit. When set, it indicates a power-down request issued by Function0 and would normally have asserted a PCI interrupt if bit 21 was set (see section 7.9). Reading this bit clears it.			0
15:6	These bits reflect the state of the internal MIO[11:2]. The internal MIO[11:2] reflect the non-inverted or inverted state of MIO[11:2] pins respectively.[2]	-	R	XXXh
19:16	UART Interrupt Mask. When set (=1) these bit enable each internal UART to assert a PCI interrupt respectively. When cleared (=0) they prevent the respective channel from asserting a PCI interrupt.[3]	W	RW	Fh
20	MIO[0] Interrupt Mask (Mode[1:0]≠'01'). When set (=1) this bit enables MIO0 pin to assert a PCI interrupt. When cleared (=0) it prevents MIO0 pin from asserting a PCI interrupt.[2]	W	RW	1
	Parallel Port Interrupt Mask (Mode[1:0]='01'). When set (=1) this bit enables the Parallel Port to assert a PCI interrupt. When cleared (=0) it prevents the Parallel Port from asserting a PCI interrupt.	W	RW	1
21	MIO[1] Interrupt Mask (LCC[6:5]='00'). When set (=1) this bit enables MIO1 pin to assert a PCI interrupt. When cleared (=0) it prevents MIO1 pin from asserting a PCI interrupt.[2]	W	RW	1
	Function0 Power-down Interrupt Mask (LCC[6:5] ≠'00'). When set (=1) this bit enables the power-down logic in Function0 to assert a PCI interrupt. When cleared (=0) it prevents the power-down logic in Function0 from asserting a PCI interrupt.	W	RW	0
31:22	MIO Interrupt Mask. When set (=1) these bits enable each MIO[11:2] pin to assert a PCI interrupt respectively. When cleared (=0) they prevent the respective pins from asserting a PCI interrupt.[2]	W	RW	3FFh

Note 1: GIS[3:0] are the inverse of UIS[24], UIS[18], UIS[6] and UIS[0] respectively. Systems that do not require the Local Bus or parallel port need not read this register to identify the source of the interrupt as long as they read the UIS (offset 18h) register.

Note 2: The returned value is either the direct state of the corresponding MIO pin or its inverse as configured by the Multi-purpose I/O Configuration register 'MIC' (offset 0x04). As the internal MIO can assert a PCI interrupt, the inversion feature can define each external interrupt to be defined as active-low or active-high, as controlled by the MIC register.

Note 3: The UART Interrupt Mask register bits are all set after a hardware reset to enable the interrupt from all internal UARTs. This will cater for generic device-driver software that does not access the Local Configuration Registers. The default setting for UART Interrupt Mask bits can be changed using the serial EEPROM. Note that even though by default the UART interrupts are enabled in this register, since after a reset the IER registers of individual UARTs disables all interrupts, a PCI interrupt will not be asserted after a hardware reset.

Note 4: When Mode[1:0]='10', the MIO pins are used to define a Subsystem ID value, therefore all interrupts due to MIO pins are disabled regardless of the state of the GIS register. The MIO Interrupts Mask register bits are all set after a hardware reset to enable the interrupt from all MIO pins from boot up. The default setting for MIO Interrupt Mask bits can be changed using the serial EEPROM.

6.5 PCI Interrupts

Interrupts in PCI systems are level-sensitive and can be shared. There are sixteen sources of interrupt in the OX16PCI954, one in each UART channel and twelve from Multi-Purpose IO pins (MIO11 to MIO0). The Parallel Port and MIO0 share the same interrupt status bit (GIS[4]). The PCI Power Management power-down interrupt for internal UARTs (Function0) and MIO1 share the status bit GIS[5]. The Local Bus uses the MIO pins to pass interrupts to the PCI controller.

All interrupts are routed to the PCI interrupt pins, INTA# or INTB#. The default routing asserts Function0 interrupts on INTA# and Function1 interrupts on INTB#. These default routings may be modified by writing to the Interrupt Pin field in the configuration registers using the serial EEPROM facility. The Interrupt Pin field is normally considered a hard-wired read-only value in PCI. It indicates to system software which PCI interrupt pin (if any) is used by a function. The interrupt pin may only be modified using the serial EEPROM facility, and card developers must not invoke any combination which violates the PCI specification. Note that OX16PCI954 only has two PCI interrupt pins, INTA# and INTB#. If in doubt, the default routings should be used. Table 10 relates the Interrupt Pin field to the device pin used.

Interrupt Pin	Device Pin used
0	None
1	INTA#
2	INTB#
3 to 255	Reserved

Table 10: 'Interrupt pin' definition

During the system initialisation process and PCI device configuration, system-specific software reads the interrupt pin field to determine which (if any) interrupt pin is used by each function. It programmes the system interrupt router to logically connect this PCI interrupt pin to a system-specific interrupt vector (IRQ). It then writes this routing information to the Interrupt Line field in the function's PCI configuration space. Device driver software must then hook the interrupt using the information in the Interrupt Line field.

Interrupt status for all sixteen sources of interrupt is available using the GIS register in the Local Configuration Register set, which can be accessed using I/O or Memory accessed from both logical functions. This facility enables each function to snoop on interrupts asserted from the other function regardless of the interrupt routing.

The interrupt from each UART channel is enabled using the IER register and the MCR register for that UART. If the interrupt is enabled and active, then the device will drive the PCI interrupt pin low. Generic device driver software will use the IER register to enable interrupts. The OX16PCI954 offers additional interrupt masking ability using GIS[19:16] (see section 6.4.8). An internal UART channel may assert a PCI interrupt if the interrupt is enabled by IER and GIS[19:16].

All interrupts can be enabled / disabled individually using the GIS register set in the Local configuration registers. When an MIO pin is enabled, an external device can assert a PCI interrupt by driving that pin. The sense of the MIO external interrupt pins (active-high or active-low) is defined in the MIC register. The parallel port can also assert an interrupt (Note: this effectively disables the MIO[0] interrupt).

6.6 Power Management

The OX16PCI954 is compliant with PCI Power Management Specification Revision 1.0. Each logical function implements its own set of Power Management registers and supports the power states D0, D2 and D3. Power management is accomplished by power-down and power-up requests, asserted via interrupts and the PME# pin respectively. Each function can assert the PME# pin independently. The PME# pin is de-asserted when the sticky PME_Status bit is cleared in both functions.

Power-down request is not defined by Power Management 1.0. It is a device-specific feature and requires a bespoke device driver implementation. The device driver can either implement the power-down itself or in the case of Function 0, use a special interrupt and power-down features offered by the device to determine when the UARTs are ready for power-down.

The PME# pin can, in certain cases, activate the PME# signal when power is removed from the device, which will cause the PC to wake up from Low-power state D3(cold). To ensure full cross-compatibility with systemboard implementations, use of an isolator FET is recommended. If Power Management capabilities are not required, the PME# pin can be treated as no-connect.

6.6.1 Power Management of Function 0

Function 0 can be configured to monitor the activity of the serial channels, and issue a power-down interrupt when all four ports are inactive (no interrupts pending and both transmitter and receiver are idle). It can also issue a wake-up request on the PME# line from power states D2 and D3. The conditions for inactive mode are the same as the ones for sleep-mode (see section 7.6.4); however power management operation and 16C950 sleep mode are separate and independent operations, affording maximum flexibility in power usage.

Whenever the device driver places Function0 in power-state D3, the clock to all internal UARTs is shut off immediately and will only be turned on when the device driver places function0 in power-state D0. In this case, only activity on the RI line (the trailing edge of a pulse) will assert a wake-up request. Wake-up from power sate D2 is configurable, and can be triggered by activity on any combination of modem lines or the serial data input (SIN) line. See section 7.11.10 to mask wakeup events. In case of a wake up request from SIN when function0 is in power-state D2, the clock for that channel is turned on so serial data framing can be maintained.

When all channels are ready for power-down (i.e. inactive), the power management circuitry waits for a period of time programmed in Power-down Filter Time (LCC[6:5], see section 6.4.1) and if all channels are still inactive, the OX16PCI954 can issue a PCI interrupt if it is enabled. The filter stops the UARTs from issuing too many interrupts whenever the UART activity is intermittent. Upon a power down interrupt, the device driver can change the power-state of Function0 as required. Note that the power-state of the device is only changed by the device driver and at no point will the OX16PCI954 change its own power state. The interrupt merely informs the device driver that this PCI logical function can is ready for power down.

When enabled, the power-down interrupt status is reflected in GIS[5] which is normally used to return the value of MIO1. It also uses the corresponding interrupt mask bit, GIS[21]. The interrupt masking operation is shown in Table 11.

The device driver can enable the power-down request by first writing a power-down filter time to LCC[6:5] which is not '00'. Then it can either operate in polling mode by reading GIS[5] or use a PCI interrupt. When LCC[6:5] is not '00', GIS[5] will be a 'sticky-bit' which is set whenever there is power-down request from Function 0. This bit is cleared when the device driver reads the GIS[5] register. GIS[5] will assert a PCI interrupt if GIS[21] is set.

Function0 implements the PCI Power Management power-states D0, D2 and D3. Whenever the device driver changes the power-state to state D2 or D3, Function0 takes the following actions:

- The internal clock to internal UARTs is shut down.
- PCI interrupt for Function0 is disabled regardless of the value of GIS[19:16].
- Access to I/O or Memory BARs of Function0 is disabled.

However, access to the configuration space is still enabled.

Function0 can issue a wake up request by asserting PME# if it is enabled by PMCSR[8] of Function0. The PME# assertion is immediate and does not use the power-down filter timer. It operates even if LCC[6:5] is set to '00'. The wake up condition for Function0 is as follows:-

When Function0 is in power-state D3, a trailing edge on the modem line 'RI' asserts PME# as long PMCSR[8] is set. When Function0 is in power-state D3, a change in the state of any modem line which is enabled by a 16C950-specific mask bit, or a change in the state of the serial input line if enabled by a 16C950-specific mask bit can issue a wake up request by asserting the PME# signal (see section 8.4.11). After a hardware reset all of these mask bits are cleared to enable wake up PME# assertion from all modem lines and the SIN line. As the wake up operation requires at least one mask bit to be enabled, the device driver can for example disable the masks from three UART channels so that only one channel can issue a wake up request, or

disable all masks with the exception of the Ring Indicator, so only a modem ring can wake up the computer.

When Function0 issues a wake up request, the PME_Status (PMCSR[15]) will be set. This is a sticky bit which will be cleared by writing a '1' to it. While PME_En (PMCSR[8]) in Function0 is set, PME_Status will assert the PME# pin to inform the device driver that a power management wake up event has occurred. After a wake up event is signalled, the device driver is expected to return the function to the D0 power-state.

6.6.2 Power Management of function 1

The power-down request for the Local Bus (Function1) is application-dependent. The device driver can use any of the multi-purpose I/O lines, MIO[12:3] to issue a power-down request.

Function1 implements the PCI Power Management power-states D0, D2 and D3. Whenever the device driver changes the power-state to state D2 or D3, Function1 takes the following actions:-

- The external UART_Clk_Out pin is disabled regardless of the programmed value in LCC[2].
- The Local Bus clock pin, LBCK, is disabled regardless of the programmed value in LT2[30].
- The PCI interrupt for Function1 is disabled.
- Access to I/O or Memory BARs of Function1 is disabled.

However, access to the configuration space is still enabled. The device driver can optionally assert/de-assert any of its selected (design dependant) MIO pins to switch off VCC, disable other external clocks, or activate shut-down modes to any external devices on the Local Bus.

Function1 can issue a wake up request by using the MIO2 pin. When LCC[7] is set, rising or falling edge of MIO2 will cause Function1 to issue a wake up request by setting PME_Status = (PMCSR[15]), if it is enabled by PMCSR[8] of Function1. When LCC[7] is set, the MIO2 pin will remain in input mode regardless of the value programmed in MIC[5], However MIC[4] still controls the input sense. PME_Status is a sticky bit which will be cleared by writing a '1' to it. While PME_En (PMCSR[8]) bit in Function1 is set, PME_Status will assert the PME# pin to inform the device driver that a power management wake up event has occurred. After a wake up event is signalled, the device driver is expected to return the function to the D0 power-state. Settings for wake up events are shown in Table 12.

LCC[6:5]	GIS[21]	Power-down Filter Time	Operation
00	X	N/A	Function0 power-down interrupt is disabled. MIO1 can assert as interrupt is GIS[21] is set.
01	0	4 s	Function0 power-down interrupt is disabled. GIS[5] reflects the state of the internal power-down mode for Polling operation. MIO1 interrupt is disabled.
10	0	129 s	
11	0	518 s	
01	1	4 s	Function0 power-down is enabled. GIS[5] reflects the state of the internal power-down mode. MIO1 interrupt is disabled.
10	1	129 s	
11	1	515 s	

Table 11: Function 0 (UARTs) Power down interrupt settings

LCC[7]	MIC[4]	MIO2 Rising	MIO2 Falling	Function1 PME_Status
0	X	X	X	Remains unchanged
1	0	yes	X	Gets set
1	0	no	X	Remains unchanged
1	1	X	Yes	Gets set
1	1	X	No	Remains unchanged

Table 12: Function 1 (Local Bus) Wake-up configuration

7 INTERNAL OX16C950 UARTS

Each of the four UART channels in the OX16PCI954 operates individually as an OX16C950 high-peformance serial port. Each channel has its own full set of registers, but all share a common clock and FIFOSEL pin. After a device reset, a common configuration state is loaded into all four channels, but after this time each can be operated individually through its own 8-byte block of addressable space.

7.1 Operation – mode selection

Each channel is backward compatible with the 16C450, 16C550, 16C654 and 16C750 UARTs. The operation of the ports depends on a number of mode settings, which are referred to throughout this section. The modes, conditions and corresponding FIFO depth are tabulated below:

UART Mode	FIFO size	FCR[0]	Enhanced mode (EFR[4]=1)	FCR[5] (guarded with LCR[7] = 1)	FIFOSEL pin
450	1	0	X	X	X
550	16	1	0	0	0
Extended 550	128	1	0	X	1
650	128	1	1	X	X
750	128	1	0	1	0
950[1]	128	1	1	X	X

Table 13: UART Mode Configuration

Note 1: 950 mode configuration is identical to 650 configuration

7.1.1 450 Mode

After a hardware reset, bit 0 of the FIFO Control Register ('FCR') is cleared, hence the UARTs are compatible with the 16C450. The transmitter and receiver FIFOs (referred to as the 'Transmit Holding Register' and 'Receiver Holding Register' respectively) have a depth of one. This is referred to as 'Byte mode'. When FCR[0] is cleared, all other mode selection parameters are ignored.

7.1.2 550 Mode

Connect FIFOSEL to GND. After a hardware reset, writing a 1 to FCR[0] will increase the FIFO size to 16, providing compatibility with 16C550 devices.

7.1.3 Extended 550 Mode

Connect FIFOSEL to VDD. Writing a 1 to FCR[0] will now increase the FIFO size to 128, thus providing a 550 device with 128 deep FIFOs.

7.1.4 750 Mode

For compatibility with 16C750, connect FIFOSEL to GND. Writing a 1 to FCR[0] will increase the FIFO size to 16. In a similar fashion to 16C750, the FIFO size can be further increased to 128 by writing a 1 to FCR[5]. Note that access to FCR[5] is protected by LCR[7]. i.e., to set FCR[5], software should first set LCR[7] to temporarily remove the guard. Once FCR[5] is set, the software should clear LCR[7] for normal operation.

The 16C750 additional features are available as long as the UART is not put into Enhanced mode; i.e. ensure EFR[4] = '0'. These features are:

- Deeper FIFOs
- Automatic RTS/CTS out-of-band flow control
- Sleep mode

7.1.5 650 Mode

The OX16C950 is compatible with the 16C650 when EFR[4] is set, i.e. the device is in Enhanced mode. As 650 software drivers usually put the device in Enhanced mode, running 650 drivers on the one of the UART channels will result in 650 compatibility with 128 deep FIFOs, as long as FCR[0] is set. This is regardless of the state of the FIFOSEL pin. Note that the 650 emulation mode of the OX16PCI954 provides 128-deep FIFOs rather than the 32 provided by a legacy 16C654.

In enhanced (650) mode the device has the following features available over those provided by a generic 550. (Note: some of these are similar to those provided in 750 mode, but enabled using different registers).

- Deeper FIFOs
- Sleep mode
- Automatic in-band flow control
- Special character detection
- Infra-red "IrDA-format" transmit and receive mode
- Transmit trigger levels
- Optional clock prescaler

7.1.6 950 Mode

The additional features offered in 950 mode generally only apply when the UART is in Enhanced mode (EFR[4]='1'). Provided FCR[0] is set, in Enhanced mode the FIFO size is 128 regardless of the state of FIFOSEL.

Note that 950 mode configuration is identical to that of 650 mode, however additional 950 specific features are enabled using the Additional Control Register 'ACR' (see section 7.11.3). In addition to larger FIFOs and higher baud rates, the enhancements of the 950 mode over 650 emulation mode are:

- Selectable arbitrary trigger levels for the receiver and transmitter FIFO interrupts
- Improved automatic flow control using selectable arbitrary thresholds
- DSR#/DTR# automatic flow control
- Transmitter and receiver can be optionally disabled
- Software reset of device
- Readable FIFO fill levels
- Optional generation of an RS-485 buffer enable signal
- Four-byte device identification (0x16C95001)
- Readable status for automatic in-band and out-of-band flow control
- External 1x clock modes (see section 7.10.4)
- Flexible "M+N/8" clock prescaler (see section 7.10.2)
- Programmable sample clock to allow data rates up to 15 Mbps (see section 7.10.3).
- 9-bit data mode
- Readable FCR register

The 950 trigger levels are enabled when ACR[5] is set where bits 4 to 7 of FCR are ignored. Then arbitrary trigger levels can be defined in RTL, TTL, FCL and FCH registers (see section 7.11). The Additional Status Register ('ASR') offers flow control status for the local and remote transmitters. FIFO levels are readable using RFL and TFL registers.

The UART has a flexible prescaler capable of dividing the system clock by any value between 1 and 31.875 in steps of 0.125. It divides the system clock by an arbitrary value in "M+N/8" format, where M and N are 5- and 3-bit binary numbers programmed in CPR[7:3] and CPR[2:0] respectively. This arrangement offers a great deal of flexibility when choosing an input clock frequency to synthesise arbitrary baud rates. The default division value is 4 to provide backward compatibility with 16C650 devices.

The user may apply an external 1x (or Nx) clock for the transmitter and receiver to the RI# and DSR# pin respectively. The transmitter clock may instead be asserted on the DTR# pin. The external clock options are selected through the CKS register (offset 0x02 of ICR).

It is also possible to define the over-sampling rate used by the transmitter and receiver clocks. The 16C450/16C550 and compatible devices employ 16 times over-sampling, where there are 16 clock cycles per bit. However the 95x UART channels can employ any over-sampling rate from 4 to 16 by programming the TCR register. This allows the data rates to be increased to 460.8 Kbps using a 1.8432MHz clock, or 15 Mbps using a 60 MHz clock. The default value after a reset for this register is 0x00, which corresponds to a 16 cycle sampling clock. Writing 0x01, 0x02 or 0x03 will also result in a 16 cycle sampling clock. To program the value to any value from 4 to 15 it is necessary to write this value into the TCR i.e. to set the device to a 13 cycle sampling clock it would be necessary to write 0x0D to TCR. For further information see section 7.10.3

The UARTs also offer 9-bit data frames for multi-drop industrial applications.

7.2 Register description tables

Each UART is accessed through an 8-byte block of I/O space (or through memory space). Since there are more than 8 registers, the mapping is also dependent on the state of the Line Control Register 'LCR' and Additional Control Register 'ACR':

1. LCR[7]=1 enables the divider latch registers DLL and DLM.
2. LCR specifies the data format used for both transmitter and receiver. Writing 0xBF (an unused format) to LCR enables access to the 650 compatible register set. Writing this value will set LCR[7] but leaves LCR[6:0] unchanged. Therefore, the data format of the transmitter and receiver data is not affected. Write the desired LCR value to exit from this selection.
3. ACR[7]=1 enables access to the 950 specific registers.
4. ACR[6]=1 enables access to the Indexed Control Register set (ICR) registers as described on page 33.

Register Name	Address	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
THR [1]	000	W	Data to be transmitted							
RHR [1]	000	R	Data received							
IER [1,2] 650/950 Mode	001	R/W	CTS interrupt mask	RTS interrupt mask	Special Char. Detect	Sleep mode	Modem interrupt mask	Rx Stat interrupt mask	THRE interrupt mask	RxRDY interrupt mask
550/750 Mode			Unused		Alternate sleep mode					
FCR [3] 650 mode	010	W	RHR Trigger Level		THR Trigger Level		Tx Trigger Enable	Flush THR	Flush RHR	Enable FIFO
750 mode			RHR Trigger Level		FIFO Size	Unused				
950 mode			Unused							
ISR [3]	010	R	FIFOs enabled		Interrupt priority (Enhanced mode)		Interrupt priority (All modes)			Interrupt pending
LCR [4]	011	R/W	Divisor latch access	Tx break	Force parity	Odd / even parity	Parity enable	Number of stop bits	Data length	
MCR [3,4] 550/750 Mode	100	R/W	Unused		CTS & RTS Flow Control	Enable Internal Loop Back	Unused		RTS	DTR
650/950 Mode			Baud prescale	IrDA mode	XON-Any					
LSR [3,5] Normal	101	R	Data Error	Tx Empty	THR Empty	Rx Break	Framing Error	Parity Error	Overrun Error	RxRDY
9-bit data mode								9th Rx data bit		
MSR [3]	110	R	DCD	RI	DSR	CTS	Delta DCD	Trailing RI edge	Delta DSR	Delta CTS
SPR [3] Normal	111	R/W	Temporary data storage register and Indexed control register offset value bits							
9-bit data mode			Unused							9th Tx data bit
Additional Standard Registers – These registers require divisor latch access bit (LCR[7]) to be set to 1.										
DLL	000	R/W	Divisor latch bits [7:0] (Least significant byte)							
DLM	001	R/W	Divisor latch bits [15:8] (Most significant byte)							

Table 14: Standard 550 Compatible Registers

Register Name	Address	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
To access these registers LCR must be set to 0xBF										
EFR	010	R/W	CTS flow control	RTS Flow control	Special char detect	Enhance mode	In-band flow control mode			
XON1	100	R/W	XON Character 1							
9-bit mode			Special character 1							
XON2	101	R/W	XON Character 2							
9-bit mode			Special Character 2							
XOFF1	110	R/W	XOFF Character 1							
9-bit mode			Special character 3							
XOFF2	111	R/W	XOFF Character 2							
9-bit mode			Special character 4							

Table 15: 650 Compatible Registers

Register Name	Address	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASR [1,6,7]	001	R/W [7]	Tx Idle	FIFO size	FIFO-SEL	Special Char Detect	DTR	RTS	Remote Tx Disabled	Tx Disabled
RFL [6]	011	R	Number of characters in the receiver FIFO							
TFL [3,6]	100	R	Number of characters in the transmitter FIFO							
ICR [3,8,9]	101	R/W	Data read/written depends on the value written to the SPR prior to the access of this register (see Table 17)							

Table 16: 950 Specific Registers

Register access notes:

Note 1: Requires LCR[7] = 0
Note 2: Requires ACR[7] = 0
Note 3: Requires that last value written to LCR was not 0xBF
Note 4: To read this register ACR[7] must be = 0
Note 5: To read this register ACR[6] must be = 0
Note 6: Requires ACR[7] = 1
Note 7: Only bits 0 and 1 of this register can be written
Note 8: To read this register ACR[6] must be = 1
Note 9: This register acts as a window through which to read and write registers in the Indexed Control Register set

Register Name	SPR Offset [10]	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Indexed Control Register Set										
ACR	0x00	R/W	Addit-ional Status Enable	ICR Read Enable	950 Trigger Level Enable	DTR definition and control		Auto DSR Flow Control Enable	Tx Disable	Rx Disable
CPR	0x01	R/W	5 Bit "integer" part of clock prescaler					3 Bit "fractional" part of clock prescaler		
TCR	0x02	R/W	Unused				4 Bit N-times clock selection bits [3:0]			
CKS	0x03	R/W	Tx 1x Mode	Tx CLK Select	BDOUT on DTR	DTR 1x Tx CLK	Rx 1x Mode	0	Receiver Clock Sel[1:0]	
TTL	0x04	R/W	Unused	Transmitter Interrupt Trigger Level (0-127)						
RTL	0x05	R/W	Unused	Receiver Interrupt Trigger Level (1-127)						
FCL	0x06	R/W	Unused	Automatic Flow Control Lower Trigger Level (0-127)						
FCH	0x07	R/W	Unused	Automatic Flow Control Higher Trigger level (1-127)						
ID1	0x08	R	Hardwired ID byte 1 (0x16)							
ID2	0x09	R	Hardwired ID byte 1 (0xC9)							
ID3	0x0A	R	Hardwired ID byte 1 (0x50)							
REV	0x0B	R	Hardwired revision byte (0x01)							
CSR	0x0C	W	Writing 0x00 to this register will reset the UART (Except the CKS register)							
NMR	0x0D	R/W	Unused		9th Bit SChar 4	9th Bit SChar 3	9th Bit SChar 2	9th Bit SChar 1	9th-bit Int. En.	9 Bit Enable
MDM	0x0E	R/W	0	0	SIN wakeup disable	Modem Wakeup Disable	Δ DCD Wakeup disable	Trailing RI edge disable	Δ DSR Wakeup disable	Δ CTS Wakeup disable
RFC	0X0F	R	FCR[7]	FCR[6]	FCR[5]	FCR[4]	FCR[3]	FCR[2]	FCR[1]	FCR[0]
GDS	0X10	R	0	0	0	0	0	0	0	Good data status

Table 17: Indexed Control Register Set

Note 10: The SPR offset column indicates the value that must be written into SPR prior to reading / writing any of the Indexed Control Registers via ICR. Offset values not listed in the table are reserved for future use and must not be used.

To read or write to any of the Indexed Controlled Registers use the following procedure:

Writing to ICR registers:
Ensure that the last value written to LCR was not 0xBF (reserved for 650 compatible register access value).
Write the desired offset to SPR (address 111b).
Write the desired value to ICR (address 101b).

Reading from ICR registers:
Ensure that the last value written to LCR was not 0xBF (see above).
Write 0x00 offset to SPR to select ACR.
Set bit 6 of ACR (ICR read enable) by writing x1xxxxxb to address 101b. Ensure that other bits in ACR are not changed.
(Software drivers should keep a copy of the contents of the ACR elsewhere since reading ICR involves overwriting ACR!)
Write the desired offset to SPR (address 111b).
Read the desired value from ICR (address 101b).
Write 0x00 offset to SPR to select ACR.
Clear bit 6 of ACR bye writing x0xxxxxb to ICR, thus enabling access to standard registers again.

7.3 Reset Configuration

7.3.1 Hardware Reset

After a hardware reset, all writable registers are reset to 0x00, with the following exceptions:

DLL, which is reset to 0x01.
CPR, which is reset to 0x20.

The state of read-only registers following a hardware reset is as follows:

RHR[7:0]: Indeterminate
RFL[6:0]: 0000000_2
TFL[6:0]: 0000000_2
LSR[7:0]: 0x60 signifying that both the transmitter and the transmitter FIFO are empty
MSR[3:0]: 0000_2
MSR[7:4]: Dependent on modem input lines DCD, RI, DSR and CTS respectively
ISR[7:0]: 0x01, i.e. no interrupts are pending
ASR[7:0]: $1xx00000_2$

The reset state of output signals are tabulated below:

Signal	Reset state
SOUT	Inactive High
RTS#	Inactive High
DTR#	Inactive High

Table 18: Output Signal Reset State

7.3.2 Software Reset

An additional feature available in the OX16C950 UART is software resetting of the serial channel. This command has the same effect on a single channel as a hardware reset except it does not reset the clock source selections (i.e. CKS register). To reset the UART write 0x00 to the Channel Software Reset register 'CSR'.

7.4 Transmitter and receiver FIFOs

Both the transmitter and receiver have associated holding registers (FIFOs), referred to as the transmitter holding register (THR) and receiver holding register (RHR) respectively.

In normal operation, when the transmitter finishes transmitting a byte it will remove the next data from the top of the THR and proceed to transmit it. If the THR is empty, it will wait until data is written into it. If THR is empty and the last character being transmitted has been completed (i.e. the transmitter shift register is empty) the transmitter is said to be idle. Similarly, when the receiver finishes receiving a byte, it will transfer it to the bottom of the RHR. If the RHR is full, an overrun condition will occur (see section 7.5.3).

Data is written into the bottom of the THR queue and read from the top of the RHR queue completely asynchronously to the operation of the transmitter and receiver.

The size of the FIFOs is dependent on the setting of the FCR register. When in Byte mode, these FIFOs only accept one byte at a time before indicating that they are full; this is compatible with the 16C450. When in a FIFO mode, the size of the FIFOs is either 16 (compatible with the 16C550) or 128.

Data written to the THR when it is full is lost. Data read from the RHR when it is empty is invalid. The empty or full status of the FIFOs are indicated in the Line Status Register 'LSR' (see section 7.5.3). Interrupts are generated when the UART is ready for data transfer to/from the FIFOs. The number of items in each FIFO may also be read back from the transmitter FIFO level (TFL) and receiver FIFO level (RFL) registers (see section 7.11.2).

7.4.1 FIFO Control Register 'FCR'

FIFO setup:

FCR[0]: Enable FIFO mode
logic 0 ⇒Byte mode.
logic 1 ⇒FIFO mode.

This bit should be enabled before setting the FIFO trigger levels.

FCR[1]: Flush RHR
logic 0 ⇒No change.
logic 1 ⇒Flushes the contents of the RHR

This is only operative when already in a FIFO mode. The RHR is automatically flushed whenever changing between Byte mode and a FIFO mode. This bit will return to zero after clearing the FIFOs.

FCR[2]: Flush THR
logic 0 ⇒ No change.
logic 1 ⇒Flushes the contents of the THR, in the same manner as FCR[1] does for the RHR.

THR Trigger levels:

FCR[3]: Tx trigger level enable
logic 0 ⇒Transmit trigger levels enabled
logic 1 ⇒Transmit trigger levels disabled

When FCR[3]=0, the transmitter trigger level is always set to 1, thus ignoring FCR[5:4]. Alternatively, 950-mode trigger levels can be set using ACR[5].

FCR[5:4]: Compatible trigger levels

450, 550 and extended 550 modes:
The transmitter interrupt trigger levels are set to 1 and FCR[5:4] are ignored.

650 mode:
In 650 mode the transmitter interrupt trigger levels can be set to the following values:

FCR[5:4]	Transmit Interrupt Trigger level
00	16
01	32
10	64
11	112

Table 19: Transmit Interrupt Trigger Levels

These levels only apply when in Enhanced mode and when FCR[3] is set, otherwise the trigger level is set to 1. A transmitter empty interrupt will be generated (if enabled) if the TFL falls below the trigger level.

750 Mode:
In 750 compatible mode, transmitter trigger level is set to 1, FCR[4] is unused and FCR[5] defines the FIFO depth as follows:

FCR[5]=0: FIFO size is 16 bytes.
FCR[5]=1: FIFO size is 128 bytes.

In non-Enhanced mode and when FIFOSEL pin is low, FCR[5] is writable only when LCR[7] is set. Note that in Enhanced mode, the FIFO size is increased to 128 bytes when FCR[0] is set.

950 mode:
Setting ACR[5]=1 enables 950-mode trigger levels set using the TTL register (see section 7.11.4), FCR[5:4] are ignored.

RHR trigger levels

FCR[7:6]: Compatible Trigger levels

450, 550, extended 550, 650 and 750 modes:
The receiver FIFO trigger levels are defined using FCR[7:6]. The interrupt trigger level and upper flow control trigger level where appropriate are defined by L1 in the table below. L2 defines the lower flow control trigger level. Separate upper and lower flow control trigger levels introduce a hysteresis element in in-band and out-of-band flow control (see section 7.9). In Byte mode (450 mode) the trigger levels are all set to 1.

950 mode:
In similar fashion to for transmitter trigger levels, setting ACR[5]=1 enables 950-mode receiver trigger levels. FCR[7:6] are ignored.

FCR [7:6]	Mode					
	550 *FIFO Size 16*		Ext. 550 / 750 *FIFO Size 128*		650 *FIFO Size 128*	
	L1	L2	L1	L2	L1	L2
00	1	n/a	1	1	16	1
01	4	n/a	32	1	32	16
10	8	n/a	64	1	112	32
11	14	n/a	112	1	120	112

Table 20: Compatible Receiver Trigger Levels

A receiver data interrupt will be generated (if enabled) if the Receiver FIFO Level ('RFL') reaches the upper trigger level.

7.5 Line Control & Status

7.5.1 False Start Bit Detection

On the falling edge of a start bit, the receiver will wait for 1/2 bit and re-synchronise the receiver's sampling clock onto the centre of the start bit. The start bit is valid if the SIN line is still low at this mid-bit sample and the receiver will proceed to read in a data character. Verifying the start bit prevents noise generating spurious character generation. Once the first stop bit has been sampled, the received data is transferred to the RHR and the receiver will then wait for a low transition on SIN (signifying the next start bit).

The receiver will continue receiving data even if the RHR is full or the receiver has been disabled (see section 7.11.3) in order to maintain framing synchronisation. The only difference is that the received data does not get transferred to the RHR.

7.5.2 Line Control Register 'LCR'

The LCR specifies the data format that is common to both transmitter and receiver. Writing 0xBF to LCR enables access to the EFR, XON1, XOFF1, XON2 and XOFF2, DLL and DLM registers. This value (0xBF) corresponds to an unused data format. Writing the value 0xBF to LCR will set LCR[7] but leaves LCR[6:0] unchanged. Therefore, the data format of the transmitter and receiver data is not affected. Write the desired LCR value to exit from this selection.

LCR[1:0]: Data length
LCR[1:0] Determines the data length of serial characters. Note however, that these values are ignored in 9-bit data framing mode, i.e. when NMR[0] is set.

LCR[1:0]	Data length
00	5 bits
01	6 bits
10	7 bits
11	8 bits

Table 21: LCR Data Length Configuration

LCR[2]: Number of stop bits
LCR[2] defines the number of stop bits per serial character.

LCR[2]	Data length	No. stop bits
0	5,6,7,8	1
1	5	1.5
1	6,7,8	2

Table 22: LCR Stop Bit Number Configuration

LCR[5:3]: Parity type
The selected parity type will be generated during transmission and checked by the receiver, which may produce a parity error as a result. In 9-bit mode parity is disabled and LCR[5:3] is ignored.

LCR[5:3]	Parity type
xx0	No parity bit
001	Odd parity bit
011	Even parity bit
101	Parity bit forced to 1
111	Parity bit forced to 0

Table 23: LCR Parity Configuration

LCR[6]: Transmission break
logic 0 ⇒Break transmission disabled.
logic 1 ⇒Forces the transmitter data output SOUT low to alert the communication terminal, or send zeros in IrDA mode.

It is the responsibility of the software driver to ensure that the break duration is longer than the character period for it to be recognised remotely as a break rather than data.

LCR[7]: Divisor latch enable
logic 0 ⇒Access to DLL and DLM registers disabled.
logic 1 ⇒Access to DLL and DLM registers enabled.

7.5.3 Line Status Register 'LSR'

This register provides the status of data transfer to CPU.

LSR[0]: RHR data available
logic 0 ⇒ RHR is empty: no data available
logic 1 ⇒ RHR is not empty: data is available to be read.

LSR[1]: RHR overrun error
logic 0 ⇒ No overrun error.
logic 1 ⇒ Data was received when the RHR was full. An overrun error has occurred. The error is flagged when the data would normally have been transferred to the RHR.

LSR[2]: Received data parity error
logic 0 ⇒ No parity error in normal mode or 9th bit of received data is '0' in 9-bit mode.
logic 1 ⇒ Data has been received that did not have correct parity in normal mode or 9th bit of received data is '1' in 9-bit mode.

The Parity error flag will be set when the data item in error is at the top of the RHR and cleared following a read of the LSR. In 9-bit mode LSR[2] is no longer a flag and corresponds to the 9th bit of the received data in RHR.

LSR[3]: Received data framing error
logic 0 ⇒ No framing error.
logic 1 ⇒ Data has been received with an invalid stop bit.

This status bit is set and cleared in the same manner as LSR[2]. When a framing error occurs, the UART will try to re-synchronise by assuming that the error was due to sampling the start bit of the next data item.

LSR[4]: Received break error
logic 0 ⇒ No receiver break error.
logic 1 ⇒ The receiver received a break.

A break condition occurs when the SIN line goes low (normally signifying a start bit) and stays low throughout the start, data, parity and first stop bit. (Note that the SIN line is sampled at the bit rate). One zero character with associated break flag set will be transferred to the RHR and the receiver will then wait until the SIN line returns high. The LSR[4] break flag will be set when this data item gets to the top of the RHR and it is cleared following a read of the LSR.

LSR[5]: THR empty
logic 0 ⇒ Transmitter FIFO (THR) is not empty.
logic 1 ⇒ Transmitter FIFO (THR) is empty.

LSR[6]: Transmitter and THR empty
logic 0 ⇒ The transmitter is not idle
logic 1 ⇒ THR is empty and the transmitter has completed the character in shift register and is in idle mode. (I.e. set whenever the transmitter shift register and the THR are both empty.)

LSR[7]: Receiver data error
logic 0 ⇒ Either there are no receiver data errors in the FIFO or it was cleared by a read of LSR.
logic 1 ⇒ At least one parity error, framing error or break indication in the FIFO.

In 450 mode LSR[7] is permanently cleared, otherwise this bit will be set when an erroneous character is transferred from the receiver to the RHR. It is cleared when the LSR is read. **Note that in 16C550 this bit is only cleared when all of the erroneous data are removed from the FIFO**. In 9-bit data framing mode parity is permanently disabled, so this bit is not affected by LSR[2].

7.6 Interrupts & Sleep Mode

The serial channel interrupts are asserted on the PCI INTA# pin. The interrupts can be enabled or disabled using the GIS register interrupt mask (see section 6.4.8) and the IER register. Unlike generic 16C550 devices, the interrupt can not be disabled using the implementation-specific MCR[3].

7.6.1 Interrupt Enable Register 'IER'

Serial channel interrupts are enabled using the Interrupt Enable Register ('IER').

IER[0]: Receiver data available interrupt mask
logic 0 ⇒ Disable the receiver ready interrupt.
logic 1 ⇒ Enable the receiver ready interrupt.

IER[1]: Transmitter empty interrupt mask
logic 0 ⇒ Disable the transmitter empty interrupt.
logic 1 ⇒ Enable the transmitter empty interrupt.

IER[2]: Receiver status interrupt
Normal mode:
logic 0 ⇒ Disable the receiver status interrupt.
logic 1 ⇒ Enable the receiver status interrupt.
9-bit data mode:
logic 0 ⇒ Disable receiver status and address bit interrupt.
logic 1 ⇒ Enable receiver status and address bit interrupt.

In 9-bit mode (i.e. when NMR[0] is set), reception of a character with the address-bit (i.e. 9th bit) set can generate a level 1 interrupt if IER[2] is set.

IER[3]: Modem status interrupt mask
logic 0 ⇒ Disable the modem status interrupt.
logic 1 ⇒ Enable the modem status interrupt.

IER[4]: Sleep mode
logic 0 ⇒ Disable sleep mode.
logic 1 ⇒ Enable sleep mode whereby the internal clock of the channel is switched off.

Sleep mode is described in section 7.6.4.

IER[5]: Special character interrupt mask or alternate sleep mode
9-bit data framing mode:
logic 0 ⇒ Disable the received special character interrupt.
logic 1 ⇒ Enable the received special character interrupt.

In 9-bit data mode, The receiver can detect up to four special characters programmed in the Special Character Registers (see map on page 32). When IER[5] is set, a level 5 interrupt is asserted when the receiver character matches one of the values programmed.

650/950 modes (non-9-bit data framing):
logic 0 ⇒ Disable the special character receive interrupt.
logic 1 ⇒ Enable the special character receive interrupt.

In 16C650 compatible mode when the device is in Enhanced mode (EFR[4]=1), this bit enables the detection of special characters. It enables both the detection of XOFF characters (when in-band flow control is enabled via EFR[3:0]) and the detection of the XOFF2 special character (when enabled via EFR[5]).

750 mode (non-9-bit data framing):
logic 0 ⇒ Disable alternate sleep mode.
logic 1 ⇒ Enable alternate sleep mode whereby the internal clock of the channel is switched off.

In 16C750 compatible mode (i.e. non-Enhanced mode), this bit is used an alternate sleep mode and has the same effect as IER[4].

IER[6]: RTS interrupt mask
logic 0 ⇒ Disable the RTS interrupt.
logic 1 ⇒ Enable the RTS interrupt.

This enable is only operative in Enhanced mode (EFR[4]=1). In non-Enhanced mode, RTS interrupt is permanently enabled

IER[7]: CTS interrupt mask
logic 0 ⇒ Disable the CTS interrupt.
logic 1 ⇒ Enable the CTS interrupt.

This enable is only operative in Enhanced mode (EFR[4]=1). In non-Enhanced mode, CTS interrupt is permanently enabled.

7.6.2 Interrupt Status Register 'ISR'

The source of the highest priority interrupt pending is indicated by the contents of the Interrupt Status Register 'ISR'. There are nine sources of interrupt at six levels of priority (1 is the highest) as shown in Table 24.

Level	Interrupt source	ISR[5:0] *see note 3*
-	No interrupt pending [1]	000001
1	Receiver status error **or** Address-bit detected in 9-bit mode	000110
2a	Receiver data available	000100
2b	Receiver time-out	001100
3	Transmitter THR empty	000010
4	Modem status change	000000
5 [2]	In-band flow control XOFF **or** Special character (XOFF2) **or** Special character 1, 2, 3 or 4 **or** bit 9 set in 9-bit mode	010000
6 [2]	CTS or RTS change of state	100000

Table 24: Interrupt Status Identification Codes

Note1: ISR[0] indicates whether any interrupts are pending.
Note2: Interrupts of priority levels 5 and 6 cannot occur unless the UART is in Enhanced mode.
Note3: ISR[5] is only used in 650 & 950 modes. In 750 mode, it is '0' when FIFO size is 16 and '1' when FIFO size is 128. In all other modes it is permanently set to 0

7.6.3 Interrupt Description

Level 1:

Receiver status error interrupt (ISR[5:0]='000110'):

Normal (non-9-bit) mode:

This interrupt is active whenever any of LSR[1], LSR[2], LSR[3] or LSR[4] are set. These flags are cleared following a read of the LSR. This interrupt is masked with IER[2].

9-bit mode:

This interrupt is active whenever any of LSR[1], LSR[2], LSR[3] or LSR[4] are set. The receiver error interrupt due to LSR[1], LSR[3] and LSR[4] is masked with IER[3]. The 'address-bit' received interrupt is masked with NMR[1]. The software driver can differentiate between receiver status error and received address-bit (9th data bit) interrupt by examining LSR[1] and LSR[7]. In 9-bit mode LSR[7] is only set when LSR[3] or LSR[4] is set and it is not affected by LSR[2] (i.e. 9th data bit).

Level 2a:

Receiver data available interrupt (ISR[5:0]='000100'):

This interrupt is active whenever the receiver FIFO level is above the interrupt trigger level.

Level 2b:

Receiver time-out interrupt (ISR[5:0]='001100'):

A receiver time-out event, which may cause an interrupt, will occur when all of the following conditions are true:

- The UART is in a FIFO mode
- There is data in the RHR.
- There has been no read of the RHR for a period of time greater than the time-out period.
- There has been no new data written into the RHR for a period of time greater than the time-out period. The time-out period is four times the character period (including start and stop bits) measured from the centre of the first stop bit of the last data item received.

Reading the first data item in RHR clears this interrupt.

Level 3:

Transmitter empty interrupt (ISR[5:0]='000010'):

This interrupt is set when the transmit FIFO level falls below the trigger level. It is cleared on an ISR read of a level 3 interrupt or by writing more data to the THR so that the trigger level is exceeded. Note that when 16C950 mode trigger levels are enabled (ACR[5]=1) and the transmitter trigger level of zero is selected (TTL=0x00), a transmitter empty interrupt will only be asserted when both the transmitter FIFO and transmitter shift register are empty and the SOUT line has returned to idle marking state.

Level 4:

Modem change interrupt (ISR[5:0]='000000'):

This interrupt is set by a modem change flag (MSR[0], MSR[1], MSR[2] or MSR[3]) becoming active due to changes in the input modem lines. This interrupt is cleared following a read of the MSR.

Level 5:

Receiver in-band flow control (XOFF) detect interrupt, Receiver special character (XOFF2) detect interrupt, Receiver special character 1, 2, 3 or 4 interrupt or 9th Bit set interrupt in 9-bit mode (ISR[5:0]='010000'):

A level 5 interrupt can only occur in Enhanced-mode when any of the following conditions are met:

- A valid XOFF character is received while in-band flow control is enabled.
- A received character matches XOFF2 while special character detection is enabled, i.e. EFR[5]=1.
- A received character matches special character 1, 2, 3 or 4 in 9-bit mode (see section 7.11.9).

It is cleared on an ISR read of a level 5 interrupt.

Level 6:
CTS or RTS changed interrupt (ISR[5:0]='100000'):
This interrupt is set whenever any of the CTS# or RTS# pins changes state from low to high. It is cleared on an ISR read of a level 6 interrupt.

7.6.4 Sleep Mode

For a channel to go into sleep mode, all of the following conditions must be met:

- Sleep mode enabled (IER[4]=1 in 650/950 modes, or IER[5]=1 in 750 mode):
- The transmitter is idle, i.e. the transmitter shift register and FIFO are both empty.
- SIN is high.
- The receiver is idle.
- The receiver FIFO is empty (LSR[0]=0).
- The UART is not in loopback mode (MCR[4]=0).
- Changes on modem input lines have been acknowledged (i.e. MSR[3:0]=0000).
- No interrupts are pending.

A read of IER[4] (or IER[5] if a 1 was written to that bit instead) shows whether the power-down request was successful. The UART will retain its programmed state whilst in power-down mode.
The channel will automatically exit power-down mode when any of the conditions 1 to 7 becomes false. It may be woken manually by clearing IER[4] (or IER[5] if the alternate sleep mode is enabled).

Sleep mode operation is not available in IrDA mode.

7.7 Modem Interface

7.7.1 Modem Control Register 'MCR'

MCR[0]: DTR
logic 0 ⇒ Force DTR# output to inactive (high).
logic 1 ⇒ Force DTR# output to active (low).

Note that DTR# can be used for automatic out-of-band flow control when enabled using ACR[4:3] (see section 7.11.3).

MCR[1]: RTS
logic 0 ⇒ Force RTS# output to inactive (high).
logic 1 ⇒ Force RTS# output to active (low).

Note that RTS# can be used for automatic out-of-band flow control when enabled using EFR[6] (see section 7.9.4).

MCR[2]: OUT1
logic 0 ⇒ Force OUT1# output low when loopback mode is disabled.
logic 1 ⇒ Force OUT1# output high.

MCR[3]: OUT2/External interrupt enable
logic 0 ⇒ Force OUT2# output low when loopback mode is disabled. If INT_SEL# is low the external interrupt is in high-impedance state when MCR[3] is cleared. If INT_SEL# is high MCR[3] does not affect the interrupt.
logic 1 ⇒ Force OUT2# output high. If INT_SEL# is low the external interrupt is enabled and operating in normal active (forcing) mode when MCR[3] is high. If INT_SEL# is high MCR[3] does not affect the interrupt.

MCR[4]: Loopback mode
logic 0 ⇒ Normal operating mode.
logic 1 ⇒ Enable local loop-back mode (diagnostics).

In local loop-back mode, the transmitter output (SOUT) and the four modem outputs (DTR#, RTS#, OUT1# and OUT2#) are set in-active (high), and the receiver inputs SIN, CTS#, DSR#, DCD#, and RI# are all disabled. Internally the transmitter output is connected to the receiver input and DTR#, RTS#, OUT1# and OUT2# are connected to modem status inputs DSR#, CTS#, RI# and DCD# respectively.

In this mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four modem status inputs. The interrupts are still controlled by the IER.

MCR[5]: Enable XON-Any in Enhanced mode or enable out-of-band flow control in non-Enhanced mode

650/950 (enhanced) modes:
logic 0 ⇒ XON-Any is disabled.
logic 1 ⇒ XON-Any is enabled.

In enhanced mode (EFR[4]=1), this bit enables the Xon-Any operation. When Xon-Any is enabled, any received data will be accepted as a valid XON (see in-band flow control, section 7.9.3).

750 (normal) mode:
logic 0 ⇒ CTS/RTS flow control disabled.
logic 1 ⇒ CTS/RTS flow control enabled.

In non-enhanced mode, this bit enables the CTS/RTS out-of-band flow control.

MCR[6]: IrDA mode
logic 0 ⇒ Standard serial receiver and transmitter data format.
logic 1 ⇒ Data will be transmitted and received in IrDA format.

This function is only available in Enhanced mode. It requires a 16x clock to function correctly.

MCR[7]: Baud rate prescaler select
logic 0 ⇒ Normal (divide by 1) baud rate generator prescaler selected.
logic 1 ⇒ Divide-by-"M+N/8" baud rate generator prescaler selected.

where M & N are programmed in CPR (ICR offset 0x01). After a hardware reset, CPR defaults to 0x20 (divide-by-4) and MCR[7] is reset. User writes to this flag will only take effect in Enhanced mode. See section 7.9.1.

7.7.2 Modem Status Register 'MSR'

MSR[0]: Delta CTS#
Indicates that the CTS# input has changed since the last time the MSR was read.

MSR[1]: Delta DSR#
Indicates that the DSR# input has changed since the last time the MSR was read.

MSR[2]: Trailing edge RI#
Indicates that the RI# input has changed from low to high since the last time the MSR was read.

MSR[3]: Delta DCD#
Indicates that the DCD# input has changed since the last time the MSR was read.

MSR[4]: CTS
This bit is the complement of the CTS# input. It is equivalent to RTS (MCR[1]) in internal loop-back mode.

MSR[5]: DSR
This bit is the complement of the DSR# input. It is equivalent to DTR (MCR[0]) in internal loop-back mode.

MSR[6]: RI
This bit is the complement of the RI# input. In internal loop-back mode it is equivalent to the internal OUT1.

MSR[7]: DCD
This bit is the complement of the DCD# input. In internal loop-back mode it is equivalent to the internal OUT2.

7.8 Other Standard Registers

7.8.1 Divisor Latch Registers 'DLL & DLM'

The divisor latch registers are used to program the baud rate divisor. This is a value between 1 and 65535 by which the input clock is divided by in order to generate serial baud rates. After a hardware reset, the baud rate used by the transmitter and receiver is given by:

$$Baudrate = \frac{InputClock}{16 * Divisor}$$

Where divisor is given by DLL + (256 x DLM). More flexible baud rate generation options are also available. See section 7.10 for full details.

7.8.2 Scratch Pad Register 'SPR'

The scratch pad register does not affect operation of the rest of the UART in any way and can be used for temporary data storage. The register may also be used to define an offset value to access the registers in the Indexed Control Register set. For more information on Indexed Control registers see sections 7.2 and 7.11.

7.9 Automatic Flow Control

Automatic in-band flow control, automatic out-of-band flow control and special character detection features can be used when in Enhanced mode (flow control is software compatible with the 16C654). Alternatively, 750-compatible automatic out-of-band flow control can be enabled when in non-Enhanced mode. In 950 mode, in-band and out-of-band flow controls are compatible with 16C654 with the addition of fully programmable flow control thresholds.

7.9.1 Enhanced Features Register 'EFR'

Writing 0xBF to LCR enables access to the EFR and other Enhanced mode registers. This value corresponds to an unused data format. Writing 0xBF to LCR will set LCR[7] but leaves LCR[6:0] unchanged. Therefore, the data format of the transmitter and receiver data is not affected. Write the desired LCR value to exit from this selection.

Note: In-band transmit and receive flow control is disabled in 9-bit mode.

EFR[1:0]: In-band receive flow control mode
When in-band receive flow control is enabled, the UART compares the received data with the programmed XOFF character(s). When this occurs, the UART will disable transmission as soon as any current character transmission is complete. The UART then compares the received data with the programmed XON character(s). When a match occurs, the UART will re-enable transmission (see section 7.11.6).

For automatic in-band flow control, bit 4 of EFR must be set. The combinations of software receive flow control can be selected by programming EFR[1:0] as follows:

logic [00] ⇒ In-band receive flow control is disabled.
logic [01] ⇒ Single character in-band receive flow control enabled, recognising XON2 as the XON character and XOFF2 as the XOFF character.
logic [10] ⇒ Single character in-band receive flow control enabled, recognising XON1 as the XON character and XOFF1 and the XOFF character.
logic [11] ⇒ The behaviour of the receive flow control is dependent on the configuration of EFR[3:2]. Single character in-band receive flow control is enabled, accepting XON1 or XON2 as valid XON characters and XOFF1 or XOFF2 as valid XOFF characters when EFR[3:2] = "01" or "10". EFR[1:0] should not be set to "11" when EFR[3:2] is '00'.

EFR[3:2]: In-band transmit flow control mode
When in-band transmit flow control is enabled, XON/XOFF character(s) are inserted into the data stream whenever the RFL passes the upper trigger level and falls below the lower trigger level respectively.

For automatic in-band flow control, bit 4 of EFR must be set. The combinations of software transmit flow control can then be selected by programming EFR[3:2] as follows:

logic [00] ⇒ In-band transmit flow control is disabled.
logic [01] ⇒ Single character in-band transmit flow control enabled, using XON2 as the XON character and XOFF2 as the XOFF character.
logic [10] ⇒ Single character in-band transmit flow control enabled, using XON1 as the XON character and XOFF1 as the XOFF character.
logic[11] ⇒ The value EFR[3:2] = "11" is reserved for future use and should not be used

EFR[4]: Enhanced mode
logic 0 ⇒ Non-Enhanced mode. Disables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7 and in-band flow control. Whenever this bit is cleared, the setting of other bits of EFR are ignored.
logic 1 ⇒ Enhanced mode. Enables the Enhanced Mode functions. These functions include enabling IER bits 4-7, FCR bits 4-5, MCR bits 5-7. For in-band flow control the software driver must set this bit first. If this bit is set, out-of-band flow control is configured with EFR bits 6-7, otherwise out-of-band flow control is compatible with 16C750.

EFR[5]: Enable special character detection
logic 0 ⇒ Special character detection is disabled.
logic 1 ⇒ While in Enhanced mode (EFR[4]=1), the UART compares the incoming receiver data with the XOFF2 value. Upon a correct match, the received data will be transferred to the RHR and a level 5 interrupt (XOFF or special character) will be asserted if level 5 interrupts are enabled (IER[5] set to 1).

EFR[6]: Enable automatic RTS flow control.
logic 0 ⇒ RTS flow control is disabled (default).
logic 1 ⇒ RTS flow control is enabled in Enhanced mode (i.e. EFR[4] = 1), where the RTS# pin will be forced inactive high if the RFL reaches the upper flow control threshold. This will be released when the RFL drops below the lower threshold. 650 and 950-mode drivers should use this bit to enable RTS flow control.

EFR[7]: Enable automatic CTS flow control.

logic 0 ⇒ CTS flow control is disabled (default).

logic 1 ⇒ CTS flow control is enabled in Enhanced mode (i.e. EFR[4] = 1), where the data transmission is prevented whenever the CTS# pin is held inactive high. 650 and 950-mode drivers should use this bit to enable CTS flow control.

A 750-mode driver should set MCR[5] to enable RTS/CTS flow control.

7.9.2 Special Character Detection

In Enhanced mode (EFR[4]=1), when special character detection is enabled (EFR[5]=1) and the receiver matches received data with XOFF2, the 'received special character' flag ASR[4] will be set and a level 5 interrupt is asserted, if enabled by IER[5]. This flag will be cleared following a read of ASR. The received status (i.e. parity and framing) of special characters does not have to be valid for these characters to be accepted as valid matches.

7.9.3 Automatic In-band Flow Control

When in-band receive flow control is enabled, the UART will compare the received data with XOFF1 or XOFF2 characters to detect an XOFF condition. When this occurs, the UART will disable transmission as soon as any current character transmission is complete. Status bits ISR[4] and ASR[0] will be set. A level 5 interrupt will occur (if enabled by IER[5]). The UART will then compare all received data with XON1 or XON2 characters to detect an XON condition. When this occurs, the UART will re-enable transmission and status bits ISR[4] and ASR[0] will be cleared.

Any valid XON/XOFF characters will not be written into the RHR. An exception to this rule occurs if special character detection is enabled and an XOFF2 character is received that is a valid XOFF. In this instance, the character will be written into the RHR.

The received status (i.e. parity and framing) of XON/XOFF characters does not have to be valid for these characters to be accepted as valid matches.

When the 'XON Any' flag (MCR[5]) is set, any received character is accepted as a valid XON condition and the transmitter will be re-enabled. The received data will be transferred to the RHR.

When in-band transmit flow control is enabled, the RFL will be sampled whenever the transmitter is idle (briefly, between characters, or when the THR is empty) and an XON/XOFF character will be inserted into the data stream if needed. Initially, remote transmissions are enabled and hence ASR[1] is clear. If ASR[1] is clear and the RFL has passed the upper trigger level (i.e. is above the trigger level), XOFF will be sent and ASR[1] will be set. If ASR[1] is set and the RFL falls below the lower trigger level, XON will be sent and ASR[1] will be cleared.

If transmit flow control is disabled after an XOFF has been sent, an XON will be sent automatically.

7.9.4 Automatic Out-of-band Flow Control

Automatic RTS/CTS flow control is selected by different means, depending on whether the UART is in Enhanced or non-Enhanced mode. When in non-Enhanced mode, MCR[5] enables both RTS and CTS flow control. When in Enhanced mode, EFR[6] enables automatic RTS flow control and EFR[7] enables automatic CTS flow control. This allows software compatibility with both 16C650 and 16C750 drivers.

When automatic CTS flow control is enabled and the CTS# input becomes active, the UART will disable transmission as soon as any current character transmission is complete. Transmission is resumed whenever the CTS# input becomes inactive.

When automatic RTS flow control is enabled, the RTS# pin will be forced inactive when the RFL reaches the upper trigger level and will return to active when the RFL falls below the lower trigger level. The automatic RTS# flow control is ANDed with MCR[1] and hence is only operational when MCR[1]=1. This allows the software driver to override the automatic flow control and disable the remote transmitter regardless by setting MCR[1]=0 at any time.

Automatic DTR/DSR flow control behaves in the same manner as RTS/CTS flow control but is enabled by ACR[3:2], regardless of whether or not the UART is in Enhanced mode.

7.10 Baud Rate Generation

7.10.1 General Operation

The UART contains a programmable baud rate generator that is capable of taking any clock input from 1.8432MHz to 60MHz and dividing it by any 16-bit divisor number from 1 to 65535 written into the DLM (MSB) and DLL (LSB) registers. In addition to this, a clock prescaler register is provided which can further divide the clock by values in the range 1.0 to 31.875 in steps of 0.125. Also, a further feature is the Times Clock Register 'TCR' which allows the sampling clock to be set to any value between 4 and 16.

These clock options allow for highly flexible baud rate generation capabilities from almost any input clock frequency (up to 60MHz). The actual transmitter and receiver baud rate is calculated as follows:

$$BaudRate = \frac{InputClock}{SC * Divisor * prescaler}$$

Where:
SC = Sample clock values defined in TCR[3:0]
Divisor = DLL + (256 x DLM)
Prescaler = 1 when MCR[7] = '0' else:
= M + (N / 8) where:
M = CPR[7:3] (Integer part – 1 to 31)
N = CPR[2:0] (Fractional part – 0.000 to 0.875)

After a hardware reset, the precaler is bypassed (set to 1) and TCR is set to 0x00 (i.e. SC = 16). Assuming this default configuration, the following table gives the divisors required to be programmed into the DLL and DLM registers in order to obtain various standard baud rates:

DLM:DLL Divisor Word	Baud Rate (bits per second)
0x0900	50
0x0300	110
0x0180	300
0x00C0	600
0x0060	1,200
0x0030	2,400
0x0018	4,800
0x000C	9,600
0x0006	19,200
0x0004	28,800
0x0003	38,400
0x0002	57,600
0x0001	115,200

Table 25: Standard PC COM Port Baud Rate Divisors (assuming a 1.8432MHz crystal)

7.10.2 Clock Prescaler Register 'CPR'

The CPR register is located at offset 0x01 of the ICR

The prescaler divides the system clock by any value in the range of 1 to "31 7/8" in steps of 1/8. The divisor takes the form "M+N/8", where M is the 5 bit value defined in CPR[7:3] and N is the 3 bit value defined in CPR[2:0].

The prescaler is by-passed and a prescaler value of '1' is selected by default when MCR[7] = 0.

Note that since access to MCR[7] is restricted to Enhanced mode only, EFR[4] should first be set and then MCR[7] set or cleared as required.

For higher baud rates use a higher frequency clock, e.g. 14.7456MHz, 18.432MHz, 32MHz, 40MHz or 60.0MHz. The flexible prescaler allows system designers to use clocks that are not integer multiples of popular baud rates; when using a non-standard clock frequency, compatibility with existing 16C550 software drivers may be maintained with a minor software patch to program the on-board prescaler to divide the high frequency clock down to 1.8432MHz.

Table 27 on the following page gives the prescaler values required to operate the UARTs at compatible baud rates with various different crystal frequencies. Also given is the maximum available baud rates in TCR = 16 and TCR = 4 modes with CPR = 1.

7.10.3 Times Clock Register 'TCR'

The TCR register is located at offset 0x02 of the ICR

The 16C550 and other compatible devices such as 16C650 and 16C750 use a 16 times (16x) over-sampling channel clock. The 16x over-sampling clock means that the channel clock runs at 16 times the selected serial bit rate. It limits the highest baud rate to 1/16 of the system clock when using a divisor latch value of unity. However, the 16C950 UART is designed in a manner to enable it to accept other multiplications of the bit rate clock. It can use values from 4x to 16x clock as programmed in the TCR as long as the clock (oscillator) frequency error, stability and jitter are within reasonable parameters. Upon hardware reset the TCR is reset to 0x00 which means that a 16x clock will be used, for compatibility with the 16C550 and compatibles.

The maximum baud-rates available for various system clock frequencies at all of the allowable values of TCR are indicated in Table 28 on the following page. These are the

values in bits-per-second (bps) that are obtained if the divisor latch = 0x01 and the Prescaler is set to 1.

The OX16PCI954 has the facility to operate at baud-rates up to 15 Mbps in normal mode.

Table 26 indicates how the value in the register corresponds to the number of clock cycles per bit. TCR[3:0] is used to program the clock. TCR[7:4] are unused and will return "0000" if read.

TCR[3:0]	Clock cycles per bit
0000 to 0011	16
0100 to 1111	4-15

Table 26: TCR Sample Clock Configuration

Use of the TCR does not require the device to be in 650 or 950 mode although only drivers that have been written to take advantage of the 950 mode features will be able to access this register. Writing 0x01 to the TCR will not switch the device into 1x isochronous mode, this is explained in the following section. (TCR has no effect in isochronous mode). If 0x01, 0x10 or 0x11 is written to TCR the device will operate in 16x mode.

Reading TCR will always return the last value that was written to it irrespective of mode of operation.

Clock Frequency (MHz)	CPR value	Effective crystal frequency	Error from 1.8432MHz (%)	Max. Baud rate with CPR = 1, TCR = 16	Max. Baud rate with CPR = 1, TCR = 4
1.8432	0x08 (1)	1.8432	0.00	115,200	460,800
7.3728	0x20 (4)	1.8432	0.00	460,800	1,843,200
14.7456	0x40 (8)	1.8432	0.00	921,600	3,686,400
18.432	0x50 (10)	1.8432	0.00	1,152,000	4,608,000
32.000	0x8B (17.375)	1.8417	0.08	2,000,000	8,000,000
33.000	0x8F (17.875)	1.8462	0.16	2,062,500	8,250,000
40.000	0xAE (21.75)	1.8391	0.22	2,500,000	10,000,000
50.000	0xD9 (27.125)	1.8433	0.01	3,125,000	12,500,000
60.000	0xFF (31.875)	1.8824	2.13	3,750,000	15,000,000

Table 27: Example clock options and their associated maximum baud rates

Sampling Clock	TCR Value	System Clock (MHz)							
		1.8432	7.372	14.7456	18.432	32	40	50	60
16	0x00	115,200	460,750	921,600	1.152M	2.00M	2.50M	3.125M	3.75M
15	0x0F	122,880	491,467	983,040	1,228,800	2,133,333	2,666,667	3,333,333	4.00M
14	0x0E	131,657	526,571	1,053,257	1,316,571	2,285,714	2,857,143	3,571,429	4,285,714
13	0x0D	141,785	567,077	1,134,277	1,417,846	2,461,538	3,076,923	3,846,154	4,615,384
12	0x0C	153,600	614,333	1,228,800	1,536,000	2,666,667	3,333,333	4,166,667	5.00M
11	0x0B	167,564	670,182	1,340,509	1,675,636	2,909,091	3,636,364	4,545,455	5,454545
10	0x0A	184,320	737,200	1,474,560	1,843,200	3.20M	4.00M	5.00M	6.00M
9	0x09	204,800	819,111	1,638,400	2,048,000	3,555,556	4,444,444	5,555,556	6,666,667
8	0x08	230,400	921,500	1,843,200	2,304,000	4.00M	5.00M	6.25M	7.50M
7	0x07	263,314	1,053,143	2,106,514	2,633,143	4,571,429	5,714,286	7,142,857	8,571428
6	0x06	307,200	1,228,667	2,457,600	3,072,000	5,333,333	6,666,667	8,333,333	10.00M
5	0x05	368,640	1,474,400	2,949,120	3,686,400	6.40M	8.00M	10.00M	12.00M
4	0x04	460,800	1,843,000	3,686,400	4,608,000	8.00M	10.00M	12.50M	15.00M

Table 28: Maximum Baud Rates Available at all 'TCR' Sampling Clock Values

7.10.4 External 1x Clock Mode

The transmitter and receiver can accept an external clock applied to the RI# and DSR# pins respectively. The clock options are selected using the CKS register (see section 7.11.8). The transmitter and receiver may be configured to operate in 1x (i.e. Isochronous mode) by setting CKS[7] and CKS[3], respectively. In Isochronous mode, transmitter or receiver will use the 1x clock (usually, but not necessarily, an external source) where asynchronous framing is maintained using start-, parity- and stop-bits. However serial transmission and reception is synchronised to the 1x clock. In this mode asynchronous data may be transmitted at baud rates up to 60Mbps. The local 1x clock source can be asserted on the DTR# pin.

Note that line drivers need to be capable of transmission at data rates twice the system clock used (as one cycle of the system clock corresponds to 1 bit of serial data). Also note that enabling modem interrupts is illegal in isochronous mode, as the clock signal will cause a continuous change to the modem status (unless masked in MDM register, see section 7.11.10).

7.10.5 Crystal Oscillator Circuit

The UARTs reference reference clock may be provided by its own crystal oscillator or directly from a clock source connected to the XTLI pin. The circuit required to use the internal oscillator is shown in Figure 3.

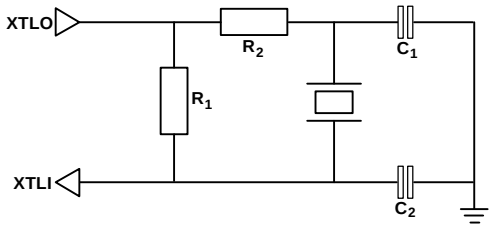


Figure 3: Crystal Oscillator Circuit

Frequency Range (MHz)	C_1 (pF)	C_2 (pF)	R_1 (Ω)	R_2 (Ω)
1.8432 - 8	68	22	220k	470R
8-60	33-68	33 – 68	220k-2M2	470R

Table 29: Component values

Note: For better stability use a smaller value of R_1. Increase R_1 to reduce power consumption.
The total capacitive load (C1 in series with C2) should be that specified by the crystal manufacturer (nominally 16pF).

7.11 Additional Features

7.11.1 Additional Status Register 'ASR'

ASR[0]: Transmitter disabled

logic 0 ⇒ The transmitter is not disabled by in-band flow control.

logic 1 ⇒ The receiver has detected an XOFF, and has disabled the transmitter.

This bit is cleared after a hardware reset or channel software reset. The software driver may write a 0 to this bit to re-enable the transmitter if it was disabled by in-band flow control. Writing a 1 to this bit has no effect.

ASR[1]: Remote transmitter disabled

logic 0 ⇒ The remote transmitter is not disabled by in-band flow control.

logic 1 ⇒ The transmitter has sent an XOFF character, to disable the remote transmitter (cleared when subsequent XON is sent).

This bit is cleared after a hardware reset or channel software reset. The software driver may write a 0 to this bit to re-enable the remote transmitter (an XON is transmitted). Note: writing a 1 to this bit has no effect.

ASR[2]: RTS

This is the complement of the actual state of the RTS# pin when the device is not in loopback mode. The driver software can determine if the remote transmitter is disabled by RTS# out-of-band flow control by reading this bit. In loopback mode this bit reflects the flow control status rather than the pin's actual state.

ASR[3]: DTR

This is the complement of the actual state of the DTR# pin when the device is not in loopback mode. The driver software can determine if the remote transmitter is disabled by DTR# out-of-band flow control by reading this bit. In loopback mode this bit reflects the flow control status rather than the pin's actual state.

ASR[4]: Special character detected

logic 0 ⇒ No special character has been detected.

logic 1 ⇒ A special character has been received and is stored in the RHR.

This can be used to determine whether a level 5 interrupt was caused by receiving a special character rather than an XOFF. The flag is cleared following the read of the ASR.

ASR[5]: FIFOSEL
This bit reflects the unlatched state of the FIFOSEL pin.

ASR[6]: FIFO size
logic 0 ⇒FIFOs are 16 deep if FCR[0] = 1.
logic 1 ⇒FIFOs are 128 deep if FCR[0] = 1.

ASR[7]: Transmitter Idle
logic 0 ⇒Transmitter is transmitting.
logic 1 ⇒Transmitter is idle.

This bit reflects the state of the internal transmitter. It is set when both the transmitter FIFO and shift register are empty.

7.11.2 FIFO Fill levels 'TFL & RFL'

The number of characters stored in the THR and RHR can be determined by reading the TFL and RFL registers respectively. When data transfer is in constant operation, the values should be interpreted as follows:

1. The number of characters in the THR is no greater than the value read back from TFL.
2. The number of characters in the RHR is no less than the value read back from RFL.

7.11.3 Additional Control Register 'ACR'

The ACR register is located at offset 0x00 of the ICR

ACR[0]: Receiver disable
logic 0 ⇒ The receiver is enabled, receiving data and storing it in the RHR.
logic 1 ⇒ The receiver is disabled. The receiver continues to operate as normal to maintain the framing synchronisation with the receive data stream but received data is not stored into the RHR. In-band flow control characters continue to be detected and acted upon. Special characters will not be detected.
Changes to this bit will only be recognised following the completion of any data reception pending.

ACR[1]: Transmitter disable
logic 0 ⇒ The transmitter is enabled, transmitting any data in the THR.
logic 1 ⇒ The transmitter is disabled. Any data in the THR is not transmitted but is held. However, in-band flow control characters may still be transmitted.
Changes to this bit will only be recognised following the completion of any data transmission pending.

ACR[2]: Enable automatic DSR flow control
logic 0 ⇒ Normal. The state of the DSR# line does not affect the flow control.
logic 1 ⇒ Data transmission is prevented whenever the DSR# pin is held inactive high.

This bit provides another automatic out-of-band flow control facility using the DSR# line.

ACR[4:3]: DTR# line configuration
When bits 4 or 5 of CKS (offset 0x03 of ICR) are set, the transmitter 1x clock or the output of the baud rate generator (Nx clock) are asserted on the DTR# pin, otherwise the DTR# pin is defined as follows:

logic [00] ⇒ DTR# is compatible with 16C450, 16C550, 16C650 and 16C750 (i.e. normal).
logic [01] ⇒ DTR# pin is used for out-of-band flow control. It will be forced inactive high if the Receiver FIFO Level ('RFL') reaches the upper flow control threshold. DTR# line will be re-activated (=0) when the RFL drops below the lower threshold (see FCL & FCH).
logic [10] ⇒ DTR# pin is configured to drive the active-low enable pin of an external RS485 buffer. In this configuration the DTR# pin will be forced low whenever the transmitter is not empty (LSR[6]=0), otherwise DTR# pin is high.
logic [11] ⇒ DTR# pin is configured to drive the active-high enable pin of an external RS485 buffer. In this configuration, the DTR# pin will be forced high whenever the transmitter is not empty (LSR[6]=0), otherwise DTR# pin is low.

If the user sets ACR[4], then the DTR# line is controlled by the status of the transmitter empty bit of LCR. When ACR[4] is set, ACR[3] is used to select active high or active low enable signals. In half-duplex systems using RS485 protocol, this facility enables the DTR# line to directly control the enable signal of external 3-state line driver buffers. When the transmitter is empty the DTR# would go inactive once the SOUT line returns to it's idle marking state.

ACR[5]: 950 mode trigger levels enable
logic 0 ⇒ Interrupts and flow control trigger levels are as described in FCR register and are compatible with 16C650/16C750 modes.
logic 1 ⇒ 16C950 specific enhanced interrupt and flow control trigger levels defined by RTL, TTL, FCL and FCH are enabled.

ACR[6]: ICR read enable
logic 0 ⇒ The Line Status Register is readable.
logic 1 ⇒ The Indexed Control Registers are readable.

Setting this bit will map the ICR set to the LSR location for reads. During normal operation this bit should be cleared.

ACR[7]: Additional status enable

logic 0 ⇒ Access to the ASR, TFL and RFL registers is disabled.

logic 1 ⇒ Access to the ASR, TFL and RFL registers is enabled.

When ACR[7] is set, the MCR, LCR and IER registers are no longer readable but remain writable, and the registers ASR, TFL and RFL replace them in the register map for read operations. The software driver may leave this bit set during normal operation, since MCR, LCR and IER do not generally need to be read.

7.11.4 Transmitter Trigger Level 'TTL'

The TTL register is located at offset 0x04 of the ICR

Whenever 950 trigger levels are enabled (ACR[5]=1), bits 4 and 5 of FCR are ignored and an alternative arbitrary transmitter interrupt trigger level can be defined in the TTL register. This 7-bit value provides a fully programmable transmitter interrupt trigger facility. In 950 mode, a priority level 3 interrupt occurs indicating that the transmitter buffer requires more characters when the interrupt is not masked (IER[1]=1) and the transmitter FIFO level falls below the value stored in the TTL register. The value 0 (0x00) has a special meaning. In 950 mode when the user writes 0x00 to the TTL register, a level 3 interrupt only occurs when the FIFO and the transmitter shift register are both empty and the SOUT line is in the idle marking state. This feature is particularly useful to report back the empty state of the transmitter after its FIFO has been flushed away.

7.11.5 Receiver Interrupt. Trigger Level 'RTL'

The RTL register is located at offset 0x05 of the ICR

Whenever 950 trigger levels are enabled (ACR[5]=1), bits 6 and 7 of FCR are ignored and an alternative arbitrary receiver interrupt trigger level can be defined in the RTL register. This 7-bit value provides a fully programmable receiver interrupt trigger facility as opposed to the limited trigger levels available in 16C650 and 16C750 devices. It enables the system designer to optimise the interrupt performance hence minimising the interrupt overhead.

In 950 mode, a priority level 2 interrupt occurs indicating that the receiver data is available when the interrupt is not masked (IER[0]=1) and the receiver FIFO level reaches the value stored in this register.

7.11.6 Flow Control Levels 'FCL' & 'FCH'

The FCL and FCH registers are located at offsets 0x06 and 0x07 of the ICR respectively

Enhanced software flow control using XON/XOFF and hardware flow control using RTS#/CTS# and DTR#/DSR# are available when 950 mode trigger levels are enabled (ACR[5]=1). Improved flow control threshold levels are offered using Flow Control Lower trigger level ('FCL') and Flow Control Higher trigger level ('FCH') registers to provide a greater degree of flexibility when optimising the flow control performance. Generally, these facilities are only available in Enhanced mode.

In 650 mode, in-band flow control is enabled using the EFR register. An XOFF character may be transmitted when the receiver FIFO exceeds the upper trigger level defined by FCR[7:6] as described in section 7.4.1. An XON is then sent when the FIFO is read down the lower fill level. The flow control is enabled and the appropriate mode is selected using EFR[3:0].

In 950 mode, the flow control thresholds defined by FCR[7:6] are ignored. In this mode, threshold levels are programmed using FCL and FCH. When flow control is enabled by EFR[3:0] and the receiver FIFO level ('RFL') reaches the value programmed in the FCH register, an XOFF will be transmitted to stop the flow of serial data as defined by EFR[3:0]. When the receiver FIFO level falls below the value programmed in FCL the flow is resumed by sending an XON character (as defined in EFR[3:0]). The FCL value of 0x00 is illegal.

CTS/RTS and DSR/DTR out-of-band flow control use the same trigger levels as in-band flow control. When out-of-band flow control is enabled, RTS# (or DTR#) line is de-asserted when the receiver FIFO level reaches the upper limit defined in the FCH and is re-asserted when the receiver FIFO is drained below a lower limit defined in FCL. When 950 trigger levels are enabled (ACR[5]=1), the CTS# flow control functions as in 650 mode and is configured by EFR[7]. However, RTS# is automatically de-asserted and re-asserted when EFR[6] is set and RFL reaches FCH and drops below FCL. DSR# flow control is configured with ACR[2]. DTR# flow control is configured with ACR[4:3].

7.11.7 Device Identification Registers

The identification registers is located at offsets 0x08 to 0x0B of the ICR

The UARTs offer four bytes of device identification. The device ID registers may be read using offset values 0x08 to 0x0B of the Indexed Control Register. Registers ID1, ID2 and ID3 identify the device as an OX16C950 and return 0x16, 0xC9 and 0x50 respectively. The REV register resides at offset 0x0B of ICR and identifies the revision of OX16C950. This register returns 0x01 for revision A of the OX16PCI954.

7.11.8 Clock Select Register 'CKS'

The CKS register is located at offset 0x03 of the ICR

This register is cleared to 0x00 after a hardware reset to maintain compatibility with 16C550, but is unaffected by software reset. This allows the user to select a clock source and then reset the channel to work-around any timing glitches.

CKS[1:0]: Receiver Clock Source Selector

logic [x0] ⇒ The output of baud rate generator (internal BDOUT#) is selected for the receiver clock.

logic [01] ⇒ The DSR# pin is selected for the receiver clock.

logic [11] ⇒ The transmitter clock is selected for the receiver. This allows RI# to be used for both transmitter and receiver.

CKS[2]: Reserved

CKS[3]: Receiver 1x clock mode selector

logic 0 ⇒ The receiver is in Nx clock mode as defined in the TCR register. After a hardware reset the receiver operates in 16x clock mode, i.e. 16C550 compatibility.

logic 1 ⇒ The receiver is in isochronous 1x clock mode.

CKS[5:4]: Transmitter 1x clock or baud rate generator output (BDOUT) on DTR# pin

logic [00] ⇒ The function of the DTR# pin is defined by the setting of ACR[4:3].

logic [01] ⇒ The transmitter 1x clock (bit rate clock) is asserted on the DTR# pin and the setting of ACR[4:3] is ignored.

logic [10] ⇒ The output of baud rate generator (Nx clock) is asserted on the DTR# pin and the setting of ACR[4:3] is ignored.

logic [11] ⇒ Reserved.

CKS[6]: Transmitter clock source selector

logic 0 ⇒ The transmitter clock source is the output of the baud rate generator (550 compatibility).

logic 1 ⇒ The transmitter uses an external clock applied to the RI# pin.

CKS[7]: Transmitter 1x clock mode selector

logic 0 ⇒ The transmitter is in Nx clock mode as defined in the TCR register. After a hardware reset the transmitter operates in 16x clock mode, i.e. 16C550 compatibility.

logic 1 ⇒ The transmitter is in isochronous 1x clock mode.

7.11.9 Nine-bit Mode Register 'NMR'

The NMR register is located at offset 0x0D of the ICR

The UART offers 9-bit data framing for industrial multi-drop applications. The 9-bit mode is enabled by setting bit 0 of the Nine-bit Mode Register (NMR). In 9-bit mode the data length setting in LCR[1:0] is ignored. Furthermore as parity is permanently disabled, the setting of LCR[5:3] is also ignored.

The receiver stores the 9th bit of the received data in LSR[2] (where parity error is stored in normal mode). Note that the UART provides a 128-deep FIFO for LSR[3:0]. The transmitter FIFO is 9 bits wide and 128 deep. The user should write the 9th (MSB) data bit in SPR[0] first and then write the other 8 bits to THR.

As parity mode is disabled, LSR[7] is set whenever there is an overrun, framing error or received break condition. It is unaffected by the contents of LSR[2] (Now the received 9th data bit).

In 9-bit mode, in-band flow control is disabled regardless of the setting of EFR[3:0] and the XON1/XON2/XOFF1 and XOFF2 registers are used for special character detection.

Interrupts in 9-Bit Mode:

While IER[2] is set, upon receiving a character with status error, a level 1 interrupt is asserted when the character and the associated status are transferred to the FIFO.

The UART can assert an optional interrupt if a received character has its 9th bit set. As multi-drop systems often use the 9th bit as an address bit, the receiver is able to generate an interrupt upon receiving an address character. This feature is enabled by setting NMR[2]. This will result in a level 1 interrupt being asserted when the address character is transferred to the receiver FIFO.

In this case, as long as there are no errors pending, i.e. LSR[1], LSR[3], and LSR[4] are clear, '0' can be read back from LSR[7] and LSR[1], thus differentiating between an 'address' interrupt and receiver error or overrun interrupt in 9-bit mode. Note however that should an overrun or error interrupt actually occur, an address character may also reside in the FIFO. In this case, the software driver should examine the contents of the receiver FIFO as well as process the error.

The above facility produces an interrupt for recognizing any 'address' characters. Alternatively, the user can configure the UART to compare the receiver data stream with up to four programmable 9-bit characters and assert a level 5 interrupt after detecting a match. The interrupt occurs when the character is transferred to the FIFO (See below).

NMR[0]: 9-bit mode enable

logic 0 ⇒ 9-bit mode is disabled.

logic 1 ⇒ 9-bit mode is enabled.

NMR[1]: Enable interrupt when 9th bit is set

logic 0 ⇒ Receiver interrupt for detection of an 'address' character (i.e. 9th bit set) is disabled.

logic 1 ⇒ Receiver interrupt for detection of an 'address' character (i.e. 9th bit set) is enabled and a level 1 interrupt is asserted.

Special Character Detection

While the UART is in both 9-bit mode and Enhanced mode, setting IER[5] will enable detection of up to four 'address' characters. The least significant eight bits of these four programmable characters are stored in special characters 1 to 4 (XON1, XON2, XOFF1 and XOFF2 in 650 mode) registers and the 9th bit of these characters are programmed in NMR[5] to NMR[2] respectively.

NMR[2]: Bit 9 of Special Character 1
NMR[3]: Bit 9 of Special Character 2
NMR[4]: Bit 9 of Special Character 3
NMR[5]: Bit 9 of Special Character 4

NMR[7:6]: Reserved

Bits 6 and 7 of NMR are always cleared and reserved for future use.

7.11.10 Modem Disable Mask 'MDM'

The MDM register is located at offset 0x0E of the ICR

This register is cleared after a hardware reset to maintain compatibility with 16C550. It allows the user to mask interrupts, sleep operation and power management events due to individual modem lines or the serial input line.

MDM[0]: Disable delta CTS

logic 0 ⇒ Delta CTS is enabled. It can generate a level 4 interrupt when enabled by IER[3]. In power-state D2, delta CTS can assert the PME# line. Delta CTS can wake up the UART when it is asleep under auto-sleep operation.

logic 1 ⇒ Delta CTS is disabled. In can not generate an interrupt, assert a PME# or wake up the UART.

MDM[1]: Disable delta DSR

logic 0 ⇒ Delta DSR is enabled. It can generate a level 4 interrupt when enabled by IER[3]. In power-state D2, delta DSR can assert the PME# line. Delta DSR can wake up the UART when it is asleep under auto-sleep operation.

logic 1 ⇒ Delta DSR is disabled. In can not generate an interrupt, assert a PME# or wake up the UART.

MDM[2]: Disable Trailing edge RI

logic 0 ⇒ Trailing edge RI is enabled. It can generate a level 4 interrupt when enabled by IER[3]. In power-state D2, trailing edge RI can assert the PME# line. Trailing edge RI can wake up the UART when it is asleep under auto-sleep operation.

logic 1 ⇒ Trailing edge RI is disabled. In can not generate an interrupt, assert a PME# or wake up the UART.

MDM[3]: Disable delta DCD

logic 0 ⇒ Delta DCD is enabled. It can generate a level 4 interrupt when enabled by IER[3]. In power-state D2, delta DCD can assert the PME# line. Delta DCD can wake up the UART when it is asleep under auto-sleep operation.

logic 1 ⇒ Delta DCD is disabled. In can not generate an interrupt, assert a PME# or wake up the UART.

MDM[4]: Reserved

This bit must be set to '0'

MDM[5]: Disable SIN wake up

logic 0 ⇒ When the device is in power-down state D2, a change in the state of the serial input line (i.e. start bit) can assert the PME# line

logic 1 ⇒ When the device is in power-down state D2, a change in the state of the serial input line cannot assert the PME# line.

MDM[7:6]: Reserved

7.11.11 Readable FCR 'RFC'

The RFC register is located at offset 0x0F of the ICR

This read-only register returns the current state of the FCR register (Note that FCR is write-only). This register is included for diagnostic purposes.

7.11.12 Good-data status register 'GDS'

The GDS register is located at offset 0x10 of the ICR

For the definition of Good-data status refer to section 6.4.7.

GDS[0]: Good Data Status

GDS[7:1]: Reserved

8 LOCAL BUS

8.1 Overview

The OX16PCI954 incorporates a bridge from PCI to the Local Bus. It allows card developers to expand the capabilities of their products by adding peripherals to this bus.

When Mode[1:0] is '00', the Local Bus is comprised of a bi-directional 8-bit data bus, an 8-bit address bus, up to four chip selects, and a number of control signals that allow for easy interfacing to standard peripherals. It also provides twelve active-high or active-low interrupt inputs.

When Mode[1:0] is '11', the Local Bus is comprised of a bi-directional 32-bit data bus, a 12-bit address bus, up to four chip selects, and the same control signals and interrupts as in 8-bit mode. In this mode the Internal UARTs are unused and the UART pins are used to extend the 8-bit Local Bus to 32-bit mode.

The local bus is configured by LT1 and LT2 (see sections 6.4.3 & 6.4.4) in the Local Configuration Register space. By programming these registers the card developer can alter the characteristics of the local bus to suit the characteristics of the peripheral devices being used.

8.2 Operation

The local bus can be accessed via I/O and memory space, in similar fashion to the internal UARTs. The mapping to the devices will vary with the application, but the bus is fully configurable to facilitate simple development.

The operation of the local bus is synchronised to the PCI bus clock. The clock signal is output on pin LBCLK if it has been enabled by setting LT2[30].

The eight bit bi-directional pins LBD[7:0] (LBD[31:0] in 32-bit mode) drive the output data onto the bus during local bus write cycles. For reads, the device latches the data read from these pins at the end of the cycle.

The local bus address is placed on pins LBA[7:0] (LBA[11:0] in 32-bit mode) at the start of each local bus cycle and will remain latched until the start of the subsequent cycle. If the maximum allowable block size (256 bytes) is allocated to the local bus in I/O space, then as access in I/O space is byte aligned, AD[7:0] are asserted on LBA[7:0]. If a smaller address range is selected, the corresponding upper address lines will be set to logic zero.

The control bus is comprised of up to four chip-select signals LBCS[3:0]#, a read strobe LBRD# and a write strobe LBWR#, in Intel-type interfaces. For Motorola-type interfaces, LBWR# is re-defined to perform read/write control signal (LBRDWR#) and the chip-select signals (LBCS[3:0]#) are re-defined to data-strobe (LBDS[3:0]#).

A reference cycle is defined, as two PCI clock cycles after the master asserts the IRDY# signal for the first time within a frame. In general, all the local bus control signals change state in the first cycle after the reference cycle, with offsets to provide suitable setup and hold times for common peripheral devices. However, all the timings can be increased / decreased independently in multiples of PCI clock cycles. This feature enables the card designer to override the length of read or write operations, the address and chip-select set-up and hold timing, and the data bus hold timing so that add-in cards can be configured to suit different speed peripheral devices connected to the Local Bus. The designer can also program the data bus to remain in the high impedance state or actively drive the bus during idle periods.

The local bus will always return to an idle state, where no chip-select (data-strobe in Motorola mode) signal is active, between adjacent accesses. During read cycles the local bus interface latches data from the bus on the rising edge of the clock where LBRD# (LBDS[3:0]# in Motorola mode) goes high. Card designers should ensure that their peripherals provide the OX16PCI954 with the specified data set-up and hold times with respect to this clock edge.

The local bus cannot accept burst transfers from the PCI bus. If a burst transfer is attempted the PCI interface will signal 'disconnect with data' on the first data phase. The local bus does accept 'fast back-to-back' transactions from PCI.

A PCI target must complete the transaction within 16 PCI clock cycles from assertion of the FRAME# signal, otherwise it should signal a retry. During a read operation from the Local Bus, OX16PCI954 waits for master-ready signal (IRDY#) and computes the number of remaining cycles to the de-assertion of the read control signal. If the total number of PCI clock cycles for that frame is greater than 16 clock cycles, OX16PCI954 will post a retry. The master would normally return immediately and complete the operation in the following frame.

8.3 Configuration & Programming

The configuration registers for the local bus controller are described in sections 6.4.3 & 6.4.4. The values of these registers after reset allow the host system to identify the function and configure its base address registers. Alternatively many of the default values can be re-programmed during device initialisation through use of the optional serial EEPROM (see section 10).

The I/O space block can be varied in size from 4 bytes to 256 bytes (32 bytes is the default) by setting LT2[22:20] accordingly. Varying the block size means that I/O space can be allocated efficiently by the system, whatever the application.

The I/O block can then be divided into one, two or four chip-select regions, depending on the setting in LT2[26:23]. To divide the area into four chip-select region, the user should select the second uppermost non-zero address bit as the Lower-Address-CS-decode. To divide into two regions, the user should select the uppermost address bit. If an address bit beyond the selected range is selected, the entire I/O space is allocated to CS0#. For example, if 32 bytes of I/O space are reserved, the active address lines are A[4:0]. To divide this into four regions, the Lower Address CS parameter should be set to A3, by programming the value '0001' into LT2[26:23]. To select two regions, choose A4, and to maintain one region, select any value greater than A4.

In 8-bit mode, the memory space block is always 4K bytes, and always divided into four chip-select regions of 1K byte each.

In 32-bit mode, again the I/O space can be varied in size from 4 bytes to 256 bytes. It is also possible to increase the memory space block size from 4K bytes to 16K bytes. Also in 32-bit mode, the Lower-Address-CS-Decode parameter afftects division of the I/O space AND memory space into chip-select regions.

A soft reset facility is provided so software can independently reset the peripherals on the local bus. The local bus reset signals, LBRST and LBRST#, are always active during a PCI bus reset and also when the configuration register bit LT2[29] is set to 1.

The clock enable bit, when set, enables a copy of the PCI bus clock output on the local bus pin LBCLK. A buffered UART clock can also be asserted on the UART_Clk_Out pin; this means that a single oscillator can be used to drive serial ports on the local bus as well as the internal UARTs.

9 BIDIRECTIONAL PARALLEL PORT

9.1 Operation and Mode selection

The OX16PCI954 offers a compact, low power, IEEE-1284 (EPP-only) compliant host-interface parallel port, designed to interface to many peripherals such as printers, scanners and external drives. It supports compatibility modes, SPP, NIBBLE and PS2, as well as EPP mode. The register set is compatible with the Microsoft® register definition. To enable the parallel port function, the Mode[1:0] pins should be set to '01'. The system can access the parallel port via two 8-byte blocks of I/O space; BAR0 contains the address of the basic parallel port registers, BAR1 contains the address of the upper registers. These are referred to as the 'lower block' and 'upper block' in this section. If the upper block is located at an address 0x400 above the lower block, generic PC device drivers can be used to configure the port, as the addressable registers of legacy parallel ports always have this relationship. If not, a custom driver will be needed.

9.1.1 SPP mode

SPP (output-only) is the standard implementation of a simple parallel port. In this mode, the PD lines always drive the value in the PDR register. All transfers are done under software control. Input must be performed in nibble mode.

Generic device driver-software may use the address in I/O space encoded in BAR0 of function 1 to access the parallel port. The default configuration allocates 8 bytes to BAR0 in I/O space.

9.1.2 PS2 mode

This mode is also referred to as bi-directional or compatible parallel port. In this mode, directional control of the PD lines is possible by setting & clearing DCR[5]. Otherwise operation is similar to SPP mode.

9.1.3 EPP mode

To use the Enhanced Parallel Port 'EPP' the mode bits (ECR[7:5]) must be set to '100'. The EPP address and data port registers are compatible with the IEEE 1284 definition. A write or read to one of the EPP port registers is passed through the parallel port to access the external peripheral. In EPP mode, the STB#, INIT#, AFD# AND SLIN# pins change from open-drain outputs to active push-pull (totem pole) drivers (as required by IEEE 1284) and the pins ACK#, AFD#, BUSY, SLIN# and STB# are redefined as INTR#, DATASTB#, WAIT#, ADDRSTB# and WRITE# respectively.

An EPP port access begins with the host reading or writing to one of the EPP port rgisters. The device automatically buffers the data between the I/O registers and the parallel port depending on whether it is a read or a write cycle. When the peripheral is ready to complete the transfer it takes the WAIT# status line high. This allows the host to complete the EPP cycle.

If a faulty or disconnected peripheral failed to respond to an EPP cycle the host would never see a rising edge on WAIT#, and subsequently lock up. A built-in time-out facility is provided in order to prevent this from happening. It uses an internal timer which aborts the EPP cycle and sets a flag in the PSR register to indicate the condition. When the parallel port is not in EPP mode the timer is switched off to reduce current consumption. The host time-out period is 10µs as specified with the IEEE-1284 specification.

The register set is compatible with the Microsoft® register definition. Assuming that the upper block is located 400h above the lower block, the registers are found at offset 000-007h and 400-402h.

9.1.4 ECP mode (not supported)

The Extended Capabilities Port 'ECP' mode is not supported.

9.2 Parallel port interrupt

The parallel port interrupt is asserted on INTB# (or INTA# if specified with the serial EEPROM). It is enabled by setting DCR[4]. When DCR[4] is set, an interrupt is asserted on the rising edge of the ACK# (INTR#) pin and held until the status register is read, which resets the INT# status bit (DSR[2]).

9.3 Register Description

The parallel port registers are described below. (NB it is assumed that the upper block is placed 400h above the lower block).

Register Name	Address Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPP (Compatibility Mode) Registers										
PDR	000h	R/W	Parallel Port Data Register							
DSR (EPP mode)	001h	R	nBUSY	ACK#	PE	SLCT	ERR#	INT#	1	Timeout
(Other modes)	001h	R	nBUSY	ACK#	PE	SLCT	ERR#	INT#	1	1
DCR	002h	R/W	0	0	DIR	INT_EN	nSLIN#	INIT#	nAFD#	nSTB#
EPPA [1]	003h	R/W	EPP Address Register							
EPPD1 [1]	004h	R/W	EPP Data 1 Register							
EPPD2 [1]	005h	R/W	EPP Data 2 Register							
EPPD3 [1]	006h	R/W	EPP Data 3 Register							
EPPD4 [1]	007h	R/W	EPP Data 4 Register							
-	400h	-	Reserved							
-	401h	-	Reserved							
ECR	402h	R/W	Mode[2:0]			Reserved – Must write '00001'				
-	403h	-	Reserved							

Table 30: Parallel port register set

Note 1 : These registers are only available in EPP mode.
Note 2 : Prefix 'n' denotes that a signal is inverted at the connector. Suffix '#' denotes active-low signalling

The reset state of PDR, EPPA and EPPD1-4 is not determinable (i.e. 0xXX). The reset value of DSR is 'XXXXX111'. DCR and ECR are reset to '0000XXXX' and '00000001' respectively.

9.3.1 Parallel port data register 'PDR'

PDR is located at offset 000h in the lower block. It is the standard parallel port data register. Writing to this register in mode 000 will drive data onto the parallel port data lines. In all other modes the drivers may be tri-stated by setting the direction bit in the DCR. Reads from this register return the value on the data lines.

9.3.2 Device status register 'DSR'

DSR is located at offset 001h in the lower block. It is a read only register showing the current state of control signals from the peripheral. Additionally in EPP mode, bit 0 is set to '1' when an operation times out (see section 9.1.3)

DSR[0]:
EPP mode: Timeout
logic 0 ⇒Timeout has not occurred.
logic 1 ⇒Timeout has occurred (Reading this bit clears it).

Other modes: Unused
This bit is permanently set to 1.

DSR[1]: Unused
This bit is permanently set to 1.

DSR[2]: INT#
logic 0 ⇒ A parallel port interrupt is pending.
logic 1 ⇒ No parallel port interrupt is pending.

This bit is activated (set low) on a rising edge of the ACK# pin. It is de-activated (set high) after reading the DSR.

DSR[3]: ERR#
logic 0 ⇒ The ERR# input is low.
logic 1 ⇒ The ERR# input is high.

DSR[4]: SLCT
logic 0 ⇒ The SLCT input is low.
logic 1 ⇒ The SLCT input is high.

DSR[5]: PE
logic 0 ⇒The PE input is low.
logic 1 ⇒The PE input is high.

DSR[6]: ACK#
logic 0 ⇒ The ACK# input is low.
logic 1 ⇒ The ACK# input is high.

DSR[7]: nBUSY
logic 0 ⇒ The BUSY input is high.
logic 1 ⇒ The BUSY input is low.

9.3.3 Device control register 'DCR'

DCR is located at offset 002h in the lower block. It is a read-write register which controls the state of the peripheral inputs and enables the peripheral interrupt. When reading this register, bits 0 to 3 reflect the actual state of STB#, AFD#, INIT# and SLIN# pins respectively. When in EPP mode, the WRITE#, DATASTB# AND ADDRSTB# pins are driven by the EPP controller, although writes to this register will override the state of the respective lines.

DCR[0]: nSTB#
logic 0 ⇒ Set STB# output to high (inactive).
logic 1 ⇒ Set STB# output to low (active).

During an EPP address or data cycle the WRITE# pin is driven by the EPP controller, otherwise it is inactive.

DCR[1]: nAFD#
logic 0 ⇒ Set AFD# output to high (inactive).
logic 1 ⇒ Set AFD# output to low (active).

During an EPP address or data cycle the DATASTB# pin is driven by the EPP controller, otherwise it is inactive.

DCR[2]: INIT#
logic 0 ⇒ Set INIT# output to low (active).
logic 1 ⇒ Set INIT# output to high (inactive).

DCR[3]: nSLIN#
logic 0 ⇒ Set SLIN# output to high (inactive).
logic 1 ⇒ Set SLIN# output to low (active).

During an EPP address or data cycle the ADDRSTB# pin is driven by the EPP controller, otherwise it is inactive.

DCR[4]: ACK Interrupt Enable
logic 0 ⇒ ACK interrupt is disabled.
logic 1 ⇒ ACK interrupt is enabled.

DCR[5]: DIR
logic 0 ⇒ PD port is output.
logic 1 ⇒ PD port is input.

This bit is overridden during an EPP address or data cycle, when the direction of the port is controlled by the bus access (read/write)

DCR[7:6]: Reserved
These bits are reserved and always set to "00".

9.3.4 EPP address register 'EPPA'

EPPA is located at offset 003h in lower block, and is only used in EPP mode. A byte written to this register will be transferred to the peripheral as an EPP address by the hardware. A read from this register will transfer an address from the peripheral under hardware control.

9.3.5 EPP data registers 'EPPD1-4'

The EPPD registers are located at offset 004h-007h of the lower block, and are only used in EPP mode. Data written or read from these registers is transferred to/from the peripheral under hardware control.

9.3.6 Extended control register 'ECR'

The Extended control register is located at offset 002h in upper block. It is used to configure the operation of the parallel port.

ECR[4:0]: Reserved
These bits are reserved and must always be set to "00001".

ECR[7:5]: Mode
These bits define the operational mode of the parallel port.

logic '000'	SPP
logic '001'	PS2
logic '010'	Reserved
logic '011'	Reserved
logic '100'	EPP
logic '101'	Reserved
logic '110'	Reserved
logic '111'	Reserved

10 SERIAL EEPROM

10.1 Specification

The OX16PCI954 can be configured using an optional serial electrically-erasable programmable read only memory (EEPROM). If the EEPROM is not present, the device will remain in its default configuration after reset. Although this may be adequate for some applications, many will benefit from the degree of programmability afforded by this feature.

The EEPROM interface is based on the 93C46/56 serial EEPROM devices which have a proprietary serial interface known as Microwire™. The interface has four pins which supply the memory device with a clock, a chip-select, and serial data input and output lines. In order to read from such a device, a controller has to output serially a read command and address, then input serially the data. The 93C46/56 and compatible devices have a 16-bit data word format but differ in memory size (and number of address bits).

The OX16PCI954 incorporates a controller module which reads data from the serial EEPROM and writes data into the configuration register space. It performs this operation in a sequence which starts immediately after a PCI bus reset and ends either when the controller finds no EEPROM is present or when it reaches the end of its data. The operation of this controller is described below. Following device configuration, driver software can access the serial EEPROM through four bits in the device-specific Local Configuration Register LCC[27:24]. Software can use this register to manipulate the device pins in order to read and modify the EEPROM contents.

The OX16PCI954 requires a total of 82 bytes of EEPROM data to program all the EEPROM writable registers. Note that 93C46 and 93C56 EEPROM devices offer 128 and 256 bytes of programmable data respectively.

A Windows® based utility to program the EEPROM is available. For further details please contact Oxford Semiconductor (see back cover).

Microwire™ is a trade mark of National Semiconductor. For a description of MicroWire, please refer to National Semiconductor data manuals.

10.2 EEPROM Data Organisation

The serial EEPROM data is divided in four zones. The size of each zone is an exact multiple of 16-bit WORDs. Zone0 is allocated to the header. A valid EEPROM program must contain a header. The EEPROM can be programmed from the PCI bus. Once the programming is complete, the device driver should either reset the PCI bus or set LCC[29] to reload the OX16PCI954 registers from the serial EEPROM. The general EEPROM data structure is shown in Table 31.

DATA Zone	Size (Words)	Description
0	One	Header
1	One or more	Local Configuration Registers
2	One to four	Identification Registers
3	Two or more	PCI Configuration Registers

Table 31: EEPROM data format

10.2.1 Zone0: Header

The header identifies the EEPROM program as valid.

Bits	Description
15:4	These bits should return 0x950 to identify a valid program. Once the OX16PCI954 reads 0x950 from these bits, it sets LCC[28] to indicate that a valid EEPROM program is present.
3	Reserved. Write '0' to this bit.
2	1 = Zone1 (Local Configuration) exists 0 = Zone1 does not exist
1	1 = Zone2 (Identification) exists 0 = Zone2 does not exist
0	1 = Zone3 (PCI Configuration) exists 0 = Zone3 does not exist

The programming data for each zone follows the proceeding zone if it exists. For example a Header value of 0x9507 indicates that all zones exist and they follow one another in sequence, while 0x9505 indicates that only Zones 1 and 3 exist where the header data is followed by Zone1 WORDs, and since Zone2 is missing Zone1 WORDs are followed by Zone3 WORDs.

10.2.2 Zone1: Local Configuration Registers

The Zone1 region of EEPROM contains the program value of the vendor-specific Local Configuration Registers using one or more configuration WORDs. Registers are selected using a 7-bit byte-offset field. This offset value is the offset from Base Address Registers in I/O or memory space (see section 6.4).

Note: Not all of the registers in the Local Configuration Register set are writable by EEPROM. If bit2 of the header is set, Zone1 configuration WORDs follow the header declaration. The format of configuration WORDs for the Local Configuration Registers in Zone1 are described in Table 32.

Bits	Description
15	'0' = There are no more Configuration WORDs to follow in Zone1. Move to the next available zone or end EEPROM program if no more zones are enabled in the Header. '1' = There is another Configuration WORD to follow for the Local Configuration Registers.
14:8	These seven bits define the byte-offset of the Local configuration register to be programmed. For example the byte-offset for LT2[23:16] is 0x0E.
7:0	8-bit value of the register to be programmed

Table 32: Zone 1 data format

Table 33 shows which Local Configuration registers are writable from the EEPROM. Note that an attempt by the EEPROM to write to any other offset locations can result in unpredictable behaviour.

Offset	Bits	Description	Reference
0x00	1:0	Must be '00'.	
0x00	2	Enable UART clock-out.	LCC[2]
0x00	4:3	Endian byte-lane select.	LCC[4:3]
0x00	6:5	Power-down filter.	LCC[6:5]
0x00	7	MIO2_PME enable.	LCC[7]
0x04	7:0	Multi-purpose IO configuration.	MIC[7:0]
0x05	7:0	Multi-purpose IO configuration.	MIC[15:8]
0x06	7:0	Multi-purpose IO configuration.	MIC[23:16]
0x08	7:0	Local Bus timing parameters	LT1[7:0]
0x09	7:0	Local Bus timing parameters	LT1[15:8]
0x0A	7:0	Local Bus timing parameters	LT1[23:16]
0x0B	7:0	Local Bus timing parameters	LT1[31:24]
0x0C	7:0	Local Bus timing parameters	LT2[7:0]
0x0D	7:0	Local Bus timing parameters	LT2[15:8]
0x0E	3:0	Must be '0000'.	
0x0E	6:4	IO Space Block size.	LT2[22:20]
0x0E	7	Lower-Address-CS-Decode.	LT2[23]
0x0F	2:0	Lower-Address-CS-Decode.	LT2[26:24]
0x0F	4:3	Memory space block size in 32-bit Local Bus.	LT2[28:27]
0x0F	5	Must be '0'.	
0x0F	6	Local Bus clock enable.	LT2[30]
0x0F	7	Bus interface type.	LT2[31]
0x1E	3:0	UART Interrupt Mask	GIS[19:16]
0x1E	4	MIO0/Parallel Port interrupt mask	GIS[20]
0x1E	7:5	Multi-purpose IO interrupt mask.	GIS[23:21]
0x1F	7:0	Multi-purpose IO interrupt mask.	GIS[31:24]

Table 33: EEPROM-writable Local Configuration Registers

10.2.3 Zone2: Identification Registers

The Zone2 region of EEPROM contains the program value for Vendor ID and Subsystem Vendor ID. The format of Device Identification configuration WORDs are described in Table 34.

Bits	Description
15	'0' = There are no more Zone2 (Identification) bytes to program. Move to the next available zone or end EEPROM program if no more zones are enabled in the Header. '1' = There is another Zone2 (Identification) byte to follow.
14:8	0x00 = Vendor ID bits [7:0]. 0x01 = Vendor ID bits [15:8]. 0x02 = Subsystem Vendor ID [7:0]. 0x03 = Subsystem Vendor ID [15:8]. 0x03 to 0x7F = Reserved.
7:0	8-bit value of the register to be programmed

Table 34: Zone 2 data format

10.2.4 Zone3: PCI Configuration Registers

The Zone3 region of EEPROM contains any changes required to the PCI Configuration registers (with the exception of Vendor ID and Subsystem Vendor ID which are programmed in Zone2). This zone is divided into two groups, each of which consists of a function header WORD, and one or more configuration WORDs for that function. The function header is described in Table 35.

Bits	Description
15	'0' = End of Zone 3. '1' = Define this function header.
14:3	Reserved. Write zeros.
2:0	Function number for the following configuration WORD(s). '000' = Function0 (Internal UARTs) '001' = Function1 (Local Bus / Parallel Port) Other values = Reserved.

Table 35: Zone 3 data format (Function Header)

The subsequent WORDs for each function contain the address offset and a byte of programming data for the PCI Configuration Space belonging to the function number selected by the proceeding Function-Header. The format of configuration WORDs for the PCI Configuration Registers are described below.

Bits	Description
15	'0' = This is the last configuration WORD in for the selected function in the Function-Header. '1' = There is another WORD to follow for this function.
14:8	These seven bits define the byte-offset of the PCI configuration register to be programmed. For example the byte-offset of the Interrupt Pin register is 0x3D. Offset values are tabulated in section 6.2.
7:0	8-bit value of the register to be programmed

Table 36: Zone 3 data format (data)

Table 37 shows which PCI Configuration registers are writable from the EEPROM for each function.

Offset	Bits	Description
0x02	7:0	Device ID bits 7 to 0.
0x03	7:0	Device ID bits 15 to 8.
0x06	3:0	Must be '0000'.
0x06	4	Extended Capabilities.
0x06	7:5	Must be '000'.
0x09	7:0	Class Code bits 7 to 0.
0x0A	7:0	Class Code bits 15 to 8.
0x0B	7:0	Class Code bits 23 to 16.
0x2E	7:0	Subsystem ID bits 7 to 0.
0x2F	7:0	Subsystem ID bits 15 to 8.
0x3D	7:0	Interrupt pin.
0x42	7:0	Power Management Capabilities bits 7 to 0.
0x43	7:0	Power Management Capabilities bits 15 to 8.

Table 37: EEPROM-writable PCI configuration registers

11 OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply voltage	-0.3	7.0	V
V_{IN}	DC input voltage	-0.3	V_{DD} + 0.3	V
I_{IN}	DC input current		+/- 10	mA
T_{STG}	Storage temperature	-40	125	°C

Table 38: Absolute maximum ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply voltage	4.5	5.5	V
T_C	Temperature	0	70	°C

Table 39: Recommended operating conditions

12 DC ELECTRICAL CHARACTERISTICS

12.1 Non-PCI I/O Buffers

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply voltage	Commercial	4.75	5.25	V
V_{IH}	Input high voltage	TTL Interface [1] TTL Schmitt trig	2.0 2.0		V
V_{IL}	Input low voltage	TTL Interface [1] TTL Schmitt trig		0.8 0.8	V
C_{IL}	Cap of input buffers			5.0	pF
C_{OL}	Cap of output buffers			10.0	pF
I_{IH}	Input high leakage current	$V_{in} = V_{DD}$	-10	10	µA
I_{IL}	Input low leakage current	$V_{in} = V_{SS}$	-10	10	µA
V_{OH}	Output high voltage	I_{OH} = 1 µA	V_{DD} – 0.05		V
V_{OH}	Output high voltage	I_{OH} = 4 mA [2]	2.4		V
V_{OL}	Output low voltage	I_{OL} = 1 µA		0.05	V
V_{OL}	Output low voltage	I_{OL} = 4 mA [2]		0.4	V
I_{OZ}	3-state output leakage current		-10	10	µA

Symbol	Parameter	Condition	Typical	Max	Units
I_{CC}	Operating supply current in normal mode	XTAL = 2 MHz	35	48.1	mA
		XTAL = 15 MHz	40	68.7	
		XTAL = 60 MHz	55	116.6	
	Operating supply current in Power-down mode	XTAL = 2 MHz	2	34.4	
		XTAL = 15 MHz	2	39.0	
		XTAL = 60 MHz	2	49.6	

Table 40: Characteristics of non-PCI I/O buffers

Note 1: All input buffers are TTL with the exception of PCI buffers
Note 2: I_{OH} and I_{OL} are 12 mA for PD/LBDB[7:0] and other Parallel Port Outputs. They are 4 mA for all other non-PCI outputs

12.2 PCI I/O Buffers

Symbol	Parameter	Condition	Min	Max	Unit
DC Specifications					
V_{CC}	Supply voltage		4.75	5.25	V
V_{IL}	Input low voltage		-0.5	0.8	V
V_{IH}	Input high voltage		2.0	V_{CC} + 0.5	V
I_{IL}	Input low leakage current	V_{IN} = 0.5V		-70	µA
I_{IH}	Input high leakage current	V_{IN} = 2.7V		70	µA
V_{OL}	Output low voltage	I_{OUT} = -2 mA		0.55	V
V_{OH}	Output low voltage	I_{OUT} = 3 mA, 6mA	2.4		V
C_{IN}	Input pin capacitance			10	pF
C_{CLK}	CLK pin capacitance		5	12	pF
C_{IDSEL}	IDSEL pin capacitance			8	pF
L_{PIN}	Pin inductance			10	nH
AC Specifications					
	Switching current	0 < V_{OUT} 1.4	-44		
$I_{OH(AC)}$	high	1.4 < V_{OUT} 2.4	-44 (V_{OUT} - 1.4)/0.024		mA
		3.1 < V_{OUT} V_{CC}		Eq. A	
	(Test point)	V_{OUT} = 3.1		-142	
	Switching current	V_{OUT} 2.2	95		
$I_{OL(AC)}$	low	2.2 > V_{OUT} > 0.55	V_{OUT} / 0.023		mA
		0.71 > V_{OUT} > 0		Eq. B	
	(Test point)	V_{OUT} = 0.71		206	
I_{CL}	Low clamp current	-5 < V_{IN} < -1	-25 + (V_{IN} +1)/ 0.015		mA
I_{HL}	High clamp current	V_{CC}+4 < V_{IN} < V_{CC}+1	25+ (V_{IN} -V_{CC} -1)/ 0.015		mA
$Slew_R$	Output rise slew rate	0.4V to 2.4V	1	5	V/nS
$Slew_F$	Output fall slew rate	2.4V to 0.4V	1	5	V/nS

Table 41: Characteristics of PCI I/O buffers

Eq. A : I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45) for 3.1 < V_{OUT} V_{CC}

Eq. B : I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT}) for 0.71 > V_{OUT} > 0

13 AC ELECTRICAL CHARACTERISTICS

13.1 PCI Bus

The timings for PCI pins comply with PCI Specification for the 5.0 Volt signalling environment.

13.2 Local Bus

By default, the Local bus control signals change state in the cycle immediately following the reference cycle, with offsets to provide setup and hold times for common peripherals in Intel mode. The tables below show these default values; however each of these can be increased or decreased by an number of PCI clock cycles by adjusting the parameters in registers LT1 and LT2.

Symbol	Parameter	Min	Max	Units
t_{ref}	IRDY# falling to reference LBCLK	Nominally 2 PCI clock cycles		
t_{za}	Reference LBCLK to Address Valid	TBD	TBD	ns
t_{ard}	Address Valid to LBRD# falling	TBD	TBD	ns
t_{zrcs1}	Reference LBCLK to LBCS# falling	TBD	TBD	ns
t_{zrcs2}	Reference LBCLK to LBCS# rising	TBD	TBD	ns
t_{csrd}	LBCS# falling to LBRD# falling	TBD	TBD	ns
t_{rdcs}	LBRD# rising to LBCS# rising	TBD	TBD	ns
t_{zrd1}	Reference LBCLK to LBRD# falling	TBD	TBD	ns
t_{zrd2}	Reference LBCLK to LBRD# rising	TBD	TBD	ns
t_{drd}	Data bus floating to LBRD# falling	TBD	TBD	ns
t_{zd1}	Reference LBCLK to data bus floating at the start of the read transaction	TBD	TBD	ns
t_{zd2}	Reference LBCLK to data bus driven by OX16PCI954 at the end of the read transaction	TBD	TBD	ns
t_{sd}	Data bus valid to LBRD# rising	TBD	TBD	ns
t_{hd}	Data bus valid after LBRD# rising	TBD	TBD	ns

Table 42: Read operation from Intel-type Local Bus

Symbol	Parameter	Min	Max	Units
t_{ref}	IRDY# falling to reference LBCLK	Nominally 2 PCI clock cycles		
t_{za}	Reference LBCLK to Address Valid	TBD	TBD	ns
t_{awr}	Address Valid to LBWR# falling	TBD	TBD	ns
t_{zwcs1}	Reference LBCLK to LBCS# falling	TBD	TBD	ns
t_{zwcs2}	Reference LBCLK to LBCS# rising	TBD	TBD	ns
t_{cswr}	LBCS# falling to LBWR# falling	TBD	TBD	ns
t_{wrcs}	LBWR# rising to LBCS# rising	TBD	TBD	ns
t_{zwr1}	Reference LBCLK to LBWR# falling	TBD	TBD	ns
t_{zwr2}	Reference LBCLK to LBWR# rising	TBD	TBD	ns
t_{zdv}	Reference LBCLK to data bus valid	TBD	TBD	ns
t_{zdf}	Reference LBCLK to data bus high-impedance	TBD	TBD	ns
t_{wrdi}	LBWR# rising to data bus invalid	TBD	TBD	ns

Table 43: Write operation to Intel-type Local Bus

Symbol	Parameter	Min	Max	Units
t_{ref}	IRDY# falling to reference LBCLK	Nominally 2 PCI clock cycles		
t_{za}	Reference LBCLK to Address Valid	TBD	TBD	ns
t_{ads}	Address Valid to LBDS# falling	TBD	TBD	ns
t_{zrds1}	Reference LBCLK to LBDS# falling	TBD	TBD	ns
t_{zrds2}	Reference LBCLK to LBDS# rising	TBD	TBD	ns
vt_{drd}	Data bus floating to LBDS# falling	TBD	TBD	ns
t_{zd1}	Reference LBCLK to data bus floating at the start of the read transaction	TBD	TBD	ns
t_{zd2}	Reference LBCLK to data bus driven by OX16PCI954 at the end of the read transaction	TBD	TBD	ns
t_{sd}	Data bus valid to LBDS# rising	TBD	TBD	ns
t_{hd}	Data bus valid after LBDS# rising	TBD	TBD	ns

Table 44: Read operation from Motorola-type Local Bus

Symbol	Parameter	Min	Max	Units
t_{ref}	IRDY# falling to reference LBCLK	Nominally 2 PCI clock cycles		
t_{za}	Reference LBCLK to Address Valid	TBD	TBD	ns
t_{ads}	Address Valid to LBDS# falling	TBD	TBD	ns
t_{zw1}	Reference LBCLK to LBRDWR# falling	TBD	TBD	ns
t_{zw2}	Reference LBCLK to LBRDWR# rising	TBD	TBD	ns
t_{wds}	LBRDWR# falling to LBDS# falling	TBD	TBD	ns
t_{dsw}	LBDS# rising to LBRDWR# rising	TBD	TBD	ns
t_{zwds1}	Reference LBCLK to LBDS# falling	TBD	TBD	ns
t_{zwds2}	Reference LBCLK to LBDS# rising	TBD	TBD	ns
t_{zdv}	Reference LBCLK to data bus valid	TBD	TBD	ns
t_{zdf}	Reference LBCLK to data bus high-impedance	TBD	TBD	ns
t_{dsdi}	LBDS# rising to data bus invalid	TBD	TBD	ns

Table 45: Write operation to Motorola-type Local Bus

13.3 Serial ports

Isochronous (x1 Clock) Timing:

Symbol	Parameter	Min	Max	Units
t_{irs}	SIN set-up time to Isochronous input clock 'Rx_Clk_In rising [1]	TBD	TBD	ns
t_{irh}	SIN hold time after Isochronous input clock 'Rx_Clk_In' rising [1]	TBD	TBD	ns
t_{its}	SOUT valid after Isochronous output clock 'Tx_Clk_Out' falling [1]	TBD	TBD	ns

Table 46: Isochronous mode timing

Note 1: In Isochronous mode, transmitter data is available after the falling edge of the x1 clock and the receiver data is sampled using the rising edge of the x1 clock. The system designer is should ensure that mark-to-space ratio of the x1 clock is such that the required set-up and hold timing constraint are met. One way of achieving this is to choose a crystal frequency which is twice the required data rate and then divide the clock by two using the on-board prescaler. In this case the mark-to-space ratio is 50/50 for the purpose of set-up and hold calculations.

14 TIMING WAVEFORMS

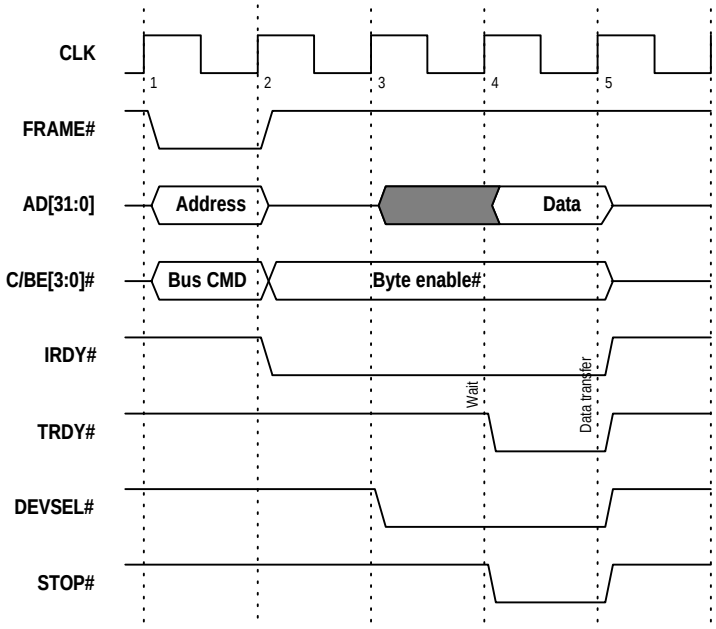


Figure 4: PCI Read Transaction from internal UARTs

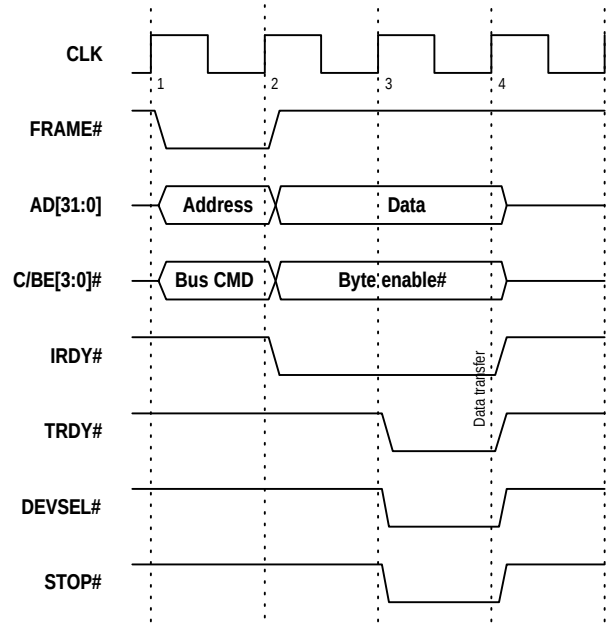


Figure 5: PCI Write Transaction to internal UARTs

TIMING WAVEFORMS

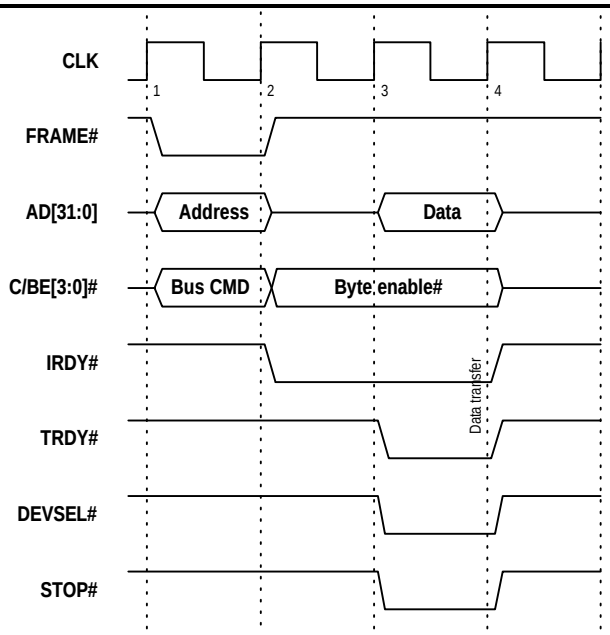


Figure 6: PCI Read transaction from Local Configuration registers

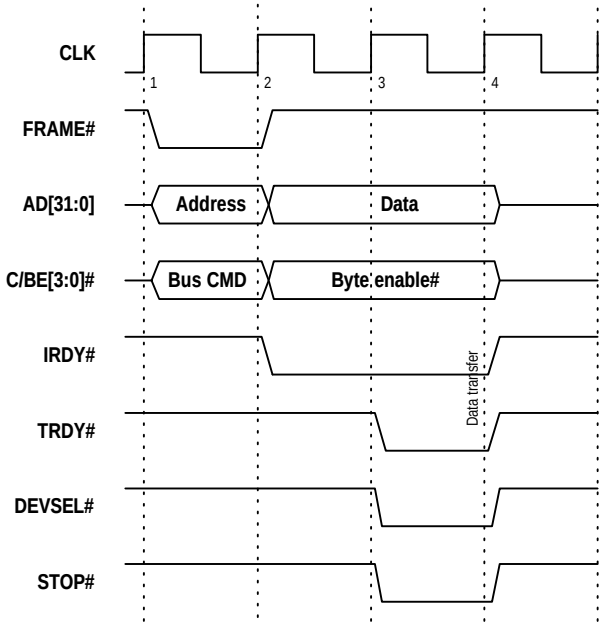


Figure 7: PCI Write transaction to Local Configuration Registers

TIMING WAVEFORMS

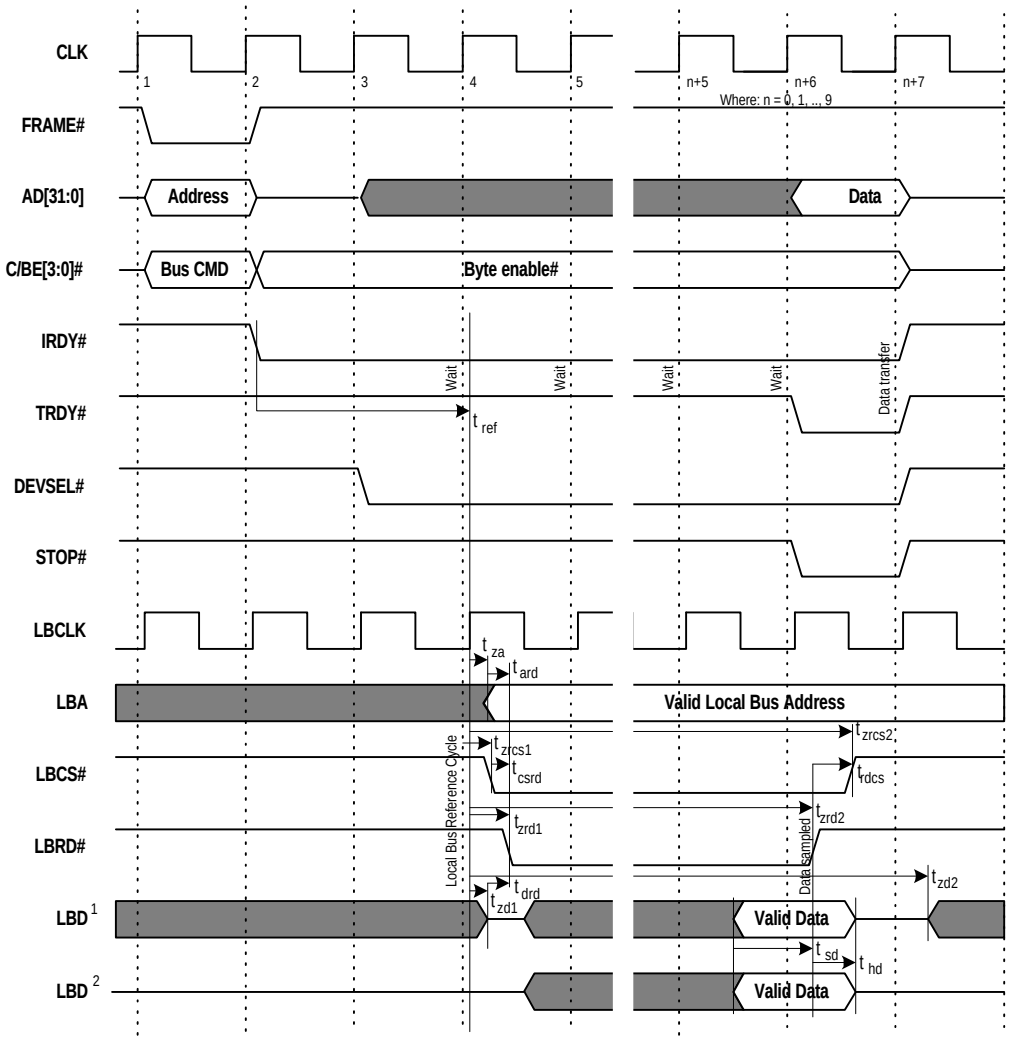


Figure 8: PCI Read Transaction from Intel-type Local Bus

TIMING WAVEFORMS

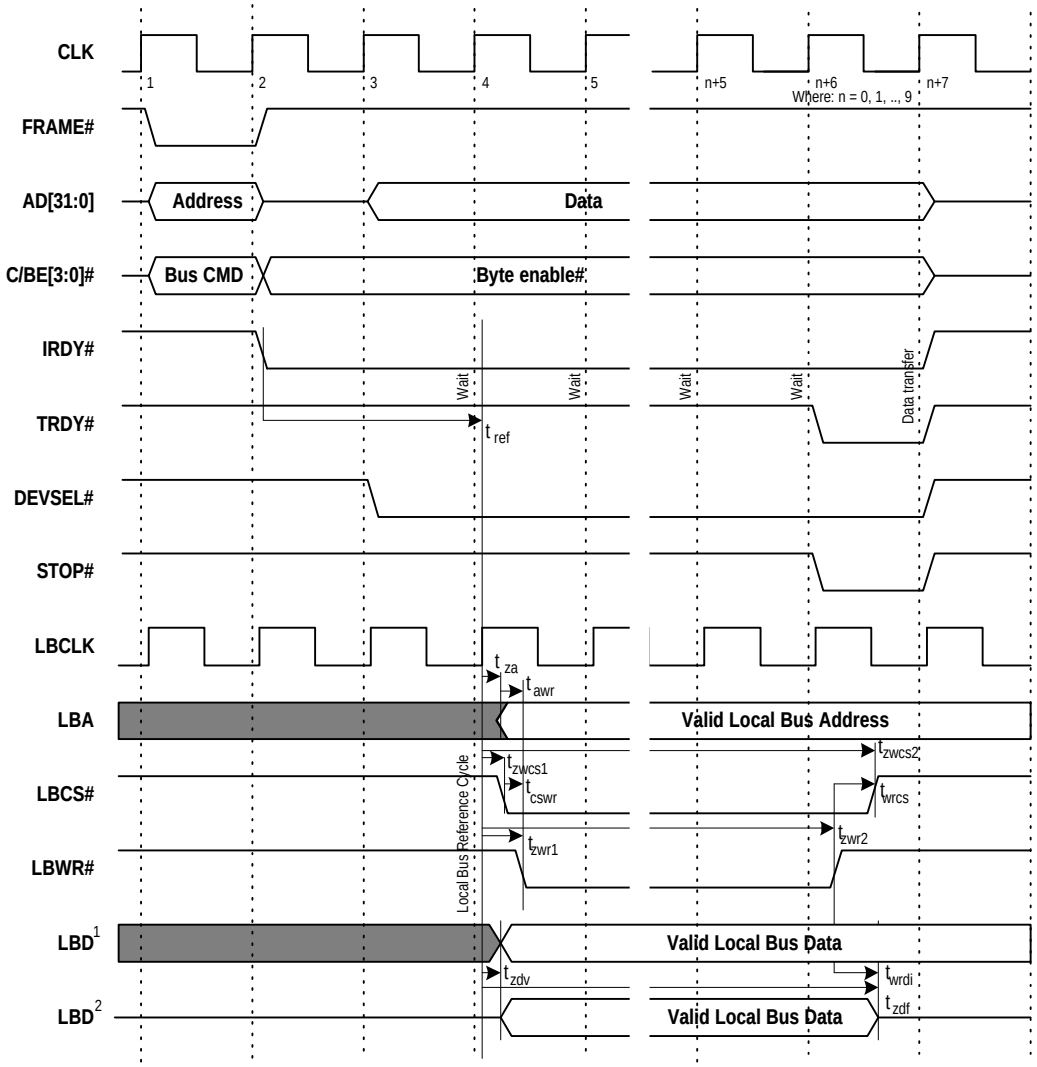


Figure 9: PCI Write Transaction to Intel-type Local Bus

TIMING WAVEFORMS

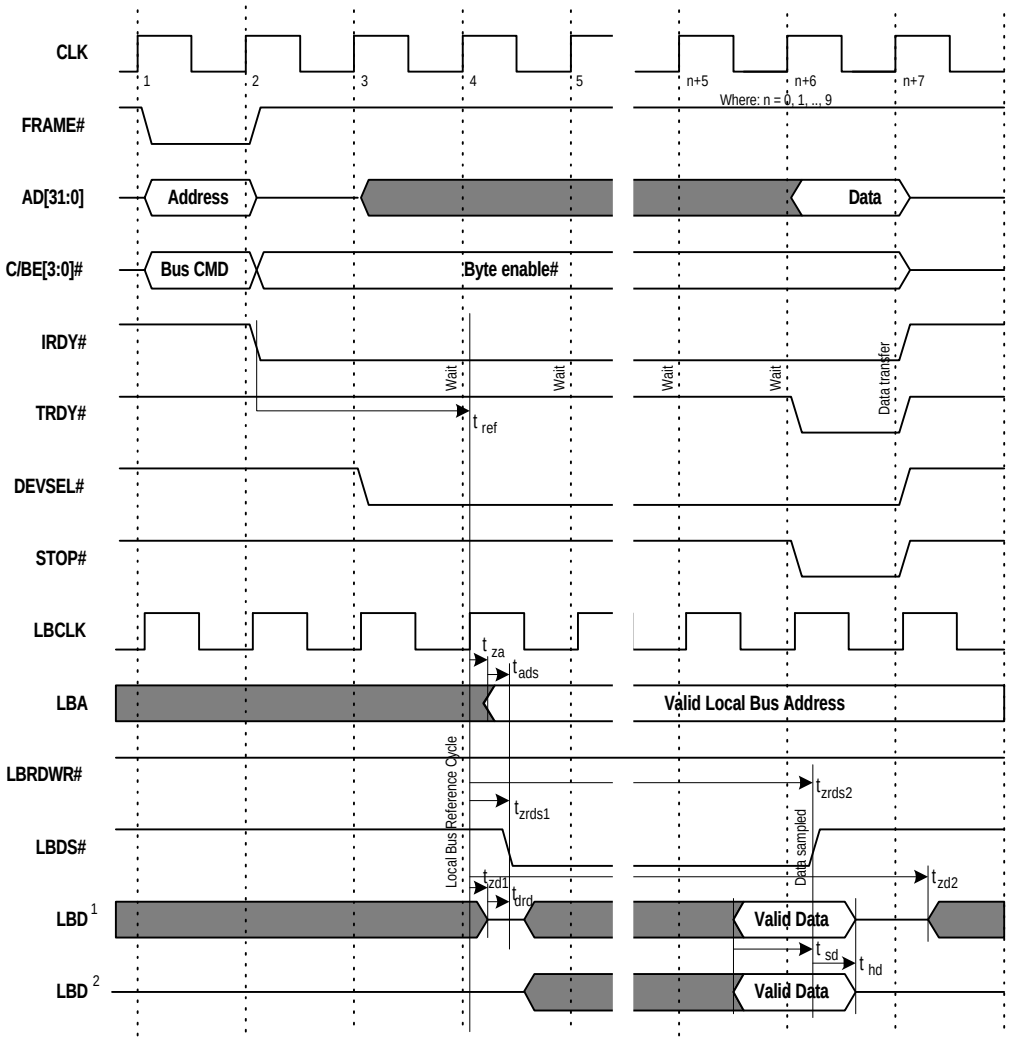


Figure 10: PCI Read Transaction from Motorola-type Local Bus

TIMING WAVEFORMS

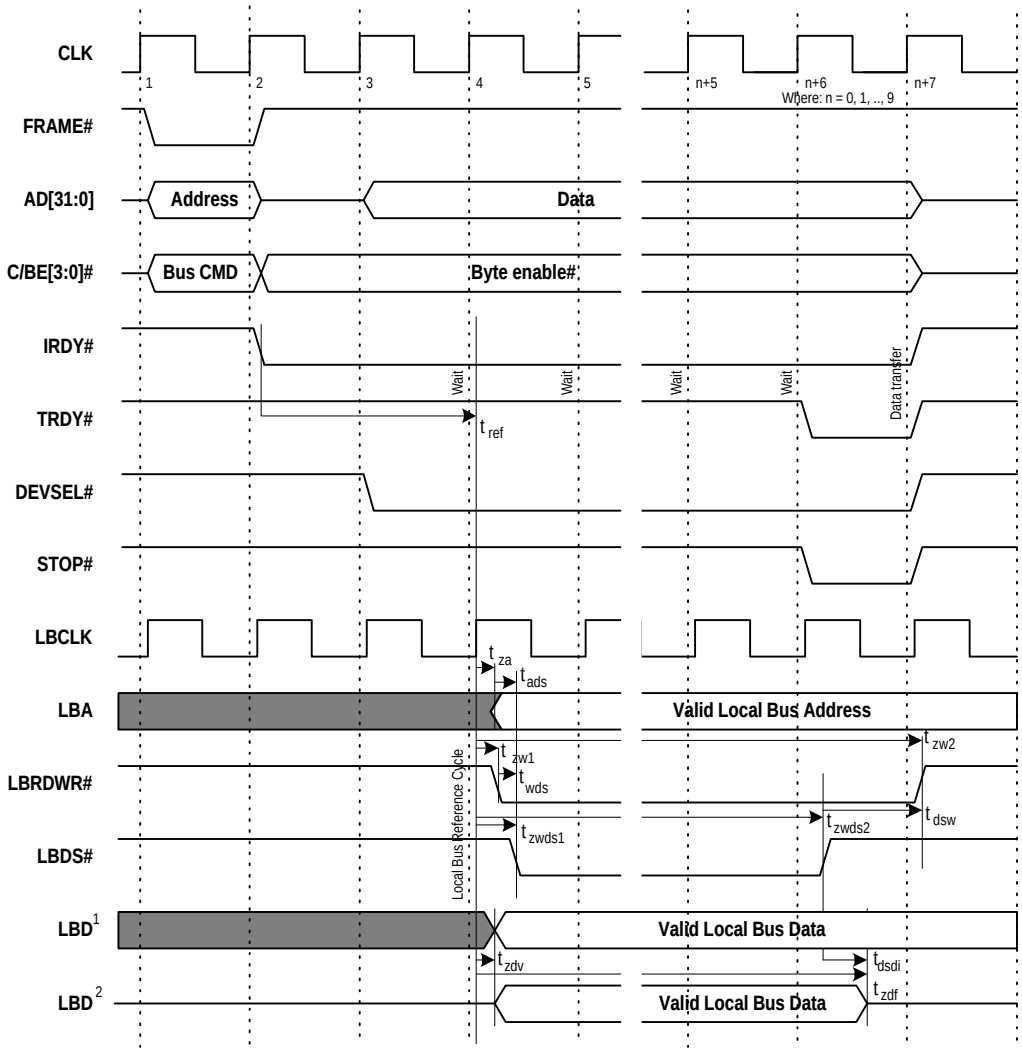


Figure 11: PCI Write Transaction to Motorola-type Local Bus

TIMING WAVEFORMS

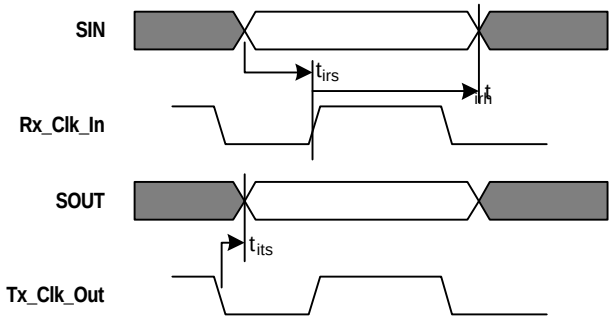


Figure 12: Isochronous (x1 clock) timing waveform

15 PACKAGE INFORMATION

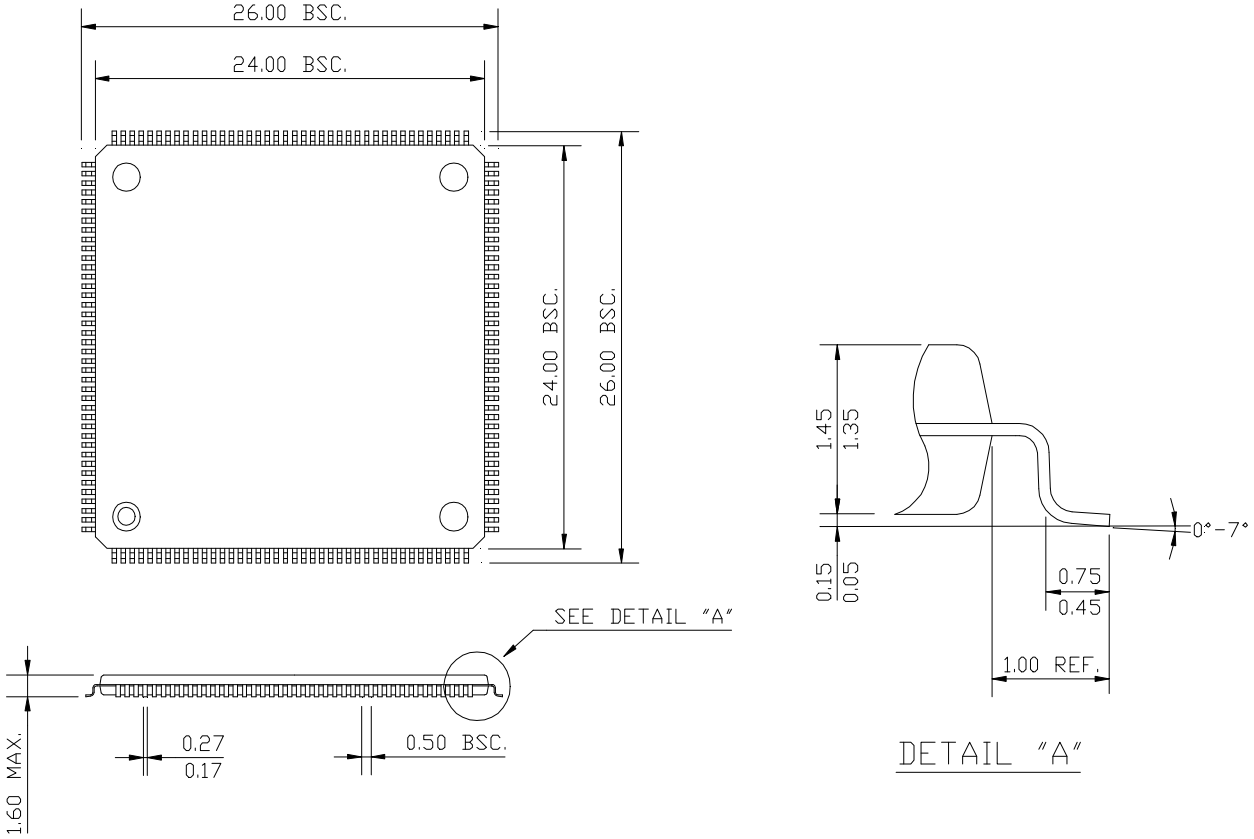


Figure 13: 160 pin Thin Quad Flat Pack (TQFP) package

16 ORDERING INFORMATION

OX16PCI954-TQC60-A

Revision

Package Type – 160 TQFP

NOTES

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