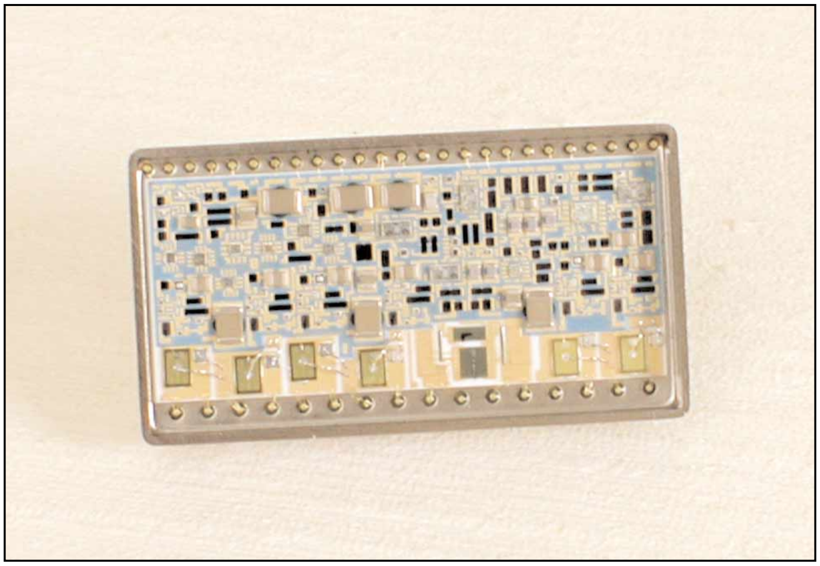
## PW-82520R

# RADIATION TOLERANT 3-PHASE DC MOTOR TORQUE CONTROLLER



## DESCRIPTION

The PW-82520R (100Vdc) is a high performance, radiation tolerant, current regulating torque loop controller designed to accurately regulate the current in the motor windings of 3-phase brushless DC and brush DC motors.

The PW-82520R is a completely self-contained motor controller that converts an analog input command signal into motor current and uses the signals from Hall-effect sensors in the motor to commutate the current in the motor windings. The motor current is internally sensed and processed into an analog signal. The current signal is summed together with the command signal to produce an error signal that controls the pulse width modulation (PWM) duty cycle of the output, thus controlling the motor current. The PW-82520R performance can be tuned by utilizing the internal error amplifier and the external Proportional/Integral (PI) regulator network components to match motor characteristics.

## APPLICATIONS

The PW-82520R is ideal for space and radiation tolerant applications requiring current regulation and/or holding torque at zero input command. System applications that can use the PW-82520R are: pumps, actuators, antenna position, environmental control and reaction/momentum wheel systems using brushless and brush motors. Available in a 1 and 3 amp small DIP-style and a 10 amp flat-pack hybrid package, the PW-82520R is suitable for applications with limited printed circuit board area.

## FEATURES

- Self-Contained 3-Phase Motor Controller
- Operates as Current or Voltage Controller
- 1, 3 and 10 Amp Output Current
- Radiation Tolerant
  - Total Dose: 100 Krads
  - SEU: > 100 MeV/mg/cm$^2$
- 1.5% Linearity
- 3% Current Regulating Accuracy
- User-Programmable Compensation
- 10 KHz - 100 KHz PWM Frequency
- Complementary Four-Quadrant Operation
- Holding Torque through Zero Current
- Cycle-by-Cycle Current Limit
- Non-Radiation Tolerant versions of this product are also available (see PW-82520/21N data sheet)

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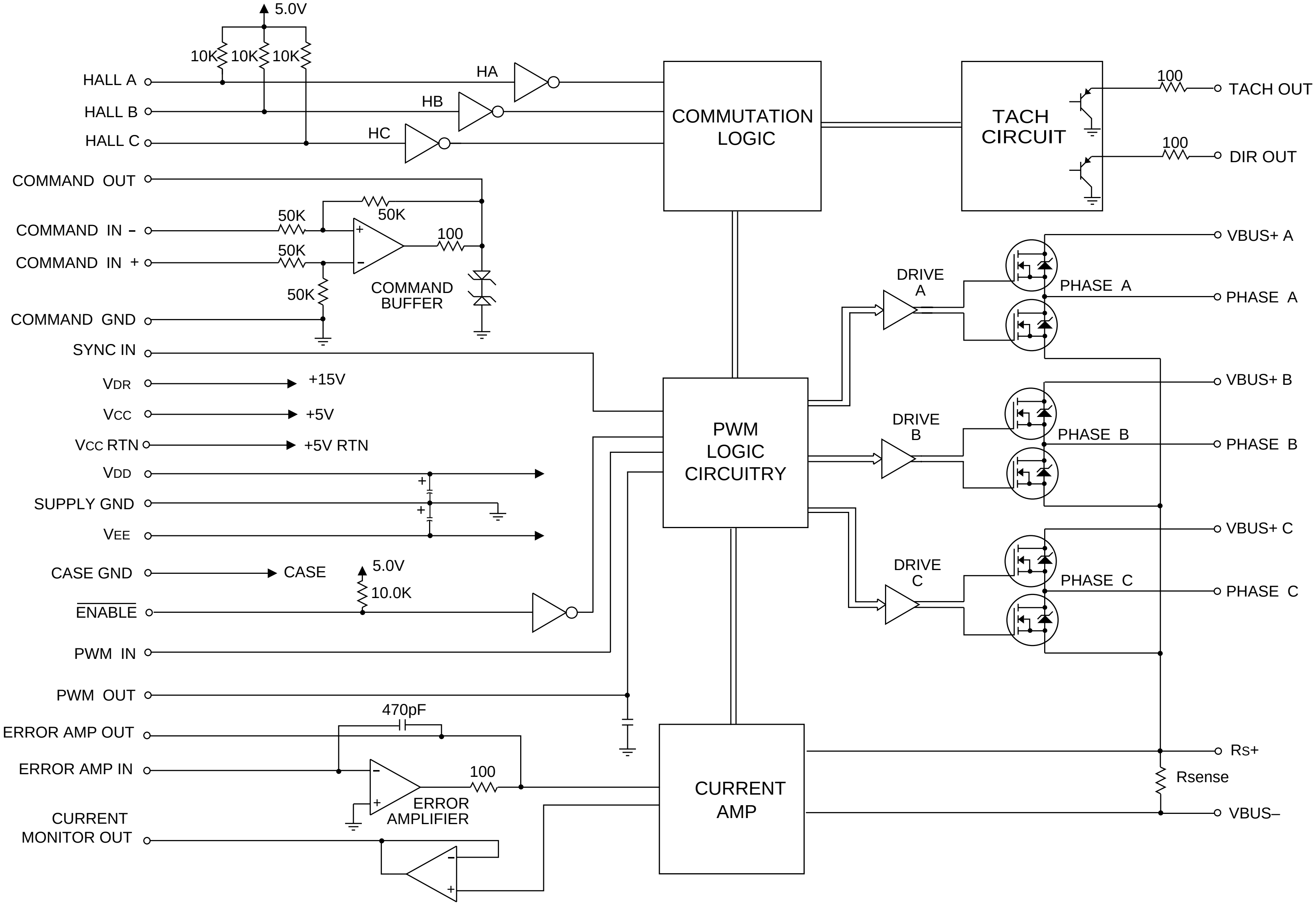


**FIGURE 1. PW-82520R BLOCK DIAGRAM**

## TABLE 1. PW-82520R ABSOLUTE MAXIMUM RATINGS (Tc = +25°C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | VALUE | UNITS |
|---|---|---|---|
| **BUS VOLTAGE** | VBUS+ A,B,C | 100.0 | Vdc |
| **+15V SUPPLY** | $V_{DR}$ | +17.5 | Vdc |
| **+5V TO +15V** | $V_{DD}$ | +17.5 | Vdc |
| **+5V SUPPLY** | $V_{CC}$ | +5.5 | Vdc |
| **-5V TO -15V** | $V_{EE}$ | -17.5 | Vdc |
| **VBUS- TO GND**<br>Voltage Differential | $V_{GNDDIF}$ | 0V to $V_{DD}$ +1.0 | Vdc |
| **CONTINUOUS OUTPUT CURRENT** | $I_{OC}$ | | |
| PW-82520R1 | | 1 | A |
| PW-82520R3 | | 3 | A |
| PW-82520R0 | | 10 | A |
| **PEAK OUTPUT CURRENT (PULSED, t = 50 µS)** | $I_{PEAK}$ | | |
| PW-82520R1 | | 3.0 | A |
| PW-82520R3 | | 8.0 | A |
| PW-82520R0 | | 20.0 | A |
| **COMMAND INPUT +** | $V_{CMD}$ + | ±15.0 | Vdc |
| **COMMAND INPUT -** | $V_{CMD}$ - | ±15.0 | Vdc |
| **LOGIC INPUTS**<br>$\overline{\text{ENABLE}}$, SYNC IN, HA, HB, HC,<br>ERROR AMP IN, PWM IN | $V_{IH}$ | 7.0 | Vdc |
| **TACH OUT / DIR OUT** | $V_{OH}$ | 40 | Vdc |
| **TACH OUT / DIR OUT** | $I_{OL}$ | 20 | mA |

## TABLE 2. PW-82520R SPECIFICATIONS (UNLESS OTHERWISE SPECIFIED, VBUS=28VDC, $V_{DR}$=+15V, $V_{CC}$ = +5V, $V_{DD}$=+5V, $V_{EE}$=-5V, TC = 25°C, LL = 500 µH, 100KRAD, PWM IN = PWM OUT AT ½ FREE RUNNING FREQUENCY)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OUTPUT (PW-82520R1)** | | | | | | |
| Output Current Continuous | $I_{OC}$ | | | | 1 | A |
| Output Current Pulsed | $I_{OP}$ | Pulse Width ≤ 50µsec | | | 3 | A |
| Current Limit | $I_{CL}$ | | 1.3 | | 2.25 | A |
| Current Offset | $I_{OFFSET}$ | FIGURE 7, $V_{CMD}$ = 0V | -20 | | +20 | mA |
| Output On-Resistance | $R_{ON}$ | +25°C | | | 0.60 | Ω |
| | | +85°C | | | 0.90 | Ω |
| Output Conductor Resistance | $R_{C}$ | +25°C | | | 0.06 | Ω |
| | | +85°C | | | 0.08 | Ω |
| Diode Forward Voltage Drop | $V_{F}$ | $I_{D}$ = 1A | | | .65 | V |
| **OUTPUT (PW-82520R3)** | | | | | | |
| Output Current Continuous | $I_{OC}$ | | | | 3 | A |
| Output Current Pulsed | $I_{OP}$ | Pulse Width ≤ 50µsec | | | 8 | A |
| Current Limit | $I_{CL}$ | | 3.25 | | 4.75 | A |
| Current Offset | $I_{OFFSET}$ | FIGURE 7, $V_{CMD}$ = 0V | -20 | | +20 | mA |
| Output On-Resistance | $R_{ON}$ | +25°C | | | 0.18 | Ω |
| | | +85°C | | | 0.27 | Ω |
| Output Conductor Resistance | $R_{C}$ | +25°C | | | 0.06 | Ω |
| | | +85°C | | | 0.08 | Ω |
| Diode Forward Voltage Drop | $V_{F}$ | $I_{D}$ = 3A | | | .85 | V |
| **OUTPUT (PW-82520R0)** | | | | | | |
| Output Current Continuous | $I_{OC}$ | | | | 10 | A |
| Output Current Pulsed | $I_{OP}$ | Pulse Width ≤ 50µsec | | | 20 | A |
| Current Limit | $I_{CL}$ | | 11 | | 14 | A |
| Current Offset | $I_{OFFSET}$ | FIGURE 7, $V_{CMD}$ = 0V | -100 | | +100 | mA |
| Output On-Resistance | $R_{ON}$ | +25°C | | | 0.055 | Ω |
| | | +85°C | | | 0.075 | Ω |
| Output Conductor Resistance | $R_{C}$ | +25°C | | | 0.06 | Ω |
| | | +85°C | | | 0.08 | Ω |
| Diode Forward Voltage Drop | $V_{F}$ | $I_{D}$ = 10A | | | .6 | V |

### TABLE 2. PW-82520R SPECIFICATIONS (CONTINUED)
### (UNLESS OTHERWISE SPECIFIED, VBUS=28VDC, $V_{DR}$=+15V, $V_{CC}$ = +5V, $V_{DD}$=+5V, $V_{EE}$=-5V, TC = 25°C, LL = 500 µH, 100KRAD, PWM IN = PWM OUT AT ½ FREE RUNNING FREQUENCY)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PROPAGATION DELAY** | Td (on) | From 0.8V on $\overline{\text{ENABLE}}$ to 90% of VBUS | | | 40 | µs |
| | Td (off) | From 2.4V on $\overline{\text{ENABLE}}$ to 10% of VBUS | | | 20 | µs |
| **SWITCHING CHARACTERISTICS (PW-82520R1)** | | | | | | |
| Upper Drive | | Rise Time =<br>90% to 10% of VBUS<br>Fall Time =<br>10% to 90% of VBUS<br>$I_O$= 1A | | | | |
| Turn-on Rise Time | $t_r$ | | | 75 | | ns |
| Turn-off Fall Time | $t_f$ | | | 30 | | ns |
| Lower Drive | | | | | | |
| Turn-on Rise Time | $t_r$ | | | 50 | | ns |
| Turn-off Fall Time | $t_f$ | | | 60 | | ns |
| **SWITCHING CHARACTERISTICS (PW-82520R3)** | | | | | | |
| Upper Drive | | Rise Time =<br>90% to 10% of VBUS<br>Fall Time =<br>10% to 90% of VBUS<br>$I_O$= 3A | | | | |
| Turn-on Rise Time | $t_r$ | | | 150 | | ns |
| Turn-off Fall Time | $t_f$ | | | 150 | | ns |
| Lower Drive | | | | | | |
| Turn-on Rise Time | $t_r$ | | | 160 | | ns |
| Turn-off Fall Time | $t_f$ | | | 130 | | ns |
| **SWITCHING CHARACTERISTICS (PW-82520R0)** | | | | | | |
| Upper Drive | | Rise Time =<br>90% to 10% of VBUS<br>Fall Time =<br>10% to 90% of VBUS<br>$I_O$= 10A | | | | |
| Turn-on Rise Time | $t_r$ | | | 200 | | ns |
| Turn-off Fall Time | $t_f$ | | | 200 | | ns |
| Lower Drive | | | | | | |
| Turn-on Rise Time | $t_r$ | | | 200 | | ns |
| Turn-off Fall Time | $t_f$ | | | 200 | | ns |
| **CURRENT MONITOR AMP (PW-82520R1/R3/R0)** | | | | | | |
| Current Monitor Offset | | Ioc = 0A | -10 | | +10 | mVdc |
| Output Current | | | -10 | | +10 | mA |
| Output Resistance | Rout | | | | 1 | Ω |
| **CURRENT MONITOR AMP (PW-82520R1)** | | | | | | |
| Current Monitor Gain | | | | 4 | | V/A |
| **CURRENT MONITOR AMP (PW-82520R3)** | | | | | | |
| Current Monitor Gain | | | | 1.33 | | V/A |
| **CURRENT MONITOR AMP (PW-82520R0)** | | | | | | |
| Current Monitor Gain | | | | 0.40 | | V/A |
| **CURRENT COMMAND** | | Tested using circuit shown in FIGURE 7 | | | | |
| Transconductance Ratio | G | | | | | |
| PW-82520R1 | | Io = 1A | 0.24 | 0.25 | 0.26 | A/V |
| PW-82520R3 | | Io = 3A | 0.73 | 0.75 | 0.77 | A/V |
| PW-82520R0 | | Io = 10A | 2.40 | 2.50 | 2.60 | A/V |
| Non-Linearity | | | -1.5 | | +1.5 | % FSR |
| Temperature Coefficient of G | | | | 0.038 | | % FSR/°C |
| **VBUS+ SUPPLY** | | | | | | |
| Nominal Operating Voltage | Vnom | | 18 | 28 | 70 | Vdc |
| **+15V SUPPLY** | | | | | | |
| Voltage | $V_{DR}$ | | +13.5 | +15.0 | +16.5 | Vdc |
| Current | | | | | | |
| Disabled (**PW-82520R1/R3/R0**) | $I_{DR}$ | $\overline{\text{ENABLE}}$ = high | | | 100 | µA |
| Enabled | | | | | | |
| **PW-82520R1** | $I_{DR}$ | $\overline{\text{ENABLE}}$ = low | | 8 | 15 | mA |
| **PW-82520R3** | $I_{DR}$ | $\overline{\text{ENABLE}}$ = low | | 18 | 25 | mA |
| **PW-82520R0** | $I_{DR}$ | $\overline{\text{ENABLE}}$ = low | | 40 | 60 | mA |
| **+5V SUPPLY** | | | | | | |
| Voltage | $V_{CC}$ | | +4.5 | +5.0 | +5.5 | Vdc |
| Current | $I_{CC}$ | | | 40 | 60 | mA |
| **+5V TO +15V SUPPLY** | | | | | | |
| Voltage | $V_{DD}$ | | +4.5 | | +16.5 | Vdc |
| Current | $I_{DD}$ | | | 35 | 50 | mA |
| **-5V TO -15V SUPPLY** | | | | | | |
| Voltage | $V_{EE}$ | | -16.5 | | -4.5 | Vdc |
| Current | $I_{EE}$ | | | 40 | 50 | mA |

### TABLE 2. PW-82520R SPECIFICATIONS (CONTINUED)
### (UNLESS OTHERWISE SPECIFIED, VBUS=28VDC, $V_{DR}$=+15V, $V_{CC}$ = +5V, $V_{DD}$=+5V, $V_{EE}$=-5V, TC = 25°C, LL = 500 µH, 100KRAD, PWM IN = PWM OUT AT ½ FREE RUNNING FREQUENCY)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SYNC IN** | | | | | | |
| Low | $V_{IL}$ | | | | 0.8 | Vdc |
| High | $V_{IH}$ | | 2.4 | | | Vdc |
| Duty Cycle | D.C. | | 49 | 50 | 51 | % |
| SYNC range as % of free-run frequency | | | 100 | | 120 | % |
| Input Impedance | $R_{IN}$ | | | 10 | | KΩ |
| **PWM IN** | | | | | | |
| + Peak Voltage | $V_{P+}$ | Vcc = 4.5 - 5.5V | 2.3 | 2.5 | 2.8 | V |
| - Peak Voltage | $V_{P-}$ | | -2.8 | -2.5 | -2.3 | V |
| Frequency | | | | | | |
| **PW-82520R1/R3** | $f_{PWM}$ | | 10 | | 110 | KHz |
| **PW-82520R0** | $f_{PWM}$ | | 10 | | 55 | KHz |
| Linearity Error | LIN | | -2 | | +2 | % |
| Duty Cycle | D.C. | | 49 | 50 | 51 | % |
| **PWM OUT** | | | | | | |
| Free Run Frequency | | | | | | |
| **PW-82520R1/R3** | $f_{PWM}$ | | 95 | 100 | 105 | KHz |
| **PW-82520R0** | $f_{PWM}$ | | 47.5 | 50 | 52.5 | KHz |
| Stability, Temperature | | Full Temp Range | | 0.5 | 2.0 | % |
| **HALL SIGNALS (**HA, HB, HC) | | | | | | |
| Logic 0 | $V_{IL}$ | | | | 0.8 | Vdc |
| Logic 1 | $V_{IH}$ | | 1.4 | | | Vdc |
| **$\overline{\text{ENABLE}}$** | | | | | | |
| Enabled | $V_{IL}$ | | | | 0.8 | Vdc |
| Disabled | $V_{IH}$ | | 2.0 | | | Vdc |
| **TACH OUT/ DIR OUT** | | | | | | |
| Output Voltage | $V_{OL}$ | @ 1 mA | | 0.7 | 1.2 | Vdc |
| Iomax | $I_O$ | | | | 20 | mA |
| **ISOLATION** | | | | | | |
| Case to Ground | | 500 Vdc HIPOT | 10 | | | MΩ |
| **COMMAND IN+/-** | | | | | | |
| Differential Input | $V_{CMD}$ | | -4 | | +4 | Vdc |
| Input Offset | | | | | 800 | µV |
| Input Offset Drift | | | | 2 | | µV/°C |
| **COMMAND OUT** | | | | | | |
| Internal Voltage Clamp | $V_{CLAMP}$ | | -5.8 | | +5.8 | Vdc |
| Slew Rate | | | | 3 | | V/µs |
| Settling Time | | $V_O$ = 0.2 - 4.5V | | 1.4 | | µs to 0.1% |
| **THERMAL (PW-82520R1/R3/R0)** | | | | | | |
| Junction Temperature | Tj | | | | +150 | °C |
| Case Operating Temperature | $T_C$ | | -55 | | +125 | °C |
| Case Storage Temperature | $T_{CS}$ | | -65 | | +150 | °C |
| **THERMAL (PW-82520R1)** | | | | | | |
| Thermal Resistance | | | | | | |
| Junction-Case | θj-c | | | | 25 | °C/W |
| Case-Air | θc-a | | | | 10 | °C/W |
| **THERMAL (PW-82520R3)** | | | | | | |
| Thermal Resistance | | | | | | |
| Junction-Case | θj-c | | | | 9 | °C/W |
| Case-Air | θc-a | | | | 10 | °C/W |
| **THERMAL (PW-82520R0)** | | | | | | |
| Thermal Resistance | | | | | | |
| Junction-Case | θj-c | | | | 4 | °C/W |
| Case-Air | θc-a | | | | 5.5 | °C/W |
| **LEAD SOLDER** | | | | | 10sec @300°C | |
| **WEIGHT** | | | | | | |
| **PW-82520R1/R3** | | | | | 1.7 (48) | oz (g) |
| **PW-82520R0** | | | | | 2.9 (82) | oz (g) |
| **RADIATION** | | | | | | |
| Total dose | | | 100 | | | Krad |
| Dose Rate | | | 0.5 | | | Rad/Sec |
| SEU at LET (Linear Energy Transfer) level | | | 100 | | | MeV/mg/$cm^2$ |
| Latch-up Immune | | | 100 | | | MeV/mg/$cm^2$ |

## INTRODUCTION

The PW-82520R is a radiation hardened, 3-phase high performance current control (torque loop) motor controller hybrid, which provides true four-quadrant control through zero current (Refer to FIGURE 1. PW-82520R Block Diagram). Its high Pulse Width Modulation (PWM) switching frequency makes it suitable for operation with low inductance motors. The PW-82520R hybrids can accept either single-ended or differential mode command signals. The current gain can be easily programmed to match the end user system requirements. The addition of an externally wired compensation network provides the user with optimum control of a wide range of loads.

The PW-82520R uses single point current sense technology with an internal non-inductive hybrid sense resistor ($R_{SENSE}$), which yields a highly linear current output over the full -55°C to +125°C military temperature range. The output current non-linearity is less than 1.5% and the total error due to all the factors such as offset, initial component accuracy, etc., is maintained well below 3% of the full scale rated output current.

The Hall sensor interface for current commutation has built-in decoder logic that ignores illegal codes and ensures that there is no cross conduction. The Hall sensor inputs are internally pulled up to +5V and can be driven from open-collector outputs.

The PWM frequency can be programmed externally by adding a capacitor from PWM OUT to PWM GND. Multiple PW-82520R's can be synchronized in two ways: 1) by using one device as a master and connecting its PWM OUT pin to the PWM IN of all the other slave devices, or 2) by applying a master SYNC pulse from an external source to the PWM IN pins on all devices to be synchronized.

The $\overline{\text{ENABLE}}$ input signal provides quick start and shutdown of the internal PWM. In addition, built-in under voltage fault protection turns off the output in case of improper power supply voltages. The hybrid features dual current limiting functions. The input command amplifier output is limited to ±5V, limiting the motor current under normal operation. In addition, there is a cycle-by-cycle current limit, which kicks in to protect the hybrid as well as the load (see TABLE 2 for $I_{CL}$ limits).

## BASIC OPERATION AND ADVANTAGES

The PW-82520R utilizes a complementary four-quadrant drive technique to control current in the load. The complementary drive has the following advantages over standard drives:

1. Holding torque in the motor at zero commanded current
2. Linear current control through zero
3. No deadband at zero

The complementary drive design produces a 50% PWM duty cycle in response to a zero current command. During a zero current command the benefit of a complementary 4 quadrant drive over a standard 4 quadrant is as follows:

### *COMPLEMENTARY (FIGURES 2, 3A)*

Complementary Drives produce a bi-directional holding torque by driving a balanced bi-polar current into the motor that has an average value of zero.

During the first quarter of the PWM cycle (starting at time zero on FIGURE 3A) the MOSFET's, PHASE A UPPER (UA) and PHASE B LOWER (LB) (FIGURE 2), are turned on. This allows current flow from phase A to phase B to increase to +Imax.

During the second quarter of the PWM cycle, the first pair of transistors, UA and LB are turned off and a second pair PHASE A LOWER (LA) & PHASE B UPPER (UB) (FIGURE 2) are turned on. This allows the current in phase A & B from the previous quarter cycle to decrease from Imax to zero. The average current during the first two-quarter cycles is positive.

During the third quarter of the PWM cycle, the second pair of switches UB & LA remain on allowing current to flow, in the negative direction, from phase B to phase A and increase to –Imax as shown in FIGURE 3A.

During the fourth quarter of the PWM cycle, the first pair of switches UA & LB are turned on while the second pair of switches UB & LA are turned off, to allow the current in the inductor to decrease to zero. The average current in the phases for the third and fourth quarter cycles is negative.

The positive current (phase A to B) in the first two-quarter cycles produces a torque in one direction and the negative current (phase B to A) in the third and fourth quarter cycles produces a torque in the opposite direction. The average of the two opposing torques results in a net zero or holding torque.

### *NON-COMPLEMENTARY (FIGURES 2, 3B)*

Non-Complementary Drives produce a unidirectional torque by applying a unipolar current into the motor that has an average positive value as shown in FIGURE 3B.

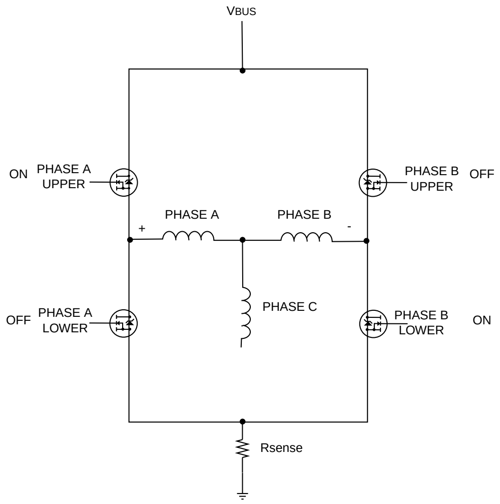
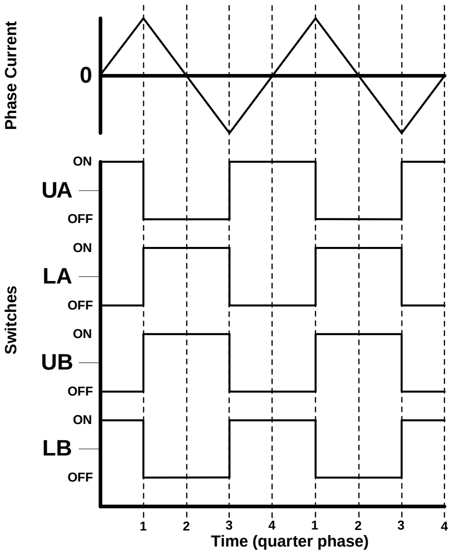
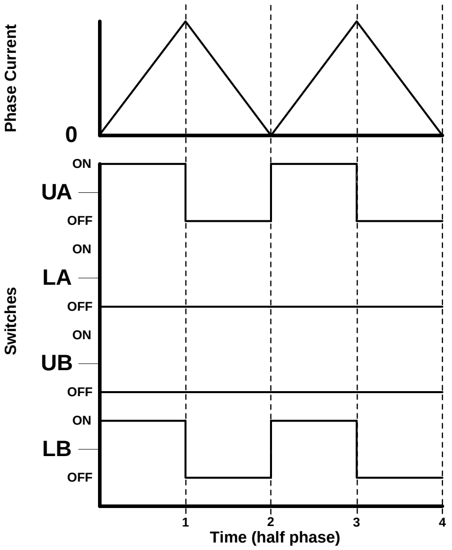


FIGURE 2. COMPLEMENTARY 4-QUADRANT DRIVE FIRST HALF OF PWM CYCLE



Drive Switches and Phase Current vs. Time

**FIGURE 3A. COMPLEMENTARY 4-QUADRANT DRIVE PWM CYCLE**



Drive Switches and Phase Current vs. Time

**FIGURE 3B. STANDARD 4 QUADRANT DRIVE PWM CYCLE**

During the first half of the PWM cycle the MOSFET's, Phase A upper and Phase B lower, are turned on to provide current into the phases.

During the second half of the PWM cycle the drive is in dead time, all transistors are turned off, the motor current continues to flow in the same direction through the device diodes, until it decays to zero.

Current flowing in to and out of the phases produces a net torque in one direction.

### *MAJOR ADVANTAGES*

The advantage of a complementary 4-quadrant drive over a standard 4-quadrant drive is that it provides holding torque during a zero current command. The motor current at 50% duty cycle is simply the magnetizing current of the motor winding. Using the complementary 4-quadrant technique allows the motor direction to be defined by the duty cycle.

Relative to a given switch pair, i.e. Phase A upper and Phase B lower, a duty cycle greater than 50% will result in a clockwise rotation whereas a duty cycle less than 50% will result in a counter clockwise rotation. Therefore, with the use of average current mode control, direction can be controlled without the use of a direction bit and the current can be controlled through zero in a very precise and linear fashion.

The PW-82520R contains all the circuitry required to close an average current mode control loop around a complementary 4-quadrant drive. The PW-82520R use of average current mode control simplifies the control loop by eliminating the need for slope compensation and by eliminating the pole created by the motor inductance. Slope compensation and the pole created by the motor inductance are two limitations normally associated with implementing standard 4 quadrant current mode controls.

## FUNCTIONAL PIN DESCRIPTIONS

### VBUS+A, VBUS+B, VBUS+C

The VBUS+ supply is the power source for the motor phases. The normal operating voltage is 28Vdc and may vary from +18 to +70Vdc with respect to VBUS-. The power stage MOSFETS in the hybrid have an absolute maximum VBUS+ supply voltage rating of 100V. The user must supply sufficient external capacitance or circuitry to prevent the bus supply from exceeding the maximum recommended voltages at the hybrid power terminals under any condition.

### POWER-ON SEQUENCE (**IMPORTANT!**)

The VBUS+ should be applied at least 50ms after $V_{DD}$ and $V_{EE}$ to allow the internal analog circuitry to stabilize. If this is not possible, the hybrid must be powered up in the "disabled" mode.

### VBUS-

This is the high current ground return for VBUS+. This point must be closely connected to SUPPLY GND for proper operation of the current loop.

### $V_{CC}$ (+5V SUPPLY) AND $V_{CC}$ RTN

These inputs are used to power the digital circuitry of the hybrid.

### $V_{DR}$ (+15V SUPPLY)

This input is used to power the gate driver circuitry for the output MOSFETs. There is no power consumption from $V_{DR}$ when the hybrid is disabled.

### $V_{DD}$ (+5V TO +15V SUPPLY), AND $V_{EE}$ (-5V TO -15V SUPPLY)

These inputs can vary from ±5V to ±15V as long as they are symmetrical. $V_{DD}$ and $V_{EE}$ are used to power the small signal analog circuitry of the hybrid. Please note that using ±5V supply will reduce the quiescent power consumption by approximately 60% when compared to ±15V operation.

## SUPPLY GND

SUPPLY GND is the return for the $V_{DR}$, $V_{EE}$, $V_{DD}$ supplies. The phase current sensing technique of the PW-82520R requires that VBUS- and SUPPLY GND (see FIGURES 6 and 7) be connected together externally (see VBUS- supply).

## CASE GND

This pin is internally connected to the hybrid case. In some applications the user may want to tie this to Ground for EMI considerations.

## HALL A, B, C SIGNALS

These are logic signals from the motor Hall-effect sensors. They use a phasing convention referred to as 120 degree spacing; that is, the output of HA is in phase with motor back EMF voltage VAB, HB is in phase with VBC, and HC is in phase with VCA. Logic “1” (or HIGH ) is defined by an input greater than 2.4Vdc or an open circuit to the controller; Logic “0”(or LOW) is defined as any Hall voltage input less than 0.8Vdc. Internal to the PW-82520R are 10K pull-up resistors tied to +5Vdc on each Hall input.

The PW-82520R will alternately operate with Hall phasing of 60° electrical spacing. If 60° commutation is used, then the output of HC must be inverted as shown in FIGURES 4 and 5. FIGURE 4 illustrates the Hall sensor outputs along with the corresponding back emf voltage they are in phase with.

### *HALL INPUT SIGNAL CONDITIONING*

When the motor is located more than two feet away from the PW-82520R controller or is in a noisy electrical environment the Hall inputs require filtering from noise. It is recommended to use a 1KΩ resistor in series with the Hall signal and a 2000 pF capacitor from the Hall input pin to the Hall supply ground pin as shown in FIGURES 6 and 7.

## PHASE A, B, C

These are the power drive outputs to the motor and switch between VBUS+ Input and VBUS- Input or become high impedance (see TABLE 3).

## $\overline{\text{ENABLE}}$

The $\overline{\text{ENABLE}}$ input is an active low (L) logic signal that enables or disables the internal PWM. In the disable mode (H), the PWM is shut down and the outputs, Phase A, Phase B and Phase C, are in an "off" state and no voltage is applied to the motor.

## TACH OUT

The TACH OUT provides a tachometer signal that is a square wave with a frequency relative to motor speed and is derived from the three Hall inputs HA, HB, HC. The tachometer circuitry combines these three signals into a single pulse train as a 50%-duty-cycle pulse. There are three pulses that occur every 360 electrical degree. The number of pulses per motor revolution is formulated below:

$$\mathrm{Pr} = \frac{P}{2} \text{ x } 3 \text{ (e.g., 6 pulses/revolution for a 4 pole motor)}$$

The motor RPM is:

$$\mathrm{RPM} = \frac{\mathrm{Tf} \text{ x } 60}{\mathrm{Pr}}$$

where:

P = number of motor poles
Pr = number of pulses per revolution
Tf = Tach output frequency cycles/second

## DIR OUT

The DIR OUT indicates the direction the motor is rotating, clockwise (CW) for a LO, or counterclockwise (CCW), indicated as a logic HI.

## CURRENT MONITOR OUT

This is a bipolar analog output voltage representative of motor current. The CURRENT MONITOR OUT will have the same scaling (± 4V for ± full scale current) as the COMMAND IN inputs.

## SYNC IN

This input, as shown in FIGURE 9, is used to synchronize the PWM switching frequency with an external clocking device. The PWM switching frequency can be pulled to up-to 20% faster than its free running frequency.

## PWM IN

The PWM comparator inputs are used to control the PWM pulse width. PWM OUT or an external triangular waveform is connected to this pin.

**WARNING:** Never apply power to the hybrid without connecting either PWM OUT or an external triangular waveform to PWM IN! Failure to do so may result in one or more outputs latching on.

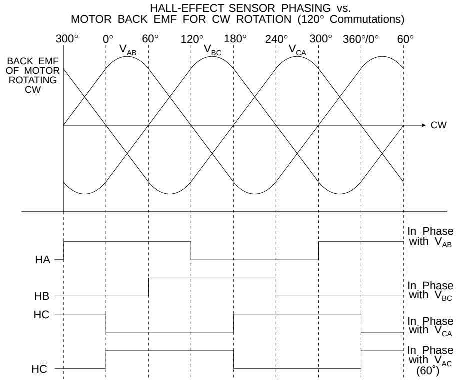
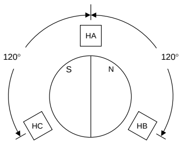
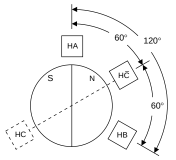


**FIGURE 4. HALL PHASING**



REMOTE POSITION SENSOR (HALL) SPACING FOR
120 DEGREE COMMUTATION



REMOTE POSITION SENSOR (HALL) SPACING FOR
60 DEGREE COMMUTATION

**FIGURE 5. HALL SENSOR SPACING**

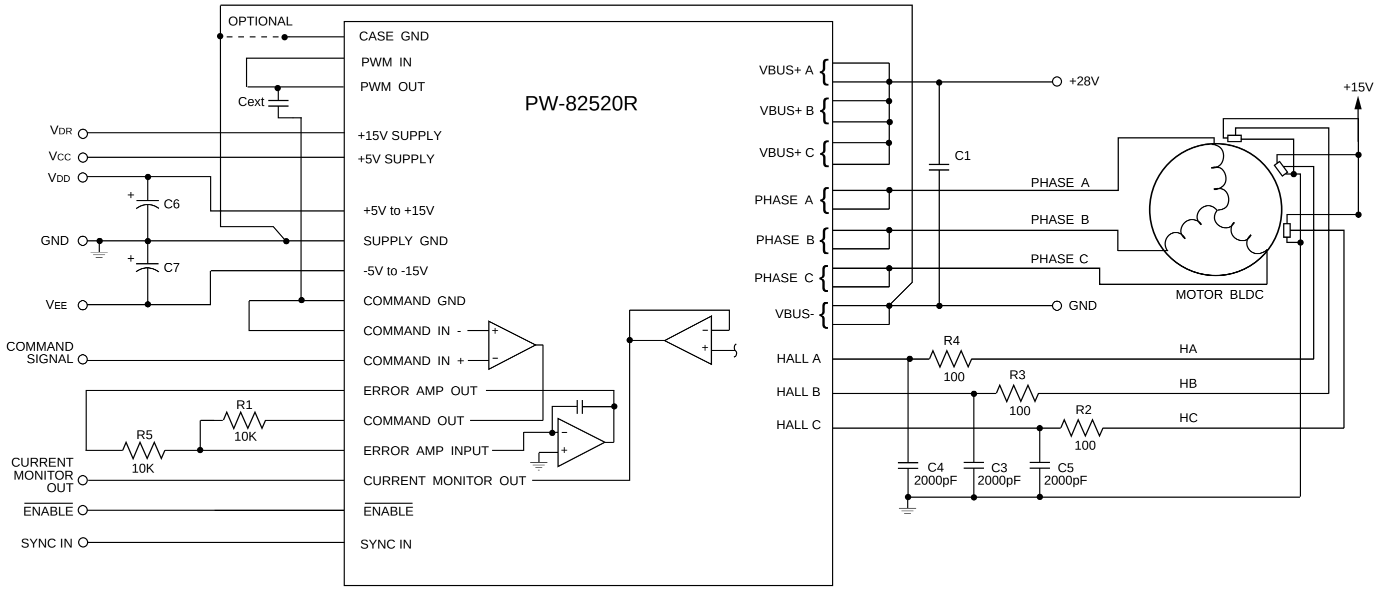


FIGURE 6. VOLTAGE CONTROL HOOK-UP

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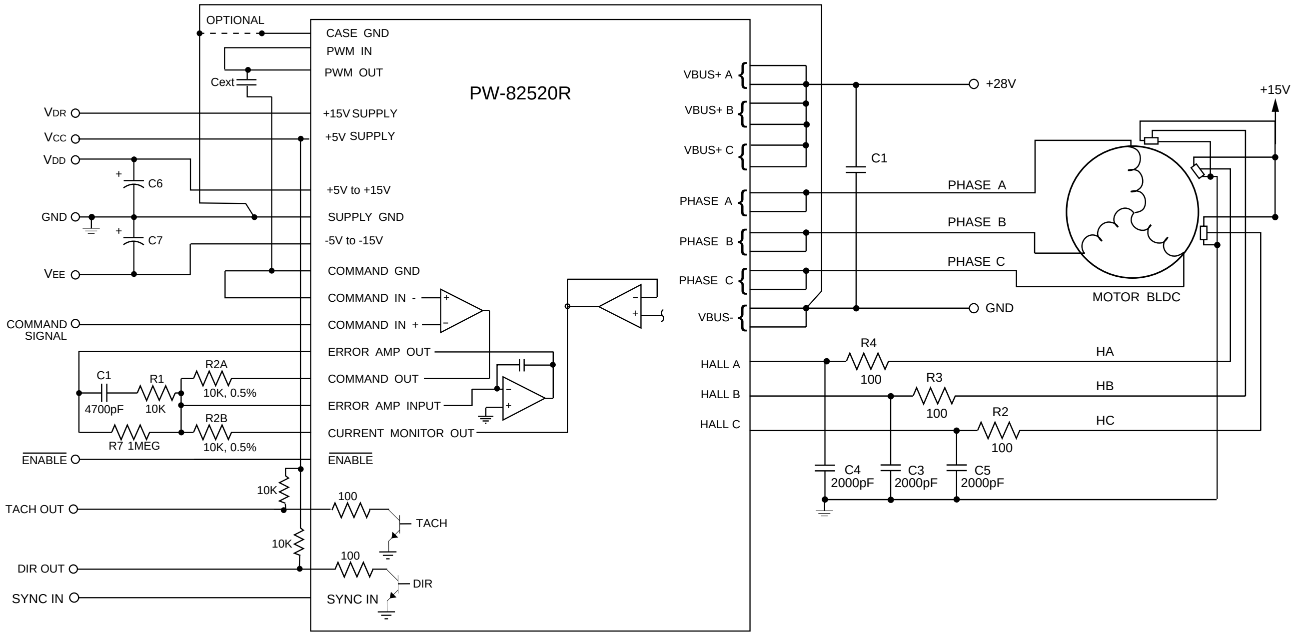


FIGURE 7. TORQUE (CURRENT) CONTROL HOOK-UP

### *PWM FREQUENCY*

The PWM frequency from the PW-82520R1/R3 (PW-82520R0) PWM OUT pin will free-run at a frequency of 100KHz ± 5KHz (50KHz ± 2.5KHz). The PWM frequency is user adjustable from 100KHz (50KHz) down to 10KHz through the addition of an external capacitor. The PWM triangular waveform generated internally is brought out to the PWM OUT pin. This output, or an external triangular waveform generated by the user, may be connected to PWM IN on the hybrid.

## PWM OUT

This is the output of the internally generated PWM triangular waveform. It is normally connected to PWM IN. The frequency of this output may be lowered by connecting an NPO capacitor (Cext) between PWM OUT and COMMAND GND. The PWM frequency is determined by the following formulas:

PW-82520R1, R3:

$$\frac{33.0\text{E-}6}{330\text{pF} + C_{EXT}\text{pF}}$$

PW-82520R0:

$$\frac{16.5\text{E-}6}{330\text{pF} + C_{EXT}\text{pF}}$$

## ERROR AMP IN, ERROR AMP OUT

These are the input and output pins for the error amplifier and are used for compensation.

### *COMPENSATION*

The PI regulator in the PW-82520R can be tuned to a specific load for optimum performance. FIGURE 8 shows the standard current loop configuration and tuning components. By adjusting R1, R2 and C1, the amplifier can be tuned. The value of R1, C1 will vary, depending on the loop bandwidth requirement.

## COMMAND IN+, COMMAND IN- , COMMAND GROUND, COMMAND OUT

These are the connection pins for the command amplifier. The command amplifier has a differential input that operates from a ±4Vdc full-scale analog current command. The command amplifier output signal is internally limited to approximately ±5Vdc to prevent the amplifier from saturating. The input impedance of the command amplifier is 50KΩ.

The PW-82520R can be used either as a current or voltage mode controller. When used as a torque controller (current mode), the input command signal is processed through the command buffer, which is internally limited to ±5Vdc. The output of the buffer (command out) is summed with the current monitor output into the error amplifier. External compensation is used on the error amplifier, so the response time can be adjusted to meet the application.

When used in the voltage mode, the voltage command signal is applied to the command amplifier to control the voltage applied to the motor. The command amplifier output is coupled into the error amplifier. The error amplifier directly varies the PWM duty cycle to control the voltage applied to the motor phase. The nominal PWM frequency in the voltage mode is 50% with zero volts applied to the command input. The PWM duty cycle is varied by the voltage applied to the command input according to the transfer function, 12% per volt applied to the command input. The duty cycle range of the output voltage is limited to approximately 5-95% in both current and voltage modes.

### *COMMAND GND*

COMMAND GND is used when the command buffer is used single-ended and the COMMAND IN- or COMMAND IN+ is tied to COMMAND GND.

### *TRANSCONDUCTANCE RATIO AND OFFSET*

When the PW-82520R is used in the current mode, the command inputs (COMMAND IN+ and COMMAND IN-) are designed such that ±4Vdc on either input, with the other input connected to ground will result in ± full-scale current (Continuous Output Current: (Ioc) - Refer to TABLE 2) flow into the load. The dc current transfer ratio accuracy is ±5% of the rated current including offset and initial component accuracy. The initial output dc current offset with both COMMAND IN+ and COMMAND IN- tied to the ground will be as shown in TABLE 2 (Ioffset) when measured using a load of 0.5mH and 1.0W at ambient room temperature with standard current loop compensation (see FIGURE 8). The winding phase current error shall be within the cumulative limits of the transconductance ratio error and the offset error.

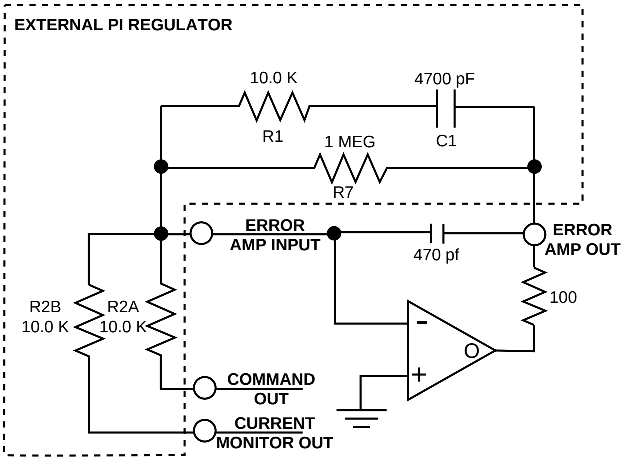


**FIGURE 8. STANDARD PI CURRENT LOOP**

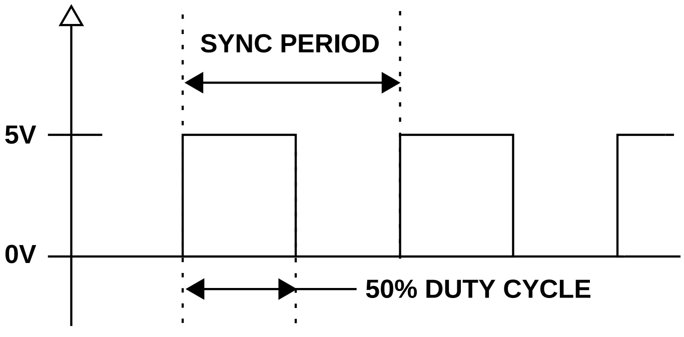


**FIGURE 9. SYNC INPUT SIGNAL**

### Rs +

Rs + is the high side of the sense resistor used for non-scaled test purposes only. Accuracy is not a guaranteed parameter.

## OUTPUT CURRENT

Output current derating as a function of the hybrid case temperature is provided in FIGURES 11 and 12. The hybrid contains internal pulse by pulse current limit circuitry to limit the output current during fault conditions. (See TABLE 2) Current Limit accuracy is +10/-15%.

**WARNING!** The PW-82520R does not have short circuit protection. The PW-82520R must see a minimum of 100µH inductive load phase-to-phase or enough phase-to-phase line-to-line resistance to limit the continuous output current to less than $I_{OC}$ at all times. Operation into a short or a condition that requires excessive output current will damage the hybrid.

## THERMAL OPERATION

It is necessary that the bottom surface (heat sink surface - FIGURES 13 and 14) of the PW-82520R be mounted to a heat sink. This heat sink shall have the capacity to dissipate heat generated by the hybrid at all levels of current output, up to the peak limit, while maintaining the case temperature limit as per FIGURE 11.

## RADIATION

### TOTAL DOSE

The hybrid shall operate, as specified in TABLE 2, when subjected to a total dose radiation environment of 100KRad (Si) at a dose rate of 0.5 Rad/sec.

TABLE 3. COMMUTATION TRUTH TABLE

| INPUTS | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|
| ENABLE | COMMAND IN | HALL | | | PHASE | | | DIR | DIR OUT |
| | POLARITY | A | B | C | A | B | C | | |
| L | POS | 1 | 0 | 1 | Z | L | H | CW | L |
| L | POS | 1 | 0 | 0 | H | L | Z | CW | L |
| L | POS | 1 | 1 | 0 | H | Z | L | CW | L |
| L | POS | 0 | 1 | 0 | Z | H | L | CW | L |
| L | POS | 0 | 1 | 1 | L | H | Z | CW | L |
| L | POS | 0 | 0 | 1 | L | Z | H | CW | L |
| L | NEG | 0 | 0 | 1 | H | Z | L | CCW | H |
| L | NEG | 0 | 1 | 1 | H | L | Z | CCW | H |
| L | NEG | 0 | 1 | 0 | Z | L | H | CCW | H |
| L | NEG | 1 | 1 | 0 | L | Z | H | CCW | H |
| L | NEG | 1 | 0 | 0 | L | H | Z | CCW | H |
| L | NEG | 1 | 0 | 1 | Z | H | L | CCW | H |
| H | - | - | - | - | Z | Z | Z | - | X |

1=Logic Voltage >2.4Vdc, 0=Logic Voltage < 0.8Vdc
* DIRECTION is based on the convention shown in FIGURE 4.
Actual motor set up might be different.

### SINGLE EVENT UPSET

The hybrid shall be Single Event Upset (SEU) immune and still meet the requirements of TABLE 2 for a Linear Energy Transfer (LET) level > 100 MeV/mg/cm$^2$.

### LATCH-UP

The hybrid is latch-up immune and meets the requirement of TABLE 2 for a LET (Linear Energy Threshold) level > 100 MeV/mg/cm$^2$.

***NOTE:*** 100KRad (Si) total dose of radiation is usually two to three times the operational level of commercial and military satellites. This is a large cost saving for the end users since Lot Acceptance Tests (LAT) are usually not required.

## BRUSH MOTOR OPERATION

The PW-82520R can also be used as a brush motor controller for current or voltage control in an H-Bridge configuration. The PW-82520R would be connected as shown in FIGURE 10.

All other connections are as shown in either FIGURES 6 or 7 depending on voltage or current mode operation. The Hall inputs are wired per TABLE 4. A positive input command will result in positive current to the motor out of Phase A.

## OPTIONAL FEATURES

### EXTERNAL SENSING RESISTOR

An external sense resistor can be connected to replace the internal resistor if this option is required. Please contact factory for this option.

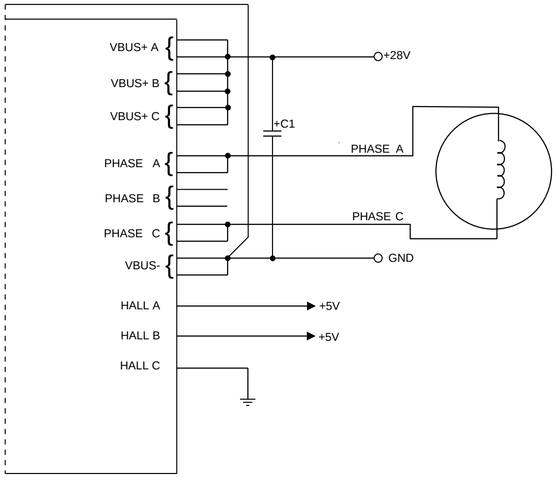


FIGURE 10. BRUSH MOTOR HOOK-UP

TABLE 4. HALL INPUTS FOR H-BRIDGE CONTROLLER

| INPUTS | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|
| ENABLE | COMMAND IN | HA | HB | HC | PH A | PH B | PH C |
| L | Positive | 1 | 1 | 0 | H | Z | L |
| L | Negative | 1 | 1 | 0 | L | Z | H |
| H | - | 1 | 1 | 0 | Z | Z | Z |

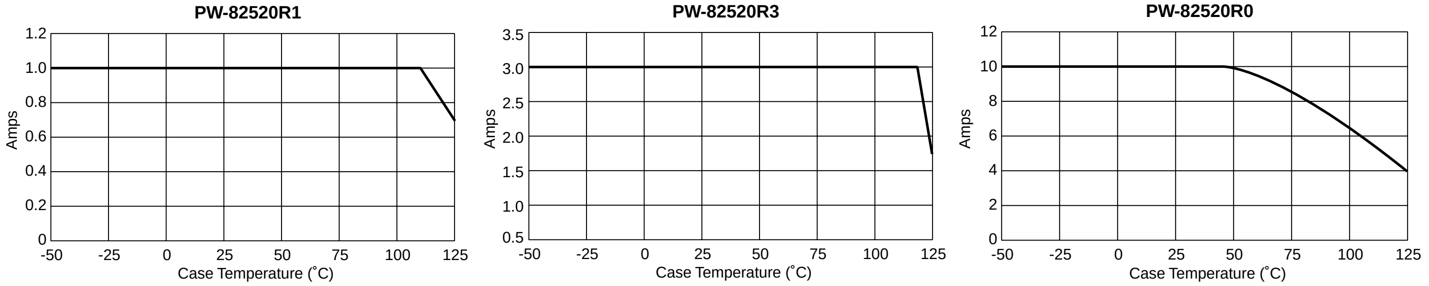


**FIGURE 11. OUTPUT CURRENT FOR CONTINUOUS COMMUTATION (ELECTRICAL > 600RPM, VBUS+ = 28V, PWM = 50KHZ)**

## PW-82520R0 POWER DISSIPATION

There are two major contributors to power dissipation in the motor driver: conduction losses, and switching losses.

### An example calculation is shown below:

VBUS = +28 V (Bus Voltage)

$I_{OA}$ = 3 A, $I_{OB}$ = 7 A (see FIGURE 12)

$f_{PWM}$ = 25 KHz (switching frequency)

ton = 36 µs, T = 40 µs (90% duty cycle) (see FIGURE 12)

Ron = 0.055 Ω (on-resistance, see TABLE 2)

Rc = 0.080 Ω (conductor resistance, see TABLE 2)

ts1 = tf = 200 ns, ts2 = 2tr = 400 ns (see TABLE 2, FIGURE 12)

$$I_{motor\ rms} = \sqrt{\left(I_{OB}I_{OA} + \frac{(I_{OB} - I_{OA})^2}{3}\right)\left(\frac{ton}{T}\right)}$$

$$I_{motor\ rms} = \sqrt{\left(7 * 3 + \frac{(7 - 3)^2}{3}\right)\left(\frac{36}{40}\right)}$$

$I_{motor\ rms}$= 4.87 amps

### 1. TRANSISTOR CONDUCTION LOSSES ($P_T$)

$P_T$ = (Imotor rms)$^2$ x (Ron)

$P_T$ = (4.87)$^2$ x (0.055)

$P_T$ = 1.30 Watts

### 2. SWITCHING LOSSES ($P_S$)

$P_S$ = [ VBUS ( $I_{OA}$ (ts1) + $I_{OB}$ (ts2) ) fo] / 2

$P_S$ = [ 28 ( 3 (200 x$10^{-9}$) + 7 (400 x$10^{-9}$) ) 25x$10^3$] / 2

$P_S$ = 1.19 Watts

#### *TRANSISTOR POWER DISSIPATION ( $P_Q$ )*

Pq = $P_T$ + $P_S$

Pq = 1.30 + 1.19 = 2.49 Watts

#### *OUTPUT CONDUCTOR DISSIPATION*

$P_C$ = (Imotor rms)$^2$ x (Rc)

$P_C$ = (4.87)$^2$ x (0.080)

$P_C$ = 1.90 Watts

### 3. TRANSISTOR POWER DISSIPATION FOR CONTINUOUS COMMUTATION (ELECTRICAL > 600RPM)

Pqc = Pq (0.33)

Pqc = (2.49) x (0.33)

Pqc = 0.82 Watts

### 4. TOTAL HYBRID POWER DISSIPATION

$P_{TOTAL}$ = (Pq + Pc) x 2

$P_{TOTAL}$ = (2.49 + 1.90) x 2

$P_{TOTAL}$ = 8.78 Watts

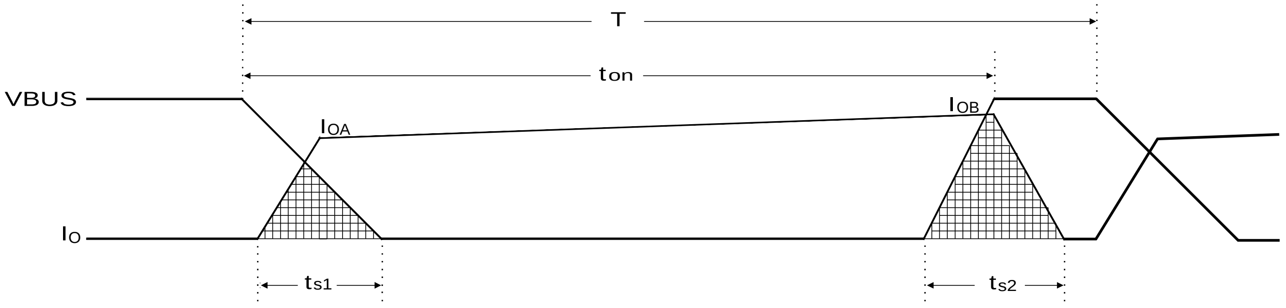
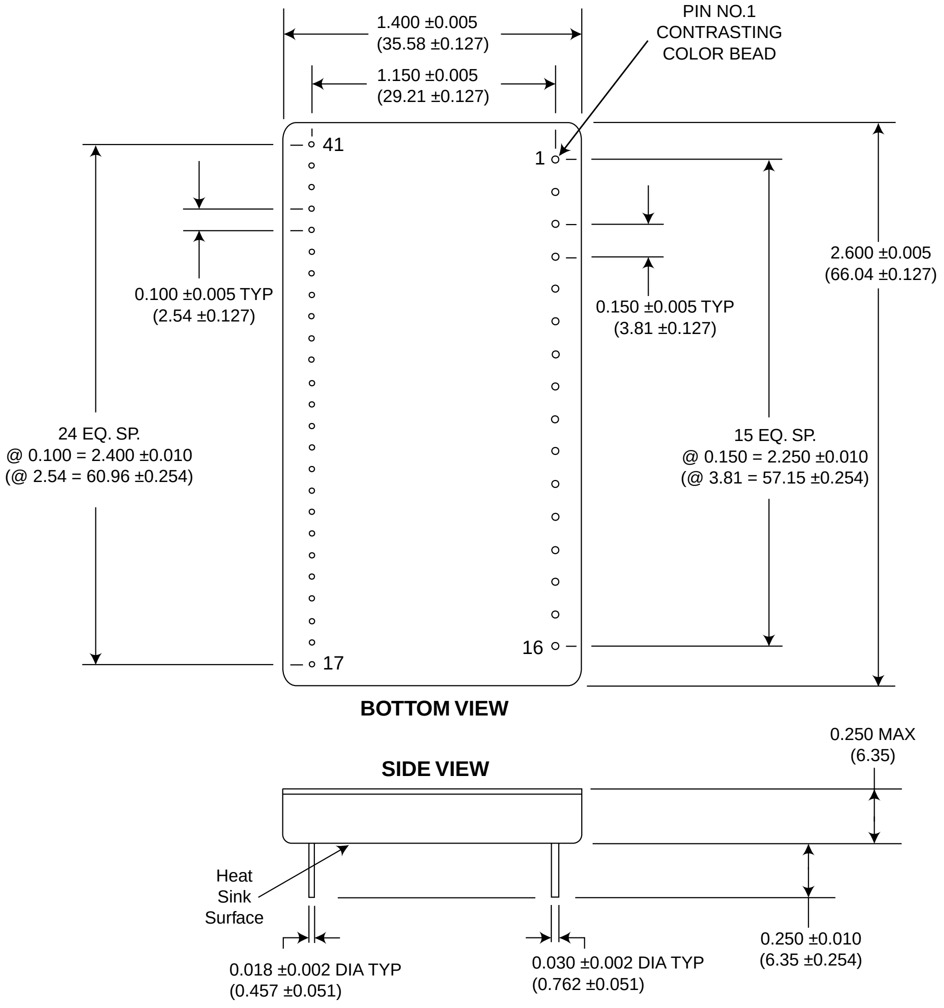


**FIGURE 12. OUTPUT CHARACTERISTICS**

**TABLE 5A. PIN FUNCTIONS**
**PW-82520 R1 AND R3**

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | VBUS+ A | 41 | TACH OUT |
| 2 | VBUS+ A | 40 | DIR OUT |
| 3 | PHASE A | 39 | HALL B |
| 4 | PHASE A | 38 | HALL A |
| 5 | VBUS+ B | 37 | HALL C |
| 6 | VBUS+ B | 36 | $\overline{\text{ENABLE}}$ |
| 7 | PHASE B | 35 | VCC |
| 8 | PHASE B | 34 | VCC RTN |
| 9 | VBUS- | 33 | VDR |
| 10 | VBUS- | 32 | SYNC IN |
| 11 | RS+ | 31 | VDD |
| 12 | RS+ | 30 | SUPPLY GND |
| 13 | VBUS+ C | 29 | VEE |
| 14 | VBUS+ C | 28 | N/C |
| 15 | PHASE C | 27 | N/C |
| 16 | PHASE C | 26 | CURRENT MONITOR OUT |
|  |  | 25 | ERROR AMP IN |
|  |  | 24 | ERROR AMP OUT |
|  |  | 23 | COMMAND OUT |
|  |  | 22 | COMMAND IN - |
|  |  | 21 | COMMAND IN + |
|  |  | 20 | COMMAND GND |
|  |  | 19 | PWM OUT |
|  |  | 18 | PWM IN |
|  |  | 17 | CASE GND |

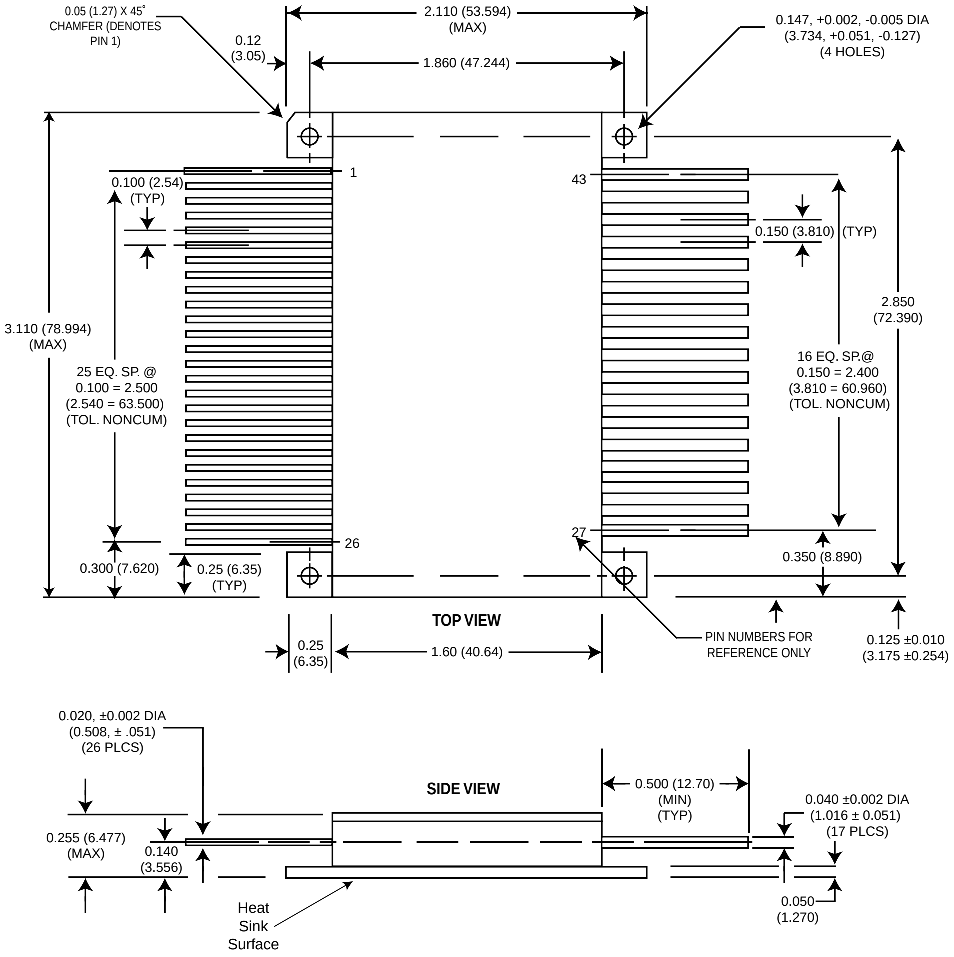


NOTES:
1. DIMENSIONS IN INCHES (MM).
2. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.

FIGURE 13. MECHANICAL OUTLINE (R1 & R3)

## TABLE 5B. PIN FUNCTIONS PW-82520 R0

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | CASE GND | 43 | N/C |
| 2 | N/C | 42 | PHASE C |
| 3 | PWM IN | 41 | PHASE C |
| 4 | PWM OUT | 40 | VBUS+ C |
| 5 | COMMAND GND | 39 | VBUS+ C |
| 6 | COMMAND IN+ | 38 | Rs+ |
| 7 | COMMAND IN- | 37 | Rs+ |
| 8 | COMMAND OUT | 36 | VBUS- |
| 9 | ERROR AMP OUT | 35 | VBUS- |
| 10 | ERROR AMP IN | 34 | PHASE B |
| 11 | CURRENT MONITOR OUT | 33 | PHASE B |
| 12 | N/C | 32 | VBUS+ B |
| 13 | N/C | 31 | VBUS+ B |
| 14 | VEE | 30 | PHASE A |
| 15 | SUPPLY GND | 29 | PHASE A |
| 16 | VDD | 28 | VBUS+ A |
| 17 | SYNC IN | 27 | VBUS+ A |
| 18 | VDR | | |
| 19 | Vcc RTN | | |
| 20 | Vcc | | |
| 21 | $\overline{\text{ENABLE}}$ | | |
| 22 | HALL C | | |
| 23 | HALL A | | |
| 24 | HALL B | | |
| 25 | DIR OUT | | |
| 26 | TACH OUT | | |



NOTES:
1. DIMENSIONS IN INCHES (MM). TOL = ±0.005 (±0.127)
2. LEAD IDENTIFICATION NUMBERS ARE FOR REFERENCE ONLY.

FIGURE 14. MECHANICAL OUTLINE (R0)

## ORDERING INFORMATION

**PW-82520RX- X X 0**

**Reliability Grade:**

0 = Standard DDC Processing, no Burn-In (See table below.)
1 = MIL-PRF-38534 Compliant
2 = B*
3 = MIL-PRF-38534 Compliant with PIND Testing
4 = MIL-PRF-38534 Compliant with Solder Dip
5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
6 = B* with PIND Testing
7 = B* with Solder Dip
8 = B* with PIND Testing and Solder Dip
9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

**Temperature Range:**

1 = -55°C to +125°C
2 = -40°C to +85°C
3 = 0°C to +70°C
4 = -55°C to +125°C with Variables Test Data
5 = -40°C to +85°C with Variables Test Data
8 = 0°C to +70°C with Variables Test Data

**Rating:**

1 = 1A
3 = 3A
0 = 10A

Consult factory for class H+ screening or class K processing.
*Standard DDC Processing with burn-in and full temperature test — see table below.

**STANDARD DDC PROCESSING**

| TEST | MIL-STD-883 | |
|---|---|---|
| | METHOD(S) | CONDITION(S) |
| INSPECTION | 2009, 2010, 2017, and 2032 | — |
| SEAL | 1014 | A and C |
| TEMPERATURE CYCLE | 1010 | C |
| CONSTANT ACCELERATION | 2001 | A |
| BURN-IN | 1015, TABLE 1 | — |

105 Wilbur Place, Bohemia, New York, U.S.A. 11716-2482

**For Technical Support - 1-800-DDC-5757 ext. 7677 or 7381**

**Headquarters, N.Y., U.S.A. -** Tel: (631) 567-5600, Fax: (631) 567-7358
**Southeast, U.S.A. -** Tel: (703) 450-7900, Fax: (703) 450-6610
**West Coast, U.S.A. -** Tel: (714) 895-9777, Fax: (714) 895-4988
**United Kingdom -** Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
**Ireland -** Tel: +353-21-341065, Fax: +353-21-341568
**France -** Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
**Germany -** Tel: +49-(0)8141-349-087, Fax: +49-(0)8141-349-089
**Japan -** Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
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