VSB 1400

VSB Master Module Interface Device

Distinctive Features

- **Bus interface circuitry for multi-master VSB systems**
- VSB master chip contains
  - **Single level arbiter**
  - **Bus requester**
  - **Bus controller**
  - **Supports vectored interrupt acknowledge cycle**
- Supports the following performance enhancing options
  - **Block moves**
  - **Early Bus Busy release**
- **Drives 48mA VSB bus signals**: BREQ*, DS*, BUSY*, PAS*
- **Input hysteresis allows device to monitor VSB signals without additional input buffers**
- **Available in Commercial, Industrial and Military temperature ranges**

Programmable Version Available

If the VSB 1400 does not match the requirements of the design, a programmable version is available (the PLX 448) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ or CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 448 and other information.

Applications

- Bus interface circuitry for slot1 or non slot1 VSB master module in multi-master VSB systems

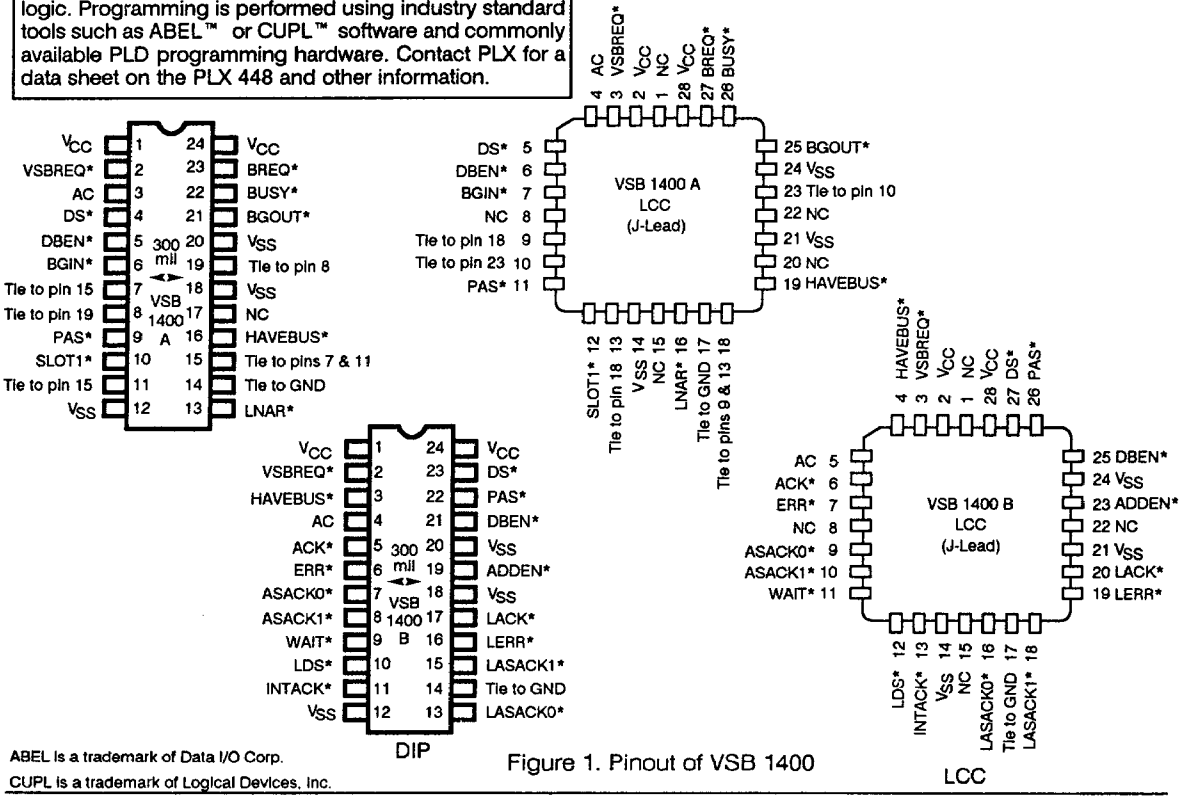
General Description

The VSB 1400 is a CMOS device which incorporates the protocol logic, drivers and buffers required to interface a master, typically a CPU, to the VSB (VME Subsystem Bus). It is packaged in compact 24 pin, 300 mil wide DIP or 28 pin LCC.

The VSB 1400 contains a VSB bus requester, controller and arbiter. The requester portion of the device asserts a VSB bus request in response to a request from the local master. The controller portion of the VSB 1400 supervises all the handshaking between the local master and the slaves. The VSB 1400 is designed to function in a multi-master VSB system, and can reside in any slot.

The protocols in the VSB 1400 are fully asynchronous.

This device is designed to function with any type of slave device or circuitry which meets the VSB specifications.



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CUPL is a trademark of Logical Devices, Inc.

Figure 1. Pinout of VSB 1400

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Pin Description

Device A

Pin LCC	Pin DIP	Signal	Description	I/O	Function
2	1	V_{CC}		–	5V supply.
3	2	VSBREQ*	VSB Request	I	Active low; Local master wants the bus.
4	3	AC	Address Cycle Complete	I	Active high; Indicates to master when address portion of VSB cycle is complete.
5	4	DS*	Data Strobe	I	Active low; Indicates valid data on bus.
6	5	DBEN*	Data Buffer Enable	I	Active low; Data buffer enable.
7	6	BGIN*	Bus Grant In	I	Active low; Bus Grant In from daisy chain or bus request input for slot1 applications.
9	7			I	Tie to pin 15 (DIP) or pin 18 (LCC).
10	8			I	Tie to pin 19 (DIP) or pin 23 (LCC).
11	9	PAS*	Address strobe	I	Active low; Indicates valid address on bus.
12	10	SLOT1*	Slot 1 master	I	Active high; Enables system arbiter for slot 1 masters.
13	11			I	Tie to pin 15 (DIP) or pin 18 (LCC).
14	12	V_{SS}		–	Chip Ground
16	13	LNAR*	Local Next Address Required	O	Active low; Indicates to local master that single or block transfer cycle is complete.
17	14			I	Tie to Ground
18	15			O	Tie to pins 7 and 11 (DIP) or pins 9 and 13 (LCC).
19	16	HAVEBUS*	Have Bus	O	Active low; Indicates to local master that it owns the bus and enables the strobes.
20	17	NC		–	No Connect
21	18	V_{SS}			Chip Ground
23	19			O	Tie to pin 8 (DIP) or pin 10 (LCC).
24	20	V_{SS}		–	Chip Ground
25	21	BGOUT*	Bus Grant Out	O	Active low; Bus Grant output to the daisy chain.
26	22	BUSY*	Busy	O	Active low; Indicates local master controls the bus, 48mA OC.
27	23	BREQ*	Bus Request	O	Active low; Bus request, 48mA OC.
28	24	V_{CC}		–	5V supply.
1, 8 15,22	–	NC		–	No Connect

Note: TS is Tri-state
OC is Open Collector

Pin Description (Con't)

Device B

28Pin LCC	24Pin DIP	Signal	Description	I/O	Function
2	1	V_{CC}		–	5V supply
3	2	VSBREQ*	VSB Request	I	Active low; Local master wants the bus.
4	3	HAVEBUS*	Have Bus	I	Active low; Indicates to local master that it owns the bus and enables the strobes.
5	4	AC	Address Cycle Complete	I	Active high; Indicates to master when address portion of VSB cycle is complete.
6	5	ACK*	Acknowledge	I	Active low; Data is valid or has been accepted.
7	6	ERR*	Error	I	Active low; Bus error or timeout has occurred.
9	7	ASACK0*	Address Transfer Acknowledge	I	Active low; Byte size information and address transfer acknowledge.
10	8	ASACK1*	Address Transfer Acknowledge	I	Active low; Byte size information and address transfer acknowledge.
11	9	WAIT*	Wait	I	Active low; VSB cycle extension or hold.
12	10	LDS*	Local Data Strobe	I	Active low; local master data strobe.
13	11	INTACK*	Interrupt Acknowledge	I	Active low; Interrupt Acknowledge input, indicates that a vectored interrupt acknowledge cycle is being initiated by the local master. If not used, must tie high.
14	12	V_{SS}		–	Chip Ground
16	13	LASACK0*	Local Address Transfer Acknowledge	O	Active low; Byte size information and address transfer acknowledge to local master.
17	14			I	Tie to Ground
18	15	LASACK1*	Local Address Transfer Acknowledge	O	Active low; Byte size information and address transfer acknowledge to local master.
19	16	LERR*	Local Error	O	Active low; Bus error or timeout to local master.
20	17	LACK*	Local Acknowledge	O	Active low; Data validation or acceptance to local master.
21	18	V_{SS}		–	Chip Ground
23	19	ADDEN*	Address Enable	O	Active low; Address buffer enable.
24	20	V_{SS}		–	Chip Ground
25	21	DBEN*	Data Buffer Enable	O	Active low; Data buffer enable.
26	22	PAS*	Address Strobe	I/O	Active low; Indicates valid address on bus, 48mA OC.
27	23	DS*	Data Strobe	I/O	Active low; Indicates valid data on bus, 48mA OC.
28	24	V_{CC}		–	5V supply.
1, 8, 15,22	–	NC		–	No Connect

Note: TS is Tri-state
OC is Open Collector

Detailed Description

The following section describes the VSB 1400 initiating, executing and terminating a data transfer cycle. The system in this configuration is a multi-master VSB system.

Bus Request and Arbitration

The local master initiates a VSB bus request by asserting VSBREQ*. VSBREQ* is generated from the CPU (for example; a 68020) address and function decoder. VSBREQ* is enabled by the CPU's AS*.

If the local master does not currently control the bus (i.e. BUSY* is deasserted), the VSB 1400 will assert BREQ*. For non slot1 applications, if BGIN* is asserted after the bus request, the VSB 1400 bus controller will keep the grant and assert BUSY*. If BGIN* is asserted before the bus request, the controller will generate a bus grant down the daisy chain, BGOUT*.

For slot 1 applications, tie the SLOT 1 and BGIN * inputs high. This engages the serial system arbiter for SLOT 1 masters.

If BUSY* is asserted when VSBREQ* is asserted, the VSB 1400 will wait until the end of the current cycle before issuing the bus grant.

Once the local master has the bus (HAVEBUS* asserted and PAS* asserted), the VSB 1400 will release BUSY*. This allows any other masters requesting the bus to concurrently arbitrate for the bus while the local master is performing data transfers. If BREQ* is asserted and the local master is in slot 1, it will generate a BGOUT*. If the local master is not in slot 1, it will pass BGIN* to BGOUT*.

Address Cycle

After asserting BUSY*, the VSB 1400 will assert HAVEBUS* to the local master to start the address cycle, HAVEBUS* will remain active as long as the local master drives VSBREQ* low.

The VSB 1400 will drive ADDEN* (the address buffer enable signal) provided that AC is deasserted and DS* is high. These two conditions indicate that the previous data cycle is complete. The local master is now ready to put the address on the bus.

When the address on the bus is valid, the VSB 1400 asserts PAS*. The VSB 1400 meets the VSB specification which calls for a minimum 10 nanosecond setup time from address enable (ADDEN*) to PAS*. NOTE: To ensure compliance with this specification, the address buffers should have a propagation delay of less than 15 ns.

ADDEN* remains asserted until the VSB 1400 receives ASACK0,1* from the responding slave and WAIT* is high. If WAIT* is low (indicating participating slaves), the VSB 1400 must also receive AC high before de-asserting ADDEN*. The assertion of these signals verifies that all the responding and participating slaves have received valid addresses and signifies the completion of the address cycle. ASACK0*, ASACK1* contain encoded byte sizing information from the responding slave.

Data Cycle

As soon as the VSB 1400 deasserts ADDEN*, it asserts the data buffer enable signal (DBEN*). The VSB specification requires a 10ns data buffer enable to data strobe (DS*) assertion setup time for write operations. To meet this requirement, the data bus transceivers must have a propagation delay of less than 15ns. The VSB 1400 asserts DS* in response to the assertion of local data strobe (LDS*) by the local master. In addition ACK* and ERR* must be deasserted.

The VSB 1400 will deassert DS* when data has been transferred to or from the responding and participating slaves. To deassert DS*, the VSB 1400 must receive WAIT* high from all the slaves, indicating that they have completed that particular data transfer operation. For the last data cycle (or the only data cycle in the case of a single transfer cycle) the responding slave must drive AC low before driving ACK* low.

For a single transfer cycle, the VSB 1400 deasserts DS* when both WAIT* and VSBREQ* go high. The VSBREQ* edge will occur after the WAIT* edge. PAS*, HAVEBUS* and DBEN* are disabled by the deassertion of VSBREQ* which signifies that the local master no longer needs to own the bus.

Block Transfer Cycle

In a block transfer cycle, LDS* strobes DS* after every data transfer. PAS* and VSBREQ* are held low throughout the block transfer. The slaves hold AC high during all transfers except the last. As mentioned above, the responding slave will drive AC low during the last data cycle to indicate that the address counter has finished counting and has run out of addresses. The last data cycle is similar to the single cycle. The block transfer is terminated in the same way.

Vectored Interrupt Acknowledge Cycle

The VSB 1400 can support a vector interrupt acknowledge master (IHV master). When the local master wishes to acknowledge an interrupt from a VSB INTV slave, it initiates an interrupt acknowledge cycle to the bus. This cycle looks like an address broadcast followed by a read cycle except that the SPACE0,1 signals are both driven low from the master and no address is broadcast from the master. Instead, the slaves contend on the bus to determine who will respond to the interrupt acknowledge cycle. The INTACK* input to the VSB 1400 causes the ADDEN* output not to be asserted during the Interrupt selection phase. Once the master sees WAIT* and AC high and one or both of the ASACK0,1* low, it can proceed with the STATUS/ID transfer phase. Once the master has received all of the STATUS/ID information (LNAR* asserted or master done), it removes VSBREQ* and the interrupt acknowledge cycle is terminated. Note that during the interrupt selection phase before driving LDS* low.

If you do not intend to support the vectored interrupt acknowledge capability, then you must tie INTACK* high.

Bus Release and Cycle Termination

When the responding slave drives AC low in the last data cycle, the VSB 1400 drives LAC* to the local master to indicate the end of the data transfer cycle. The local master can re-

lease VSBREQ* when both LAC* and ACK* are low or just when ACK* is low. VSBREQ* releases PAS* and DS*, signifying the end of the data transfer cycle.

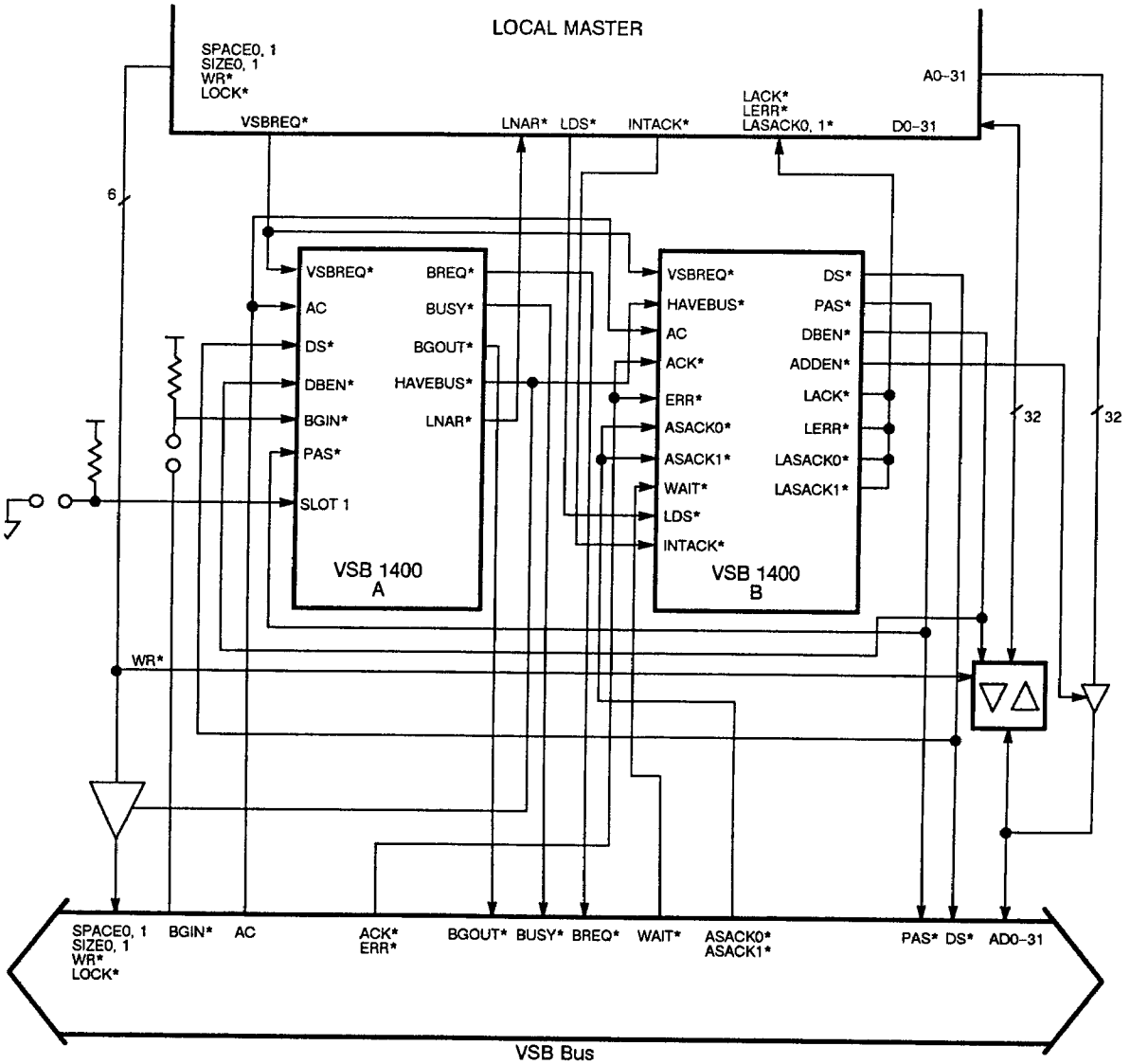


Figure 2. VSB Master Interface

Note: Master may monitor: CACHE*, IRQ*

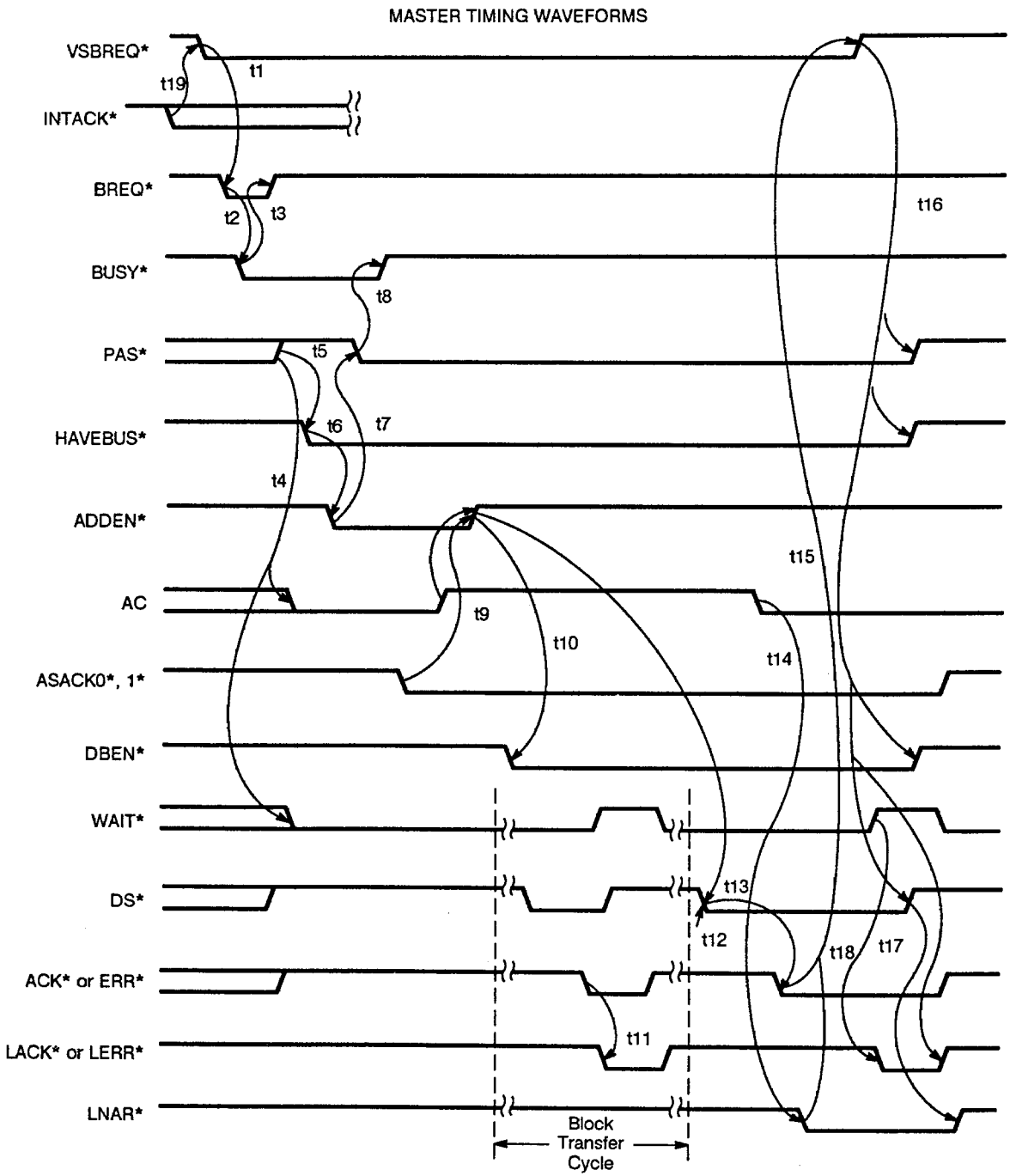


Figure 3. VSB 1400 Timing Diagram

Note: AC, ASACK0*, 1*, ACK* and WAIT* are driven by responding or participating slaves

VSB 1400 Timing Specifications

Timing Parameter	Signals	Max. Time (ns) unless otherwise specified		Description
		C-25, C-35, C-45	M-55, M-65	
t1	VSBREQ* to BR* enable	50, 70, 90	110, 130	
t2	BR* to BUSY* enable	50, 70, 90	110, 130	
t3	BUSY* to BR* release	25, 35, 45	55, 65	
t4	PAS* to WAIT* enable	25, 35, 45	55, 65	
t5	PAS* to HAVEBUS* enable	25, 35, 45	55, 65	
t6	HAVEBUS* to ADDEN* enable	25, 35, 45	55, 65	
t7	ADDEN* to PAS* enable	25, 35, 45	55, 65	Address buffers must have propagation delay of less than 15ns for 25ns PLX device
t8	PAS* to BUSY* release	25, 35, 45	55, 65	
t9	ASACKn* to ADDEN* release	25, 35, 45	55, 65	Participating and idle slaves must enable AC high before ADDEN* is released
t10	ADDEN* to DBEN* enable	25, 35, 45	55, 65	
t11	ACK* or ERR* to LACK* or LERR* enable	25, 35, 45	55, 65	WAIT* must be high
t12	DS* enable	50, 70, 90	110, 130	For DS* to be enabled from ADDEN* edge, WAIT* and LDS* must be low; ACK* and ERR* must be high; data buffers must have propagation delay of less than 15ns for a 25ns PLX device
t13	DS * to ACK* enable	tacc	tacc	Memory access time from slave
t14	AC* to LNAR* enable	25, 35, 45	55, 65	
t15	VSBREQ* release	@ local master	@ local master	ACK* low to release VSBREQ*
t16	VSBREQ* to PAS*, DS*, DBEN*, LACK* (LERR*) and HAVEBUS* release	25, 35, 45	55, 65	Releases at end of cycle
t17	DS* to LNAR* release	25, 35, 45	55, 65	
t18	WAIT* to LACK* or LERR*	25, 35, 45	55, 65	WAIT* must be high before LACK* or LERR* goes low
t19	INTACK* assert to VSBREQ* assert	min 0ns	min 0ns	INTACK* must be asserted before VSBREQ*

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -55°C to +125°C
Supply Voltage to Ground (pin 24 to pins 12, 18, & 20 on DIP) .. -0.5V to +7.0V
DC Voltage to Outputs in High Z State ..... -0.5V to +7.0V

Operating Ranges

	Ambient Temperature	Supply Voltage (V_{CC})
Commercial (C)	0°C to +70°C	5V ± 5%
Industrial (I)	-40°C to +85°C	5V ± 10%
Military (M)	-55°C to +125°C	5V ± 10%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	Output pins I_{OL} = 24mA (Com'l)		0.5	V
			I_{OL} = 24mA (MIL)		0.6	V
			Pins 13, 15, 22, 23 (DIP) I_{OL} = 48mA (Com'l)		0.5	V
			I_{OL} = 48mA (MIL)		0.6	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leakage Current	V_{SS} <= V_{IN} <= V_{CC}, V_{CC} = Max		-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} < = V_{OUT} < = V_{CC}		-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open (Com'l)			80	mA
		V_{CC} = Max, V_{IN} = GND Outputs Open (MIL)			90	mA

Capacitance (sample tested only)

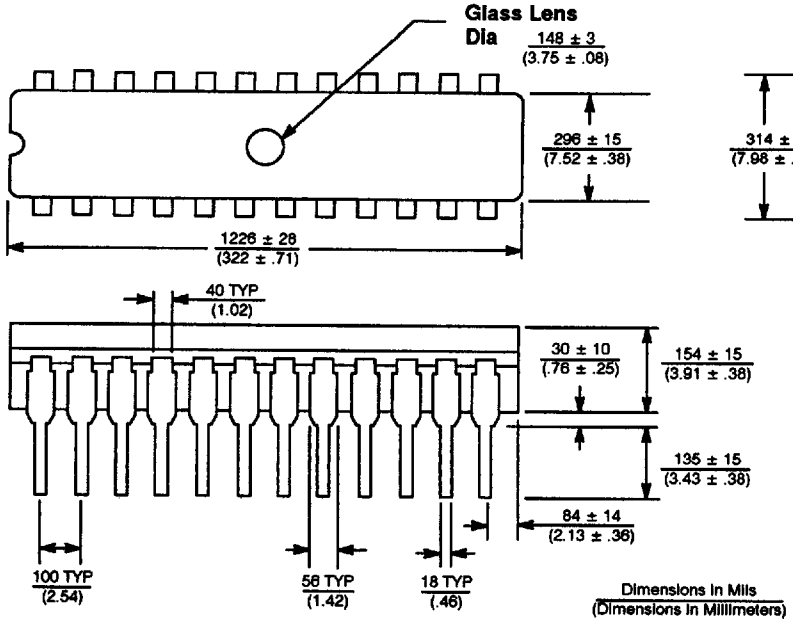
Parameter	Test Conditions	Pins	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1MHz	2-11, 14 (DIP)	5	pF
		13, 15-17, 19, 21-23 (DIP)	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1MHz	13, 15-17, 19, 21-23 (DIP)	10	pF

Packaging Information

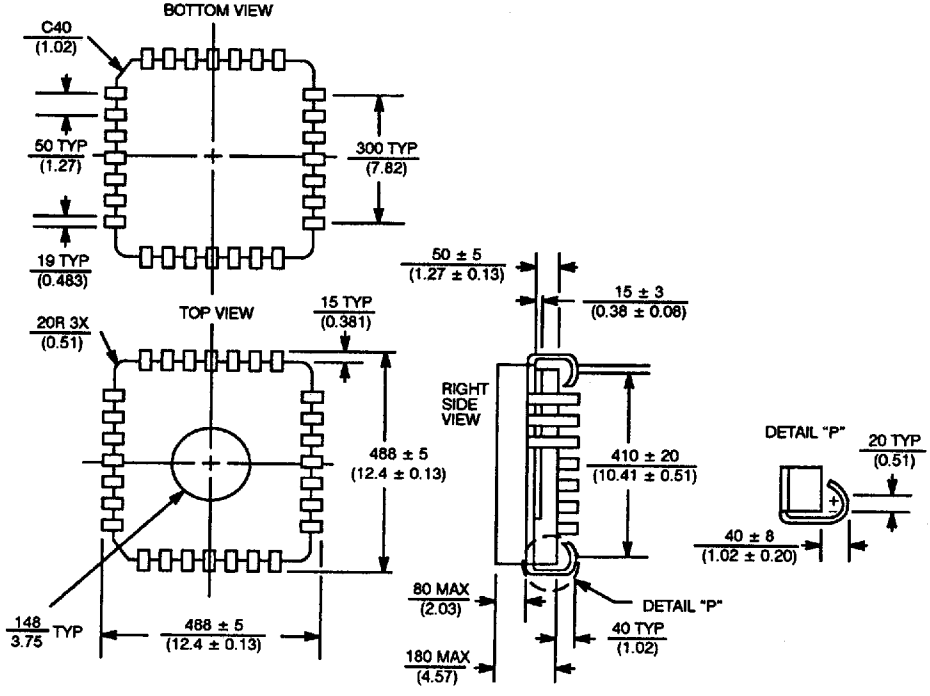
The devices are available in 24 pin slimline DIP (300 mil wide) or 28 pin LCC.

See PLX 448 or PLX 464 January 1989 or later data sheets for package dimensions. Contact PLX for further packaging information.

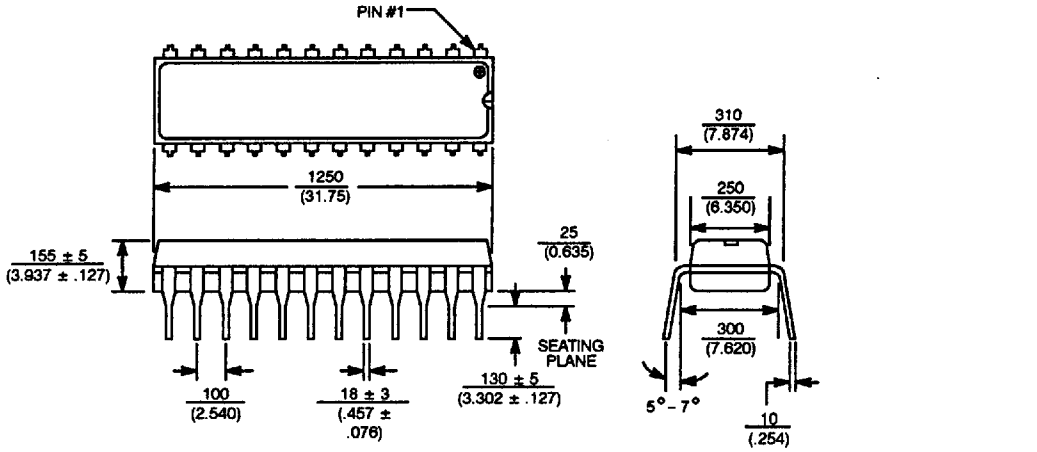
24-Lead Ceramic Dual In-line Package (CERDIP)



28-Pin J Lead Ceramic Chip Carrier



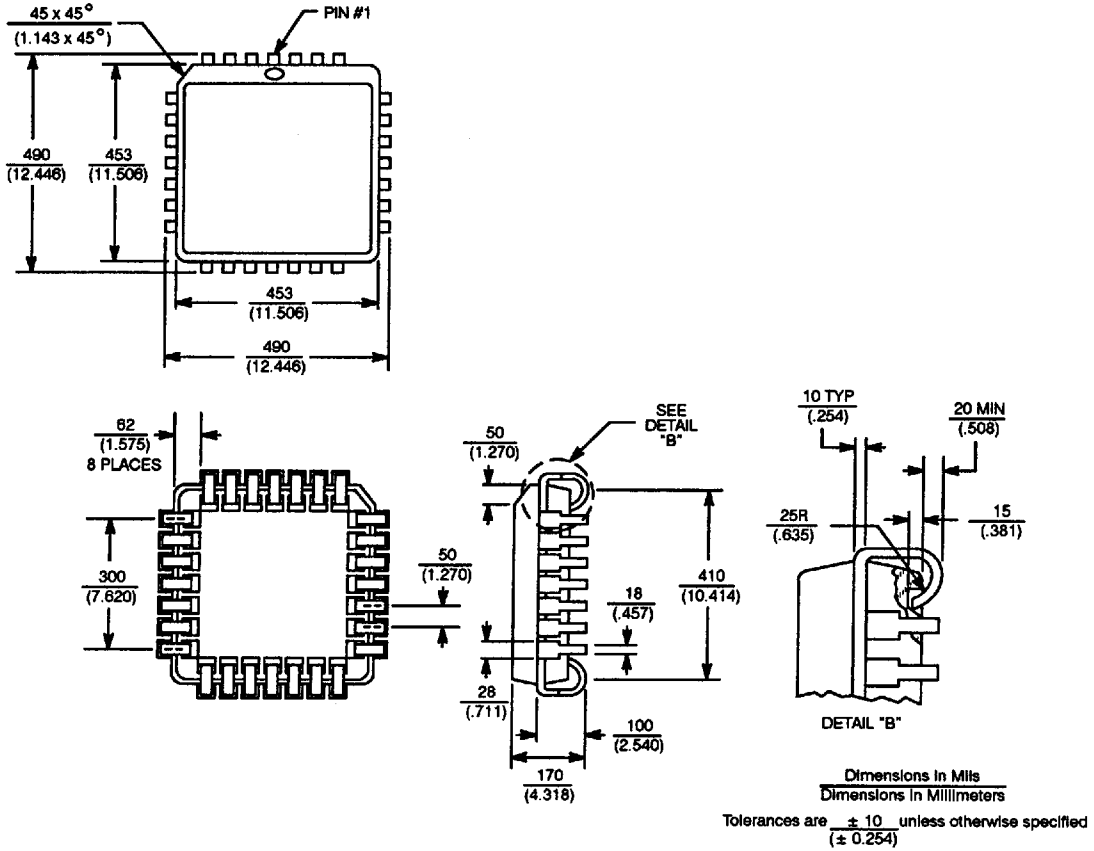
24-Pin DIP Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

28-Pin LCC Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified