REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add five vendors, CAGE 61772, CAGE 04713, CAGE 60991, CAGE 50088, and CAGE 65786. Add 04 new device types. Add case outline letter Y.	1988 JUNE 17	

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	A	A																						
SHEET	22	23																						
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Rick Offner

CHECKED BY: Ray Monnin

APPROVED BY:

DRAWING APPROVAL DATE: 24 JUNE 1986

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS 64K X 1, STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-86015

SHEET 1 OF 23

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E185

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86015	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	see 6.4	64K X 1-bit, SRAM, TS	35 ns
02	see 6.4	64K X 1-bit, SRAM, TS	35 ns (data retention)
03	see 6.4	64K X 1-bit, SRAM, TS	45 ns
04	see 6.4	64K X 1-bit, SRAM, TS	45 ns (data retention)
05	see 6.4	64K X 1-bit, SRAM, TS	55 ns
06	see 6.4	64K X 1-bit, SRAM, TS	55 ns (data retention)
07	see 6.4	64K X 1-bit, SRAM, TS	70 ns
08	see 6.4	64K X 1-bit, SRAM, TS	70 ns (data retention)

1.2.2 Case outlines. The case outlines shall be as follows:

Outline letter	Case outline
X	Figure 1 (22-lead, 1.260" x 0.290" x 0.090"), dual-in-line package
Y	Figure 2 (22-lead, 1.10" x 0.310" x 0.175"), dual-in-line package
Z	Figure 3 (22-terminal, 0.490" x 0.290" x 0.076"), chip carrier package

1.3 Absolute maximum ratings.

Input voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	+15°C/W 1/
Case Y	+30°C/W 1/
Case Z	+60°C/W 1/
Output voltage applied	-0.5 V dc to +7.0 V dc
Output current	50 mA
Maximum power dissipation, (P_D)	1.0 W
Maximum junction temperature (T_J)	+150°C

1/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.

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1.4 Recommended operating conditions.

Supply voltage range	4.5 V dc minimum to 5.5 V dc maximum
Input high voltage	2.2 V dc to V_{CC} +0.5 V
Input low voltage	-0.5 V dc to +0.8 V dc
Fanout current with output high (each)	4.0 mA
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 4.

3.2.2 Truth table. The truth table shall be as specified on figure 5.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 6.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510, 3.1.3.8) shall be subjected to and pass the internal water vapor content test (test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	I_{OH} = -4.0 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V	1, 2, 3	ALL	2.4		V
Low-level output voltage	V_{OL}	I_{OL} = +8.0 mA V_{IL} = 0.8 V, V_{IH} = 2.2. V	1, 2, 3	ALL		0.4	V
High impedance (off-state) output leakage current	I_{OLZ}	$\overline{CS} \geq V_{IH}$, V_{OUT} = 0.0 V V_{CC} = 5.5 V	1, 2, 3	ALL	-10	10	µA
	I_{OHZ}	$\overline{CS} \geq V_{IH}$, V_{OUT} = 5.5 V V_{CC} = 5.5 V	1, 2, 3	ALL	-10	10	µA
High-level input leakage current	I_{IH}	V_{IH} = 5.5 V V_{CC} = 5.5 V	1, 2, 3	ALL	-10	10	µA
Low-level input leakage current	I_{IL}	V_{IL} = 0.0 V V_{CC} = 5.5 V	1, 2, 3	ALL	-10	10	µA
Operating supply current	I_{CC1}	D_{OUT} = open, $\overline{CS}$ = V_{IL} V_{CC} = 5.5 V	1, 2, 3	03,05, 07		105	mA
				01,02, 04,06, 08		90	
DC supply current	I_{CC2}	D_{OUT} = open, $\overline{CS}$ = V_{IL} Minimum read cycle time V_{CC} = 5.5 V	1, 2, 3	03,05, 07		120	mA
				02		70	
				01,04, 06,08		95	
Standby supply current (TTL)	I_{CC3}	$\overline{CS} \geq V_{IH}$ Inputs = 0.8 V or 2.2 V V_{CC} = 5.5 V	1, 2, 3	03,05, 07		50	mA
				01,02, 04,06, 08		35	
Full standby supply current (CMOS)	I_{CC4}	$\overline{CS} \geq V_{CC}$ - 0.2 V, Inputs: $\geq V_{CC}$ - 0.2 V or $\leq$ 0.2 V V_{CC} = 5.5 V	1, 2, 3	ALL		20	mA
Data retention current 4/	I_{CCDR}	V_{DR} = 2.0 V, $\overline{CS} \geq V_{CC}$ - 0.2 V Inputs: $\geq V_{CC}$ - 0.2 V or $\leq$ 0.2 V	1, 2, 3	02,04, 06,08		1	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance	C_{IN}	V_{IN} = 0.0 V V_{CC} = 5.0 V, f = 1 MHz V_{OUT} = 0.0 V (see 4.3.1c) 5/	4	ALL		8	pF
Output capacitance	C_{OUT}			ALL		10	
Data retention voltage 4/	V_{DR}	$\overline{CS}$ = V_{DR} Inputs: $\geq V_{DR}$ - 0.2 V or $\leq$ 0.2 V	1, 2, 3	02,04, 06,08	2.0	5.5	V
Functional tests		See 4.3.1d V_{IL} = 0.0 V, V_{IH} = 3.0 V	7,8	ALL			
Address access time	t_{AVQV}		9, 10, 11	07,08		70	ns
				05,06		55	
				03,04		45	
				01,02		35	
Output hold time	t_{AXQX}		9, 10, 11	All	3		ns
Read cycle time	t_{ELEH}		9, 10, 11	07,08	70		ns
				05,06	55		
				03,04	45		
				01,02	35		
Chip enable access time	t_{ELQV}		9, 10, 11	07,08		70	ns
				05,06		55	
				03,04		45	
				01,02		35	
Chip enable to output active	t_{ELQX}	6/	9, 10, 11	ALL	5		ns
Chip disable to output disable 7/	t_{EHQZ}	6/	9, 10, 11	ALL	0	40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle time	t_{AVAV}		9, 10, 11	07,08	70		ns
				05,06	55		
				03,04	45		
				01,02	35		
Chip enable to end of write	t_{ELWH}		9, 10, 11	05,06, 07,08	55		ns
				03,04	40		
				01,02	30		
Address valid to write high	t_{AVWH}		9, 10, 11	05,06, 07,08	55		ns
				03,04	40		
				01,02	30		
Write high to address don't care	t_{WHAX}		9, 10, 11	ALL	5		ns
Write pulse width	t_{WLEH}		9, 10, 11	01,02	25		ns
				03-08	40		
Address setup to beginning of write	t_{AVWL}		9, 10, 11	01,02	5		ns
				03-08	15		
Data valid to write high	t_{DVWH}		9, 10, 11	01,02	20		ns
				03,04, 05,06	25		
				07,08	30		
Write high to data don't care	t_{WHDX}		9, 10, 11	ALL	5		ns
Write enable to output disable 7/	t_{WLQZ}	6/	9, 10, 11	01,02	0	20	ns
				03-06	0	30	
				07,08	0	35	
Output active after end of write	t_{WHQX}	6/	9, 10, 11	ALL	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address setup before chip enable	t_{AVEL}		9, 10, 11	ALL	5		ns
Chip enable high to address don't care	t_{EHAX}		9, 10, 11	ALL	5		ns
Data valid to chip enable high	t_{DVEH}		9, 10, 11	01,02	20		ns
				03,04, 05,06	25		
				07,08	30		
Chip disable to data retention time 8/	t_{CDR}	4/	9, 10, 11	02,04	45		ns
				06,08	70		
Data retention recovery time 8/	t_R	4/	9, 10, 11	02,04	45		ns
				06,08	70		ns
Chip select to power-up time 8/	t_{PU}		9, 10, 11	ALL		0	ns
Chip deselect to power-down time 8/	t_{PD}		9, 10, 11	01-04	0	45	ns
				05-08	0	70	

1/ Unless otherwise specified, T_C = -55°C to +125°C and V_{CC} = 4.5 V to 5.5 V. All voltages referenced to GND.
2/ AC measurements assume input transition time ≤ 5 ns and input levels are from GND to 3.0 V. Timing reference levels are 1.5 V.
3/ See figure 7 for ac timing waveforms and loading.
4/ Data retention devices only.
5/ Effective capacitance calculated from C = ΔV with ΔV = 3 V and V_{CC} = 5.0 V or measured with a capacitance meter.
6/ Transition to high impedance state is measured ±500 mV from steady state voltage with load specified on figure 7. This parameter is sampled and not 100 percent tested.
7/ Minimum limit not tested and is included for user guidelines.
8/ May not be tested, but shall be guaranteed to the limits specified in table I.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

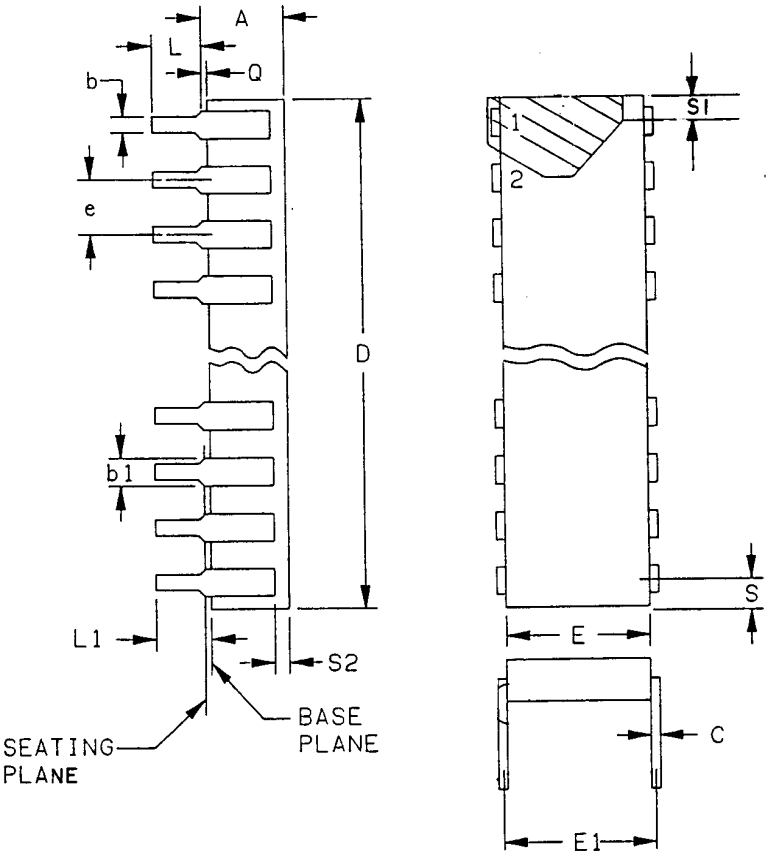
3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

STANDARDIZED MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE	REVISION LEVEL	SHEET
A	A	8

5962-86015

Case X

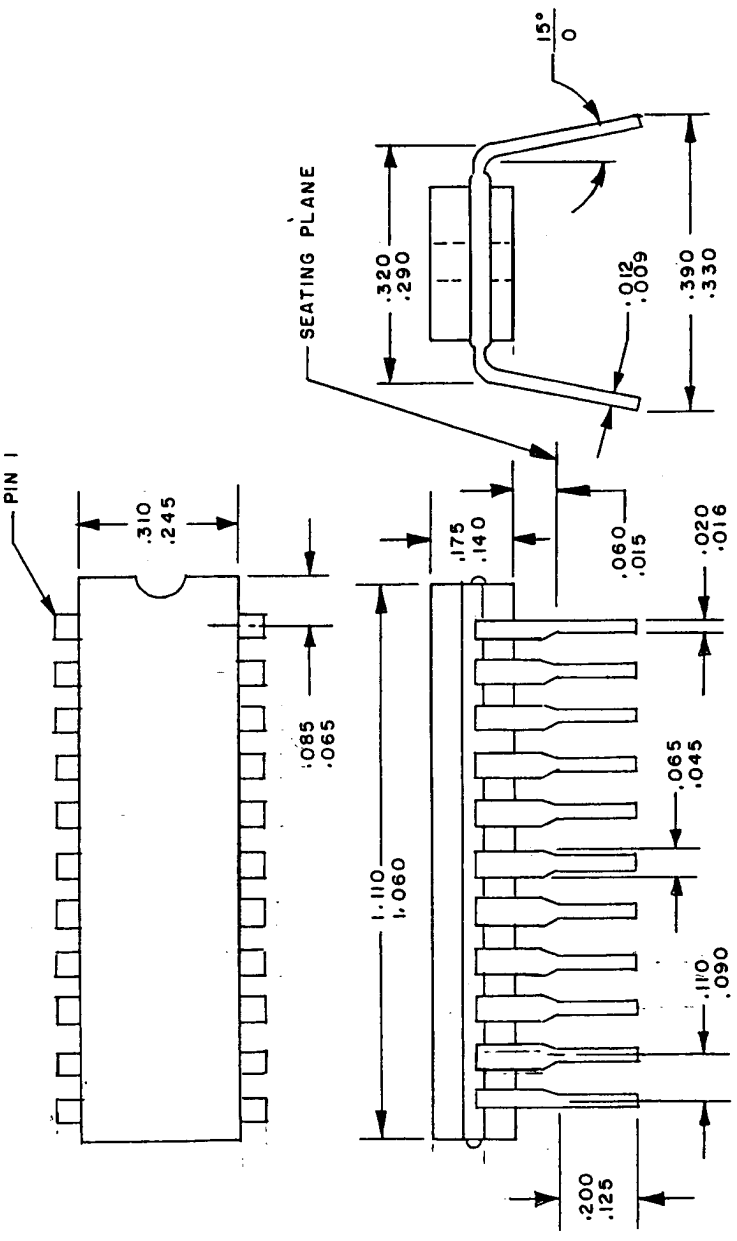


Symbol	Min	Max
A	---	.200
b	.014	.023
b1	.030	.065
c	.008	.015
D	---	1.260
E	.220	.310
E1	.290	.320
e	.100 BSC	
L	.125	.200
L1	.150	---
Q	.015	.060
S	---	.080
S1	.005	---
S2	.005	---
N	22	

Inches	mm
.005	0.13
.008	0.20
.014	0.36
.015	0.38
.023	0.58
.030	0.76
.060	1.52
.080	2.08
.125	3.18
.150	3.81
.200	5.08
.220	5.59
.290	7.37
.310	7.87
.320	8.13
1.260	32.00

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. 22-lead dual-in-line package.



Inches	mm
.009	0.22
.012	0.30
.015	0.38
.016	0.40
.020	0.50
.045	1.14
.060	1.52
.065	1.65
.085	2.15
.090	2.28
.110	2.79
.125	3.17

Inches	mm
.140	3.55
.175	4.44
.200	5.08
.245	6.22
.290	7.36
.310	7.87
.320	8.12
.330	8.38
.390	9.90
1.060	26.92
1.110	28.19

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

CASE Y

FIGURE 2. 22-lead dual-in-line package.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86015
		REVISION LEVEL A	SHEET 9

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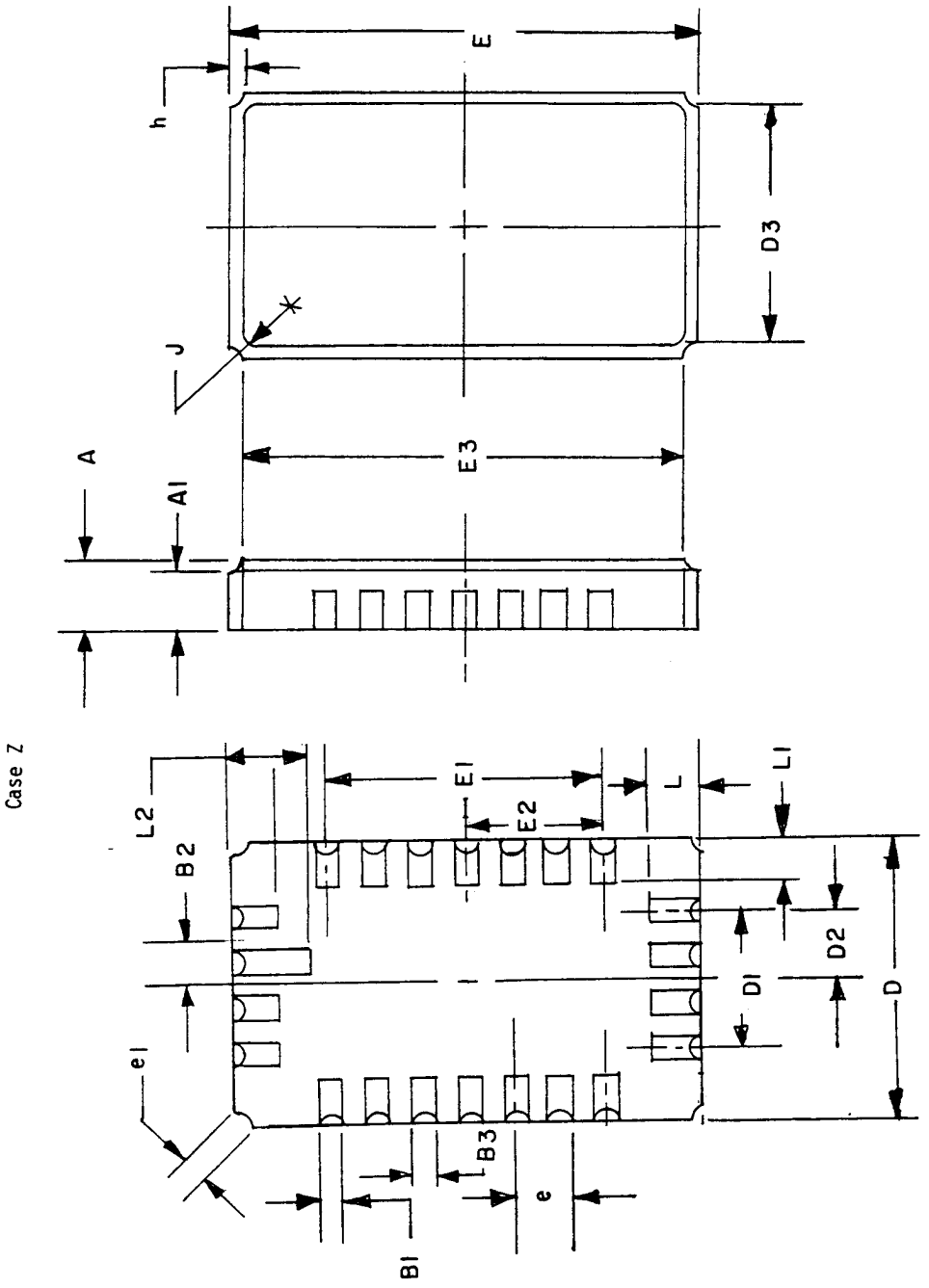

FIGURE 3. 22-terminal chip carrier package.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86015
		REVISION LEVEL A	SHEET 10

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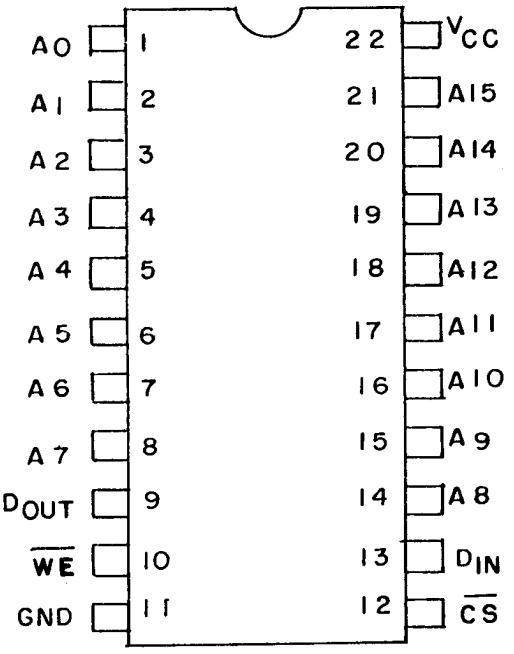
Symbol	Case Z	
	Inches	
	Min	Max
A	.060	.120
A1	.050	.088
B1	.022	.028
B2	.072 REF	
B3	.006	.041
D	.280	.305
D1	.150 BSC	
D2	.075 BSC	
D3	---	.305
E	.480	.496
E1	.300 BSC	
E2	.150 BSC	
E3	---	.496
e	.050 BSC	
e1	.015	---
h	.025 REF	
j	.025 REF	
L	.039	.055
L1	.039	.055
L2	.075	.095
ND	4	
NE	7	
N	22	

Inches	mm
.006	0.15
.015	0.38
.025	0.64
.028	0.71
.039	0.99
.050	1.27
.055	1.40
.060	1.52
.072	1.83
.075	1.91
.088	2.24
.095	2.41
.120	3.05
.150	3.81
.280	7.11
.300	7.62
.305	7.75
.496	12.29
4.00	101.6
7.00	177.8
22.00	558.80

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 3. 22-terminal chip carrier package - Continued.

Cases X and Y



Case Z

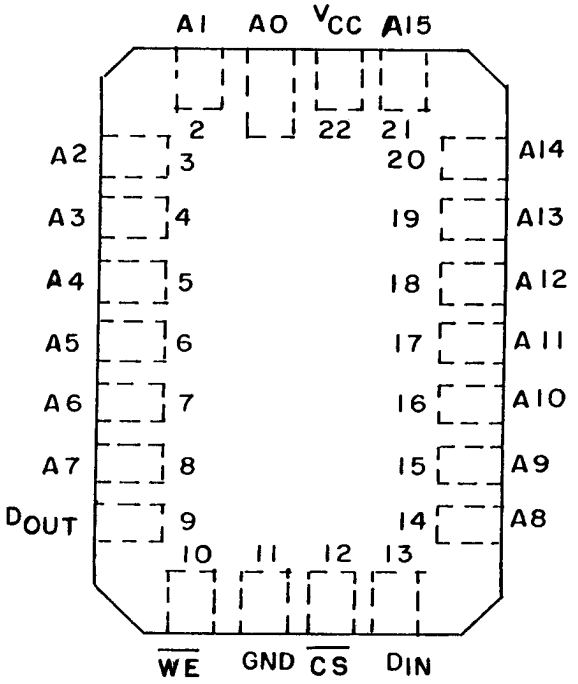


FIGURE 4. Terminal connections.

Mode	$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Power level
Standby	H	X	X	High Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	High Z	Active
Data retention	VDR	Don't	X	High Z	Data retention

High Z = High impedence
D = Valid data bit
X = Don't care

FIGURE 5. Truth table.

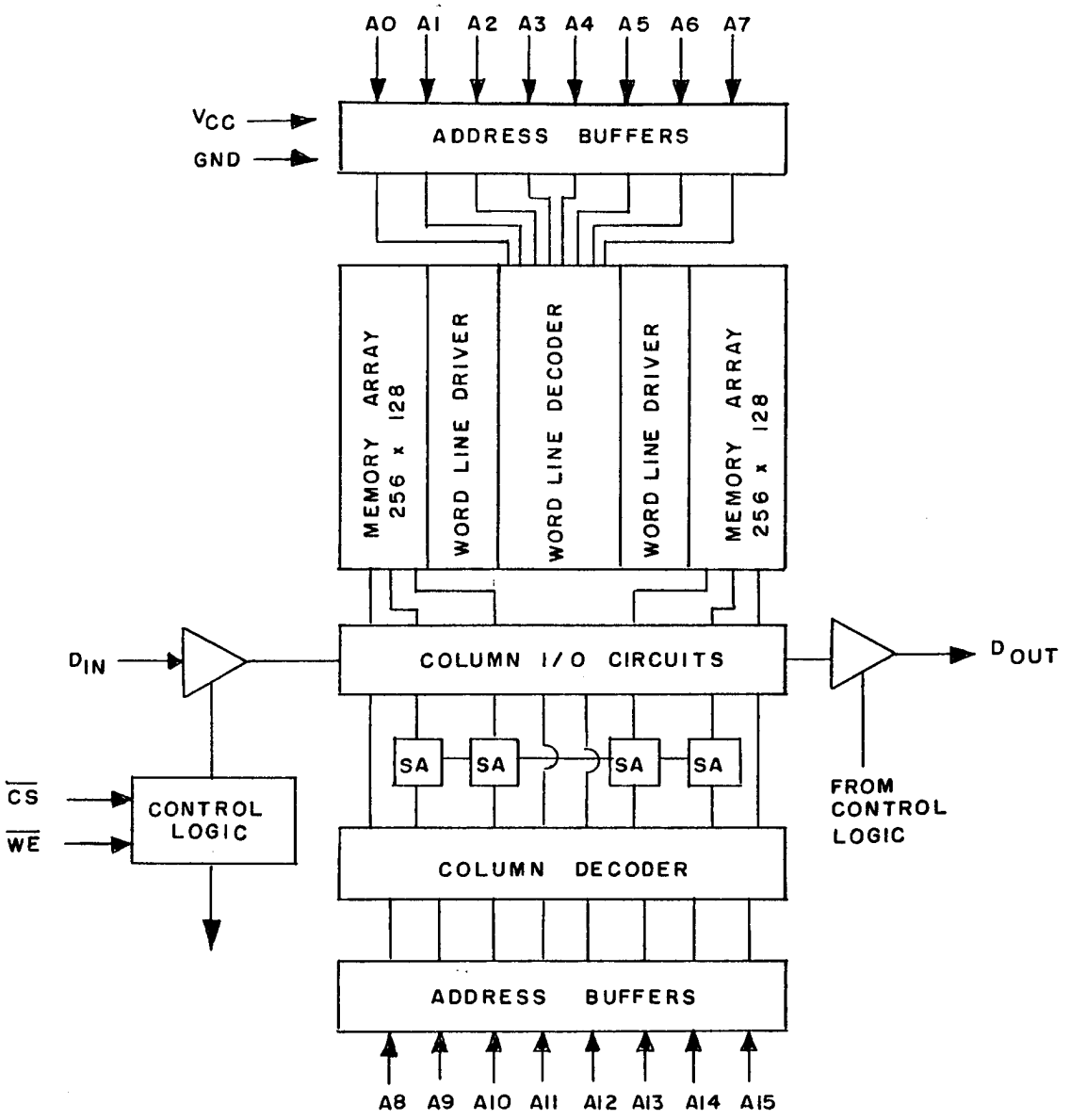


FIGURE 6. Functional block diagram.

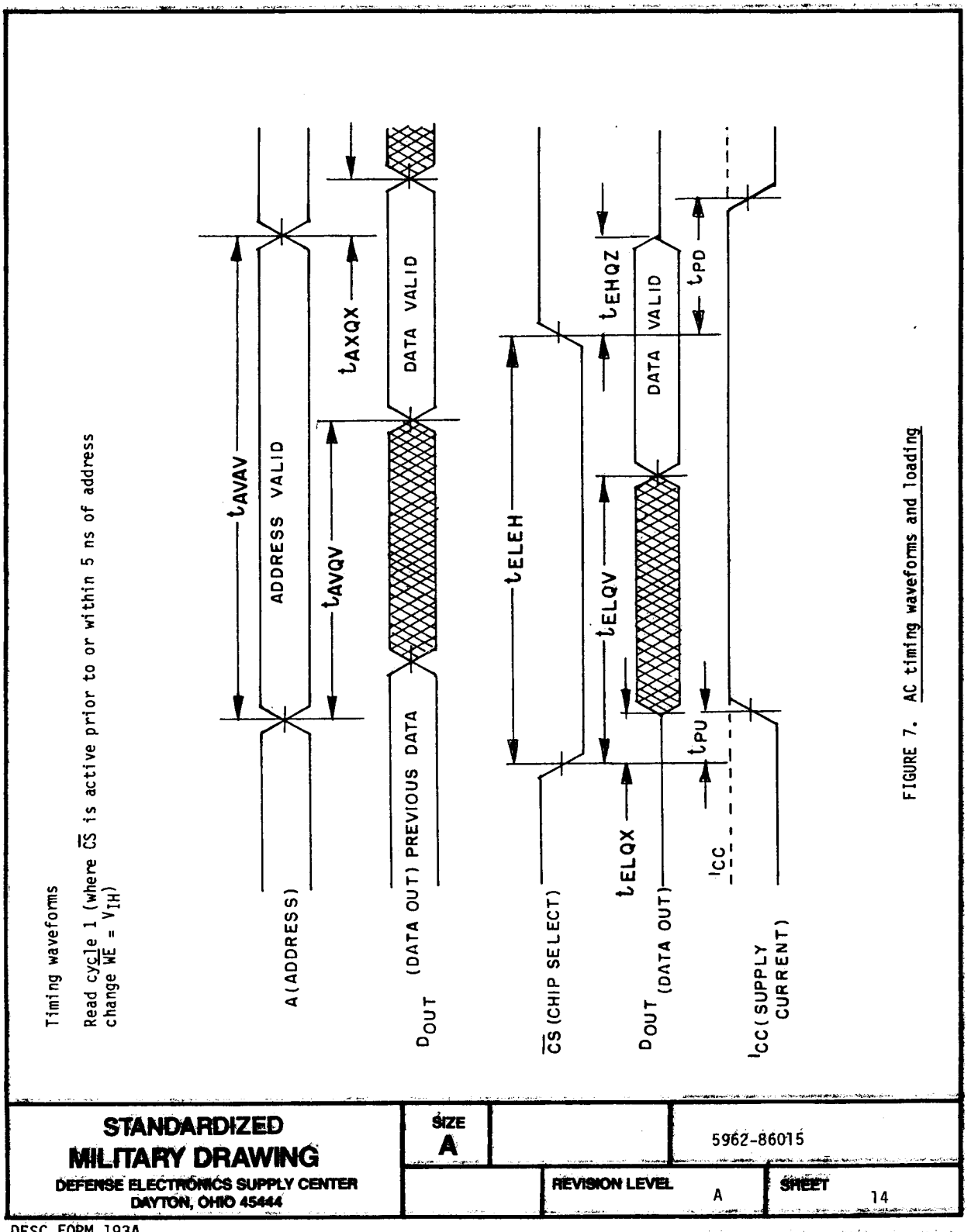


FIGURE 7. AC timing waveforms and loading

Write cycle 1. This write cycle is $\overline{WE}$ controlled, where $\overline{CS}$ is active (LOW) prior to $\overline{WE}$ becoming active (LOW). In this write cycle the data out may become active, requiring observance of t_{WLQZ} to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{WE}$ becomes inactive (HIGH) prior to $\overline{CS}$ becoming inactive (HIGH).

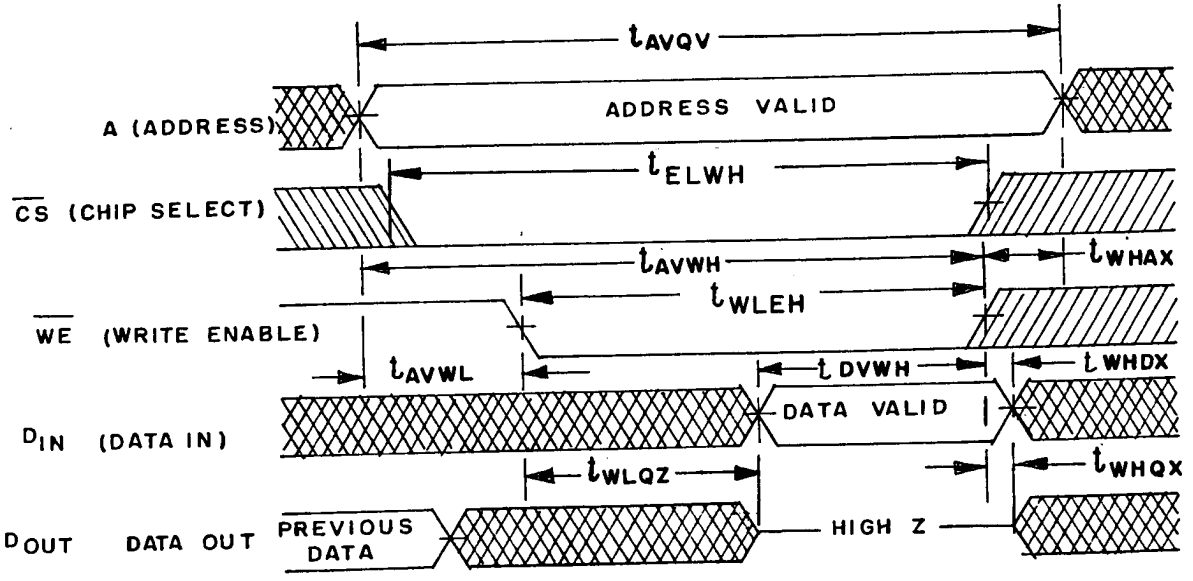


FIGURE 7. Ac timing waveforms and loading - Continued.

Write cycle 2. This write cycle is $\overline{CS}$ controlled, where $\overline{WE}$ is active (LOW) prior to, or coincident with, $\overline{CS}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (3 state) at the begininning of the write cycle, precluding potential data contention in common I/O applications.

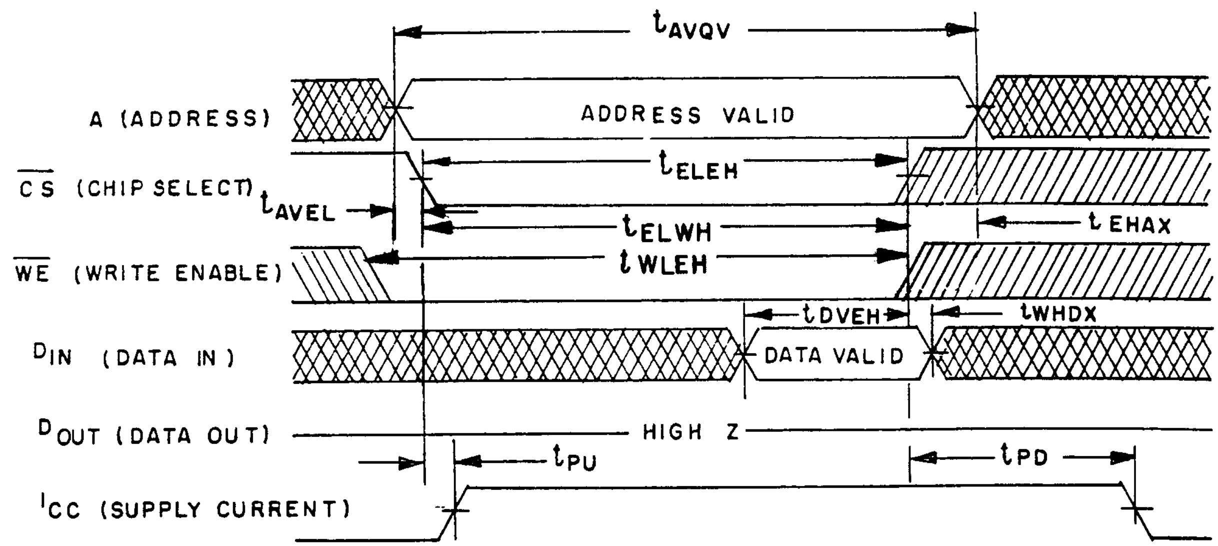


FIGURE 7. Ac timing waveforms and loading - Continued.

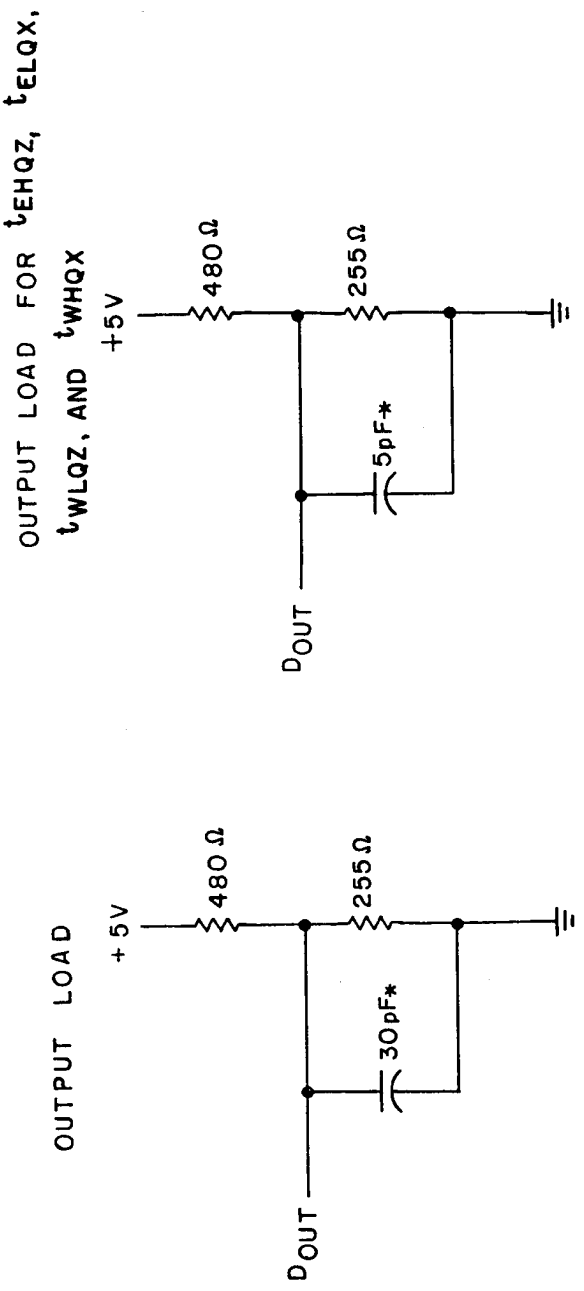


FIGURE 7. Ac timing waveforms and loading - Continued.

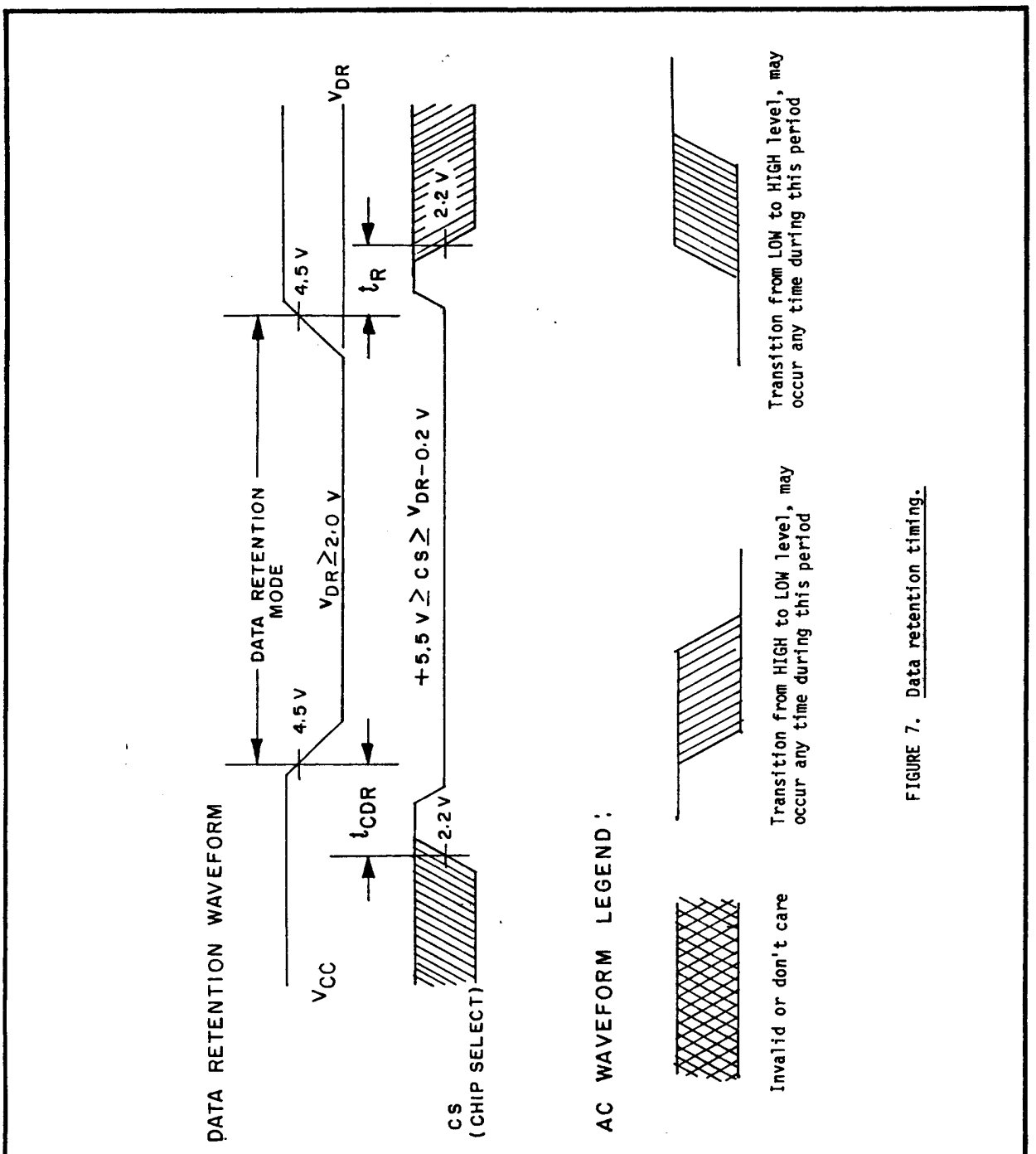


FIGURE 7. Data retention timing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test conditions C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8

* PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 test sufficient to verify the truth table of figure 5.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test conditions C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/29201BXX.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8601501XX	07263 04713	F1600DMQB35 6287-35/BXAJC	
5962-8601501YX	65786	CY7C187-35DMB	
5962-8601501ZX	07263 65786 04713	F1600-35LMQ35 CY7C187-35LMB 6287-35M/BUAJC	
5962-8601502XX	07263 50088 04713	F1601DMQB35 MKX 41H87P835 6287-35/BXAJC	
5962-8601502YX	65786 50088	CY7C187L-35DMB MKX 41H87J835	
5962-8601502ZX	65786 07263 50088 04713	CY7C187L-35LMB F1601-35LMQB35 MKX 41H87E835 6287-35M/BUAJC	
5962-8601503XX	07263 60991 61772 04713	F1600DMQB45 IMS1600S-45M IDT7187S45DB 6287-45/BXAJC	
5962-8601503YX	65786	CY7C187-45DMB	
5962-8601503ZX	07263 65786 61772 04713 60991	F1600LMQB45 CY7C187-45LMB IDT7187S45LB 6287-45M/BUAJC IMS1600N-45M	M38510/29202BUX

See footnote at end of table.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8601504XX	07263 50088 61772 04713	F1601DMQB45 MKX 41H87P845 IDT7187L45DB 6287-45/BXAJC	
5962-8601504YX	65786 50088	CY7C187L-45DMB MKX 41H87J845	
5962-8601504ZX	65786 50088 07263 61772 04713	CY7C187L-45LMB MKX 41H87E845 F1601LMQB45 IDT7187L45LB 6287-45M/BUAJC	
5962-8601505XX	07263 61772 60991	F1600DMQB55 IDT7187S55DB IMS1600S-55M	
5962-8601505ZX	07263 61772 60991	F1600LMQB5 IDT7187S55LB IMS1600N-55M	M38510/29201BUX
5962-8601506XX	07263 61772 60991 50088	F1601DMQB55 IDT7187L55DB IMS1601S-55LM MKX 41H87P855	
5962-8601506YX	50088	MKX 41H87J855	
5962-8601506ZX	07263 61772 60991 50088	F1601LMQB55 IDT7187L55LB IMS1601N-55LM MKX 41H87E855	M38510/29203BUX
5962-8601507XX	60991 61772	IMS1600S-70M IDT7187S70DB	
5962-8601507ZX	60991 61772	IMS1600N-70M IDT7187S70LB	

See footnotes at end of table.

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Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8601508XX	60991 61772	IMS1601S-70LM IDT7187L70DB	
5962-8601508ZX	60991 61772	IMS1601N-70LM IDT7187L70LB	M38510/29204BUX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
04713	Motorola, Incorporated 7402 S. Price Road Tempe, AZ 85283
07263	Fairchild Semiconductor Corporation P. O. Box 5000 Puyallup, WA 98373-0900
50088	SGS-Thomson Microelectronics 1310 Electronics Drive Carrollton, TX 75006
60991	INMOS Corporation P.O. Box 16000 Colorado Springs, CO 80935-6000
61772	Integrated Device Technology Static Ram Division 1566 Moffet Street Salinas, CA 93905
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134