ADC1113D125

Dual 11-bit ADC; serial JESD204A interface

Rev. 02 — 23 April 2010 Preliminary data sheet

1. General description

The ADC1113D125 is a dual-channel 11-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performances and low power at sample rates of 125 Msps. Pipelined architecture and output error correction ensure the ADC1113D125 is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a 3 V source for analog and a 1.8 V source for the output driver, it embeds two serial outputs. Each lane is differential and complies with the JESD204A format. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC. A set of IC configurations is also available via the binary level control pins taken, which are used at power-up. The device also includes a SPI programmable full-scale to allow flexible input voltage range from 1 V to 2 V (peak-to-peak).

Excellent dynamic performance is maintained from the baseband to input frequencies of 170 MHz or more, making the ADC1113D125 ideal for use in communications, imaging, and medical applications.

2. Features and benefits

- SNR, 66.5 dBFS; SFDR, 86 dBc
- Sample rate: 125 Msps
- Clock input divider by 2 for less jitter contribution
- 3 V, 1.8 V single supplies
- Flexible input voltage range: 1 V to 2 V (peak-to-peak)
- Two configurable serial outputs
- INL ± 1.25 LSB; DNL ± 0.25 LSB
- Pin compatible with the ADC1213D series
- HVQFN56 package
- Input bandwidth, 600 MHz
- Power dissipation, 1270 mW
- SPI register programming
- Duty cycle stabilizer
- High IF capability
- Offset binary, two's complement, gray code
- Power-down mode and Sleep mode
- Two JESD204A serial outputs

3. Applications

- Wireless and wired broadband communications
- Spectral analysis
- Ultrasound equipment
- Portable instrumentation
- Imaging systems
- Software defined radio

4. Ordering information

Table 1. Ordering information

Type number	Sampling frequency (Msps)	Package		
		Name	Description	Version
ADC1113D125HN/C1	125	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-7

5. Block diagram

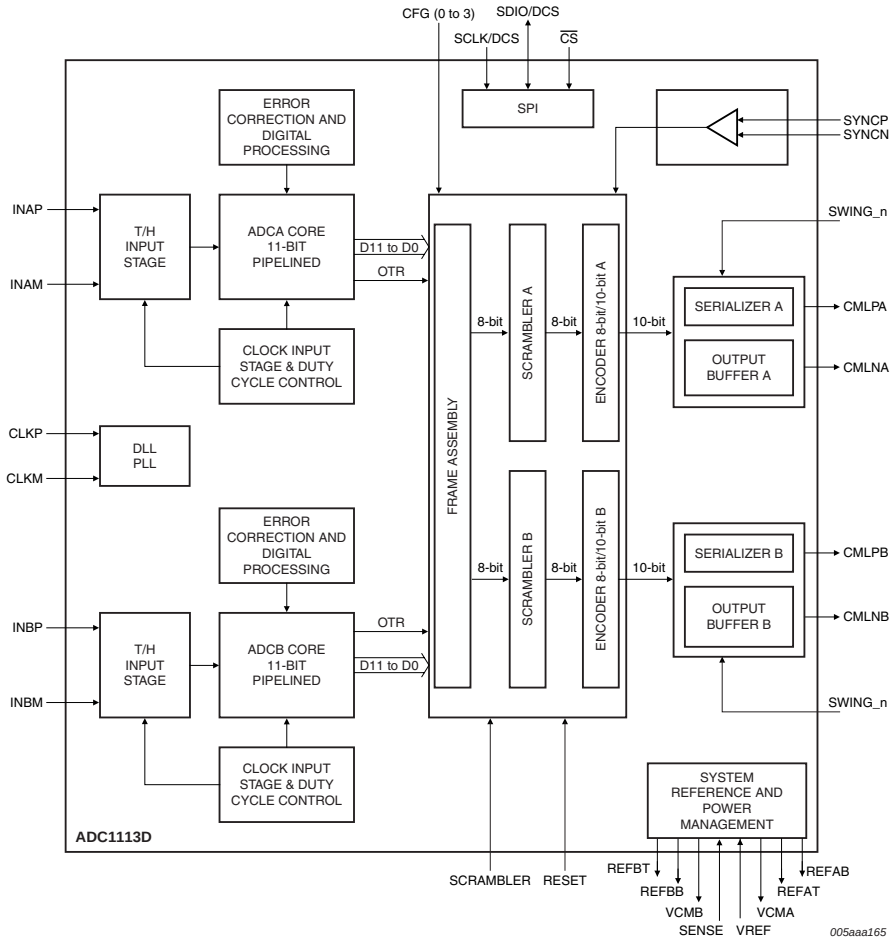


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

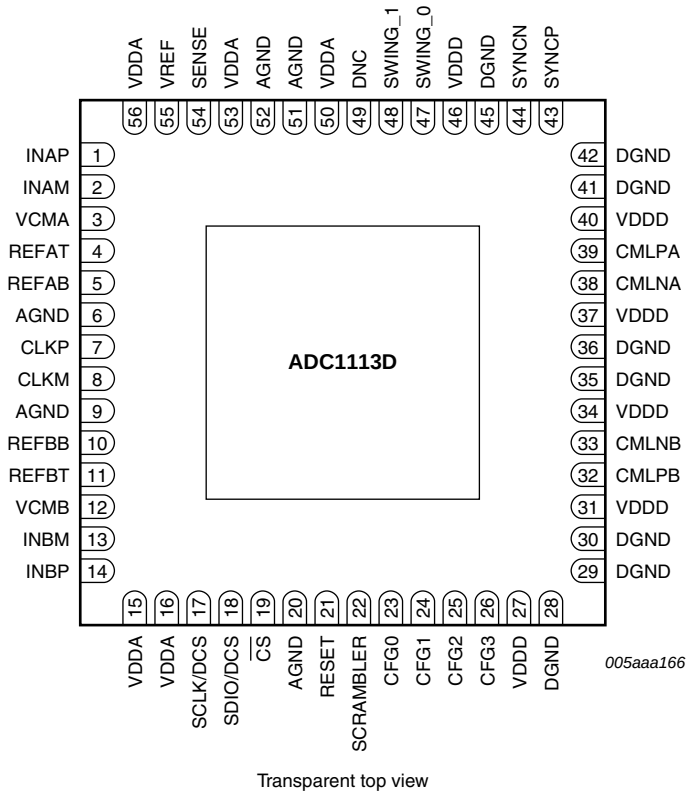


Fig 2. Pinning diagram

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
INAP	1	I	channel A analog input
INAM	2	I	channel A complementary analog input
VCMA	3	O	channel A output common voltage
REFAT	4	O	channel A top reference
REFAB	5	O	channel A bottom reference
AGND	6	G	analog ground
CLKP	7	I	clock input
CLKM	8	I	complementary clock input
AGND	9	G	analog ground
REFBB	10	O	channel B bottom reference
REFBT	11	O	channel B top reference
VCMB	12	O	channel B output common voltage
INBM	13	I	channel B complementary analog input

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
INBP	14	I	channel B analog input
VDDA	15	P	analog power supply 3 V
VDDA	16	P	analog power supply 3 V
SCLK/DCS	17	I	SPI clock data format select
SDIO/DCS	18	I/O	SPI data IO duty cycle stabilizer
$\overline{CS}$	19	I	chip select bar
AGND	20	G	analog ground
RESET	21	I	JEDEC digital IP reset
SCRAMBLER	22	I	scrambler enable and disable
CFG0	23	I/O	see Table 28 (input) or OTRA (output)[2]
CFG1	24	I/O	see Table 28 (input) or OTRB (output)[2]
CFG2	25	I/O	see Table 28 (input)
CFG3	26	I/O	see Table 28 (input)
VDDD	27	P	digital power supply 1.8 V
DGND	28	G	digital ground
DGND	29	G	digital ground
DGND	30	G	digital ground
VDDD	31	P	digital power supply 1.8 V
CMLPB	32	O	channel B output
CMLNB	33	O	channel B complementary output
VDDD	34	P	digital power supply 1.8 V
DGND	35	G	digital ground
DGND	36	G	digital ground
VDDD	37	P	digital power supply 1.8 V
CMLNA	38	O	channel A complementary output
CMLPA	39	O	channel A output
VDDD	40	P	digital power supply 1.8 V
DGND	41	G	digital ground
DGND	42	G	digital ground
SYNCP	43	I	synchronization from FPGA
SYNCN	44	I	synchronization from FPGA
DGND	45	G	digital ground
VDDD	46	P	digital power supply 1.8 V
SWING_0	47	I	JESD204 serial buffer programmable output swing
SWING_1	48	I	JESD204 serial buffer programmable output swing
DNC	49	O	Do not connect
VDDA	50	P	analog power supply 3 V
AGND	51	G	analog ground
AGND	52	G	analog ground
VDDA	53	P	analog power supply 3 V

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
SENSE	54	I	reference programming pin
VREF	55	I/O	voltage reference input/output
VDDA	56	P	analog power supply 3 V

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

[2] OTRA stands for “OuT of Range” A. OTRB stands for “OuT of Range” B.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA}	analog supply voltage		[1]	–0.4	+4.6	V
V_{DDD}	digital supply voltage		[2]	–0.4	+2.5	V
ΔV_{CC}	supply voltage difference	$V_{DDA} - V_{DDD}$		<tbd>	<tbd>	V
T_{stg}	storage temperature			–55	+125	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			-	125	°C

[1] The supply voltage V_{DDA} may have any value between –0.5 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

[2] The supply voltage V_{DDD} may have any value between –0.5 V and +5.0 V provided that the supply voltage differences ΔV_{CC} are respected.

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	17.8	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	6.8	K/W

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

9. Static characteristics

Table 5. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		2.85	3.0	3.4	V
V_{DDD}	digital supply voltage		1.65	1.8	1.95	V
I_{DDA}	analog supply current	f_{clk} = 125 Msps; f_i =70 MHz	-	343	-	mA
I_{DDD}	digital supply current	f_{clk} = 125 Msps; f_i = 70 MHz	-	150	-	mA
P_{tot}	total power dissipation	f_{clk} = 125 Msps	-	1270	-	mW
P	power dissipation	power-down mode	-	30	-	mW
		standby mode	-	200	-	mW
Digital inputs						
Clock inputs: pins CLKP and CLKM, AC coupled						
LVPECL						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	±0.8	-	V
LVDS						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	±0.4	-	V
SINE wave						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	±0.4	±1.5	-	V
LVCMOS mode						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	-	V
Logic inputs, Power-down: pins CFG0 to CFG3, SCRAMBLER, SWING_0, and SWING_1						
V_{IL}	LOW-level input voltage		-	0	-	V
V_{IH}	HIGH-level input voltage		-	$0.66V_{DDD}$	-	V
I_{IL}	LOW-level input current		–6	-	+6	µA
I_{IH}	HIGH-level input current		–30	-	+30	µA
SPI: pins $\overline{CS}$, SDIO/DCS, and SCLK/DCS						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDA}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	V_{DDA}	V
I_{IL}	LOW-level input current		–10	-	+10	µA
I_{IH}	HIGH-level input current		–50	-	+50	µA
C_I	input capacitance		-	4	-	pF

Table 5. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog inputs: pins INAP, INAM, INBP, and INBM						
I_I	input current	track mode	–5	-	+5	μA
R_I	input resistance	track mode	-	15	-	Ω
C_I	input capacitance	track mode	-	5	-	pF
$V_{I(cm)}$	common-mode input voltage	track mode	0.9	1.5	2	V
B_i	input bandwidth		-	600	-	MHz
$V_{I(dif)}$	differential input voltage	peak-to-peak	1	-	2	V
Voltage controlled regulator output: pins VCMA and VCMB						
$V_{O(cm)}$	common-mode output voltage		-	$0.5V_{DDA}$	-	V
$I_{O(cm)}$	common-mode output current		-	<tbd>	-	μA
Reference voltage input/output: pin VREF						
V_{VREF}	voltage on pin VREF	output	0.5	-	1	V
		input	0.5	-	1	V
Data outputs: CMLPA, CMLNA						
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 000						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.5	-	V
		AC coupled	-	1.65	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.35	-	V
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 001						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.45	-	V
		AC coupled	-	1.625	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.275	-	V
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 010						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.4	-	V
		AC coupled	-	1.6	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.2	-	V
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 011						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.35	-	V
		AC coupled	-	1.575	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.125	-	V
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 100						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.3	-	V
		AC coupled	-	1.55	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.05	-	V

Table 5. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial configuration: SYNCCP, SYNCCN						
V_{IL}	LOW-level input voltage	differential; input	-	0.95	-	V
V_{IH}	High-level input voltage	differential; input	-	1.47	-	V
Accuracy						
INL	integral non-linearity		–5	±1.25	+5	LSB
DNL	differential non-linearity	no missing codes guaranteed	–0.95	±0.25	+0.95	LSB
E_{offset}	offset error		-	±2	-	mV
E_G	gain error	full-scale	-	± 0.5	-	%
$M_{G(CTC)}$	channel-to-channel gain matching		-	<tbd>	-	%
Supply						
PSRR	power supply rejection ratio	100 mV (p-p) on VDDA	-	35	-	dBc

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = –40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) – V_I (INAM, INBM) = –1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

10. Dynamic characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog signal processing						
α_{2H}	second harmonic level	f_i = 3 MHz	-	88	-	dBc
		f_i = 30 MHz	-	87	-	dBc
		f_i = 70 MHz	-	85	-	dBc
		f_i = 170 MHz	-	83	-	dBc
α_{3H}	third harmonic level	f_i = 3 MHz	-	87	-	dBc
		f_i = 30 MHz	-	86	-	dBc
		f_i = 70 MHz	-	84	-	dBc
		f_i = 170 MHz	-	82	-	dBc
THD	total harmonic distortion	f_i = 3 MHz	-	86	-	dBc
		f_i = 30 MHz	-	85	-	dBc
		f_i = 70 MHz	-	83	-	dBc
		f_i = 170 MHz	-	81	-	dBc
ENOB	effective number of bits	f_i = 3 MHz	-	10.7	-	bits
		f_i = 30 MHz	-	10.7	-	bits
		f_i = 70 MHz	-	10.7	-	bits
		f_i = 170 MHz	-	10.6	-	bits
SNR	signal-to-noise ratio	f_i = 3 MHz	-	66.2	-	dBFS
		f_i = 30 MHz	-	66.2	-	dBFS
		f_i = 70 MHz	-	66.0	-	dBFS
		f_i = 170 MHz	-	65.8	-	dBFS
SFDR	spurious-free dynamic range	f_i = 3 MHz	-	87	-	dBc
		f_i = 30 MHz	-	86	-	dBc
		f_i = 70 MHz	-	84	-	dBc
		f_i = 170 MHz	-	82	-	dBc
IMD	intermodulation distortion	f_i = 3 MHz	-	89	-	dBc
		f_i = 30 MHz	-	88	-	dBc
		f_i = 70 MHz	-	86	-	dBc
		f_i = 170 MHz	-	84	-	dBc
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 70 MHz	-	100	-	dBc

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) − V_I (INAM, INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

11. Clock and digital output timing

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock timing input: pins CLKP and CLKM						
f_{clk}	clock frequency		100	-	125	Msps
$t_{lat(data)}$	data latency time		-	14	-	clock cycle
δ_{clk}	clock duty cycle	DCS_EN = 1: en	30	50	70	%
		DCS_EN = 0: dis	45	50	55	%
$t_{d(s)}$	sampling delay time		-	0.8	-	ns
t_{wake}	wake-up time		-	<tbd>	-	ns

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) − V_I (INAM, INBM) = −1 dBFS; internal reference mode; 100 W differential applied to serial outputs; unless otherwise specified.

11.1 Serial output timings

The eye diagram of the serial output is shown in Figure 3 and Figure 4. Test conditions are:

- 3.125 Gbps data rate
- T_{amb} = 25 °C
- DC coupling with two different receiver common-mode voltages

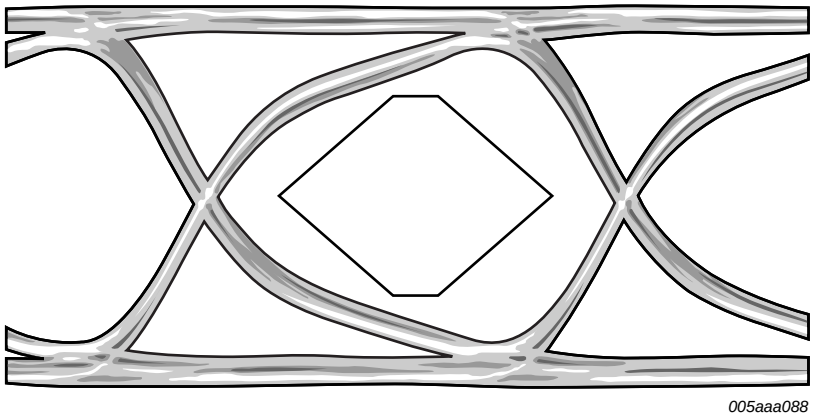


Fig 3. Eye diagram at 1 V receiver common-mode

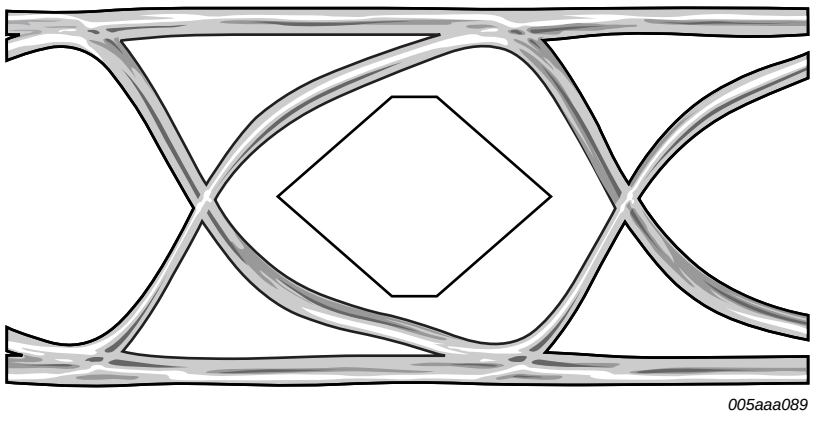


Fig 4. Eye diagram at 2 V receiver common-mode

12. SPI timing

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial Peripheral Interface timings						
$t_{w(SCLK)}$	SCLK pulse width		40	-	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		16	-	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		16	-	-	ns
t_{su}	set-up time	data to SCLKH	5	-	-	ns
		$\overline{CS}$ to SCLKH	5	-	-	ns
t_h	hold time	data to SCLKH	2	-	-	ns
		$\overline{CS}$ to SCLKH	2	-	-	ns
$f_{clk(max)}$	maximum clock frequency		-	-	25	MHz

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C and C_L = 5 pF. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) − V_I (INAM,INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

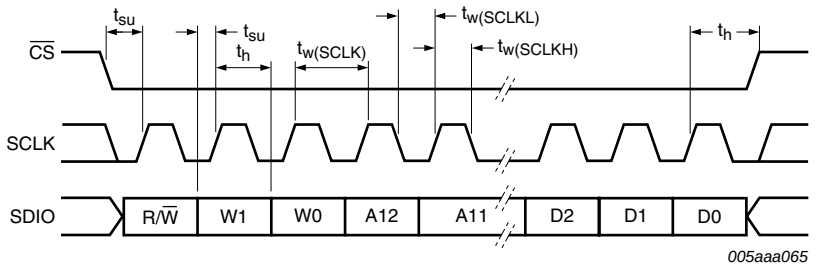


Fig 5. SPI timings

13. Application information

13.1 Analog inputs

13.1.1 Input stage description

The analog input of the ADC1113D125 supports differential or single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM set to 0.5VDDA.

The full scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 13.2 and Table 21 for further details).

Figure 6 shows the equivalent circuit of the sample and hold input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics.

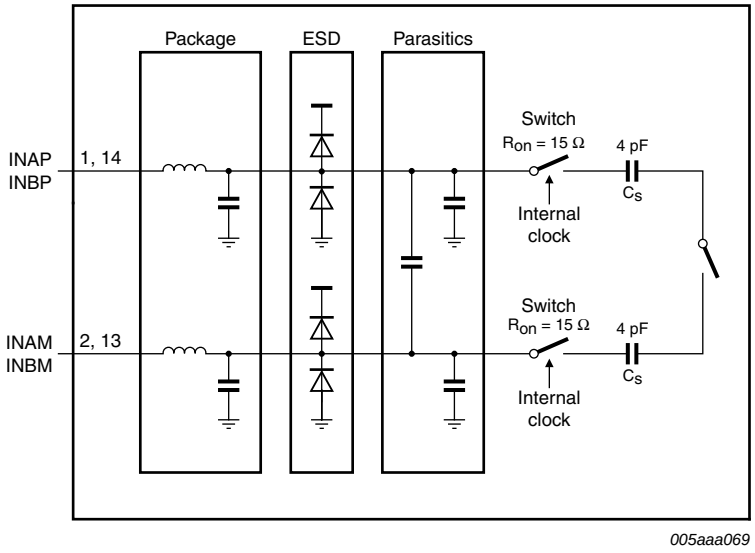


Fig 6. Input sampling circuit

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

13.1.2 Anti-kickback circuitry

Anti-kickback circuitry (R-C filter in Figure 7) is needed to counteract the effects of a charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

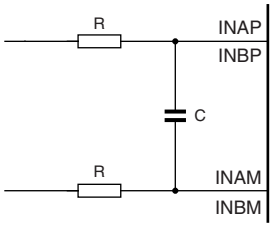


Fig 7. Anti-kickback circuit

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

Table 9. RC coupling versus input frequency - typical values

Input frequency	R	C
3 MHz	25 Ω	12 pF
70 MHz	12 Ω	8 pF
170 MHz	12 Ω	8 pF

13.1.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 8 would be suitable for a baseband application.

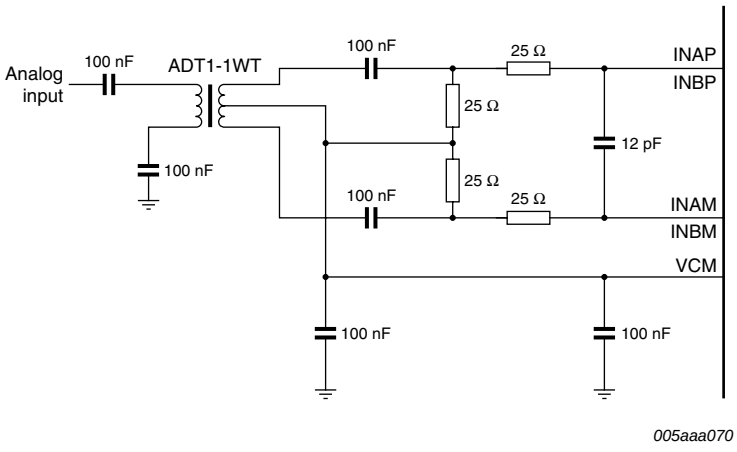


Fig 8. Single transformer configuration

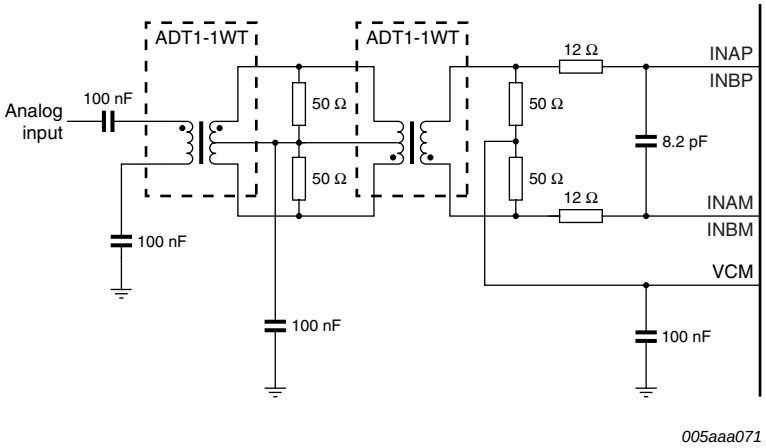


Fig 9. Dual transformer configuration

The configuration shown in Figure 9 is recommended for high frequency applications. In both cases, the choice of transformer will be a compromise between cost and performance.

13.2 System reference and power management

13.2.1 Internal/external reference

The ADC1113D125 has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF an SENSE (see Figure 11, Figure 12, Figure 13 and Figure 14), in 1 dB steps between 0 dB and −6 dB, via SPI control bits INTREF[2:0] (when bit INTREF_EN = 1; see Table 21). The equivalent reference circuit is shown in Figure 10. External reference is also possible by providing a voltage on pin VREF as described in Figure 13.

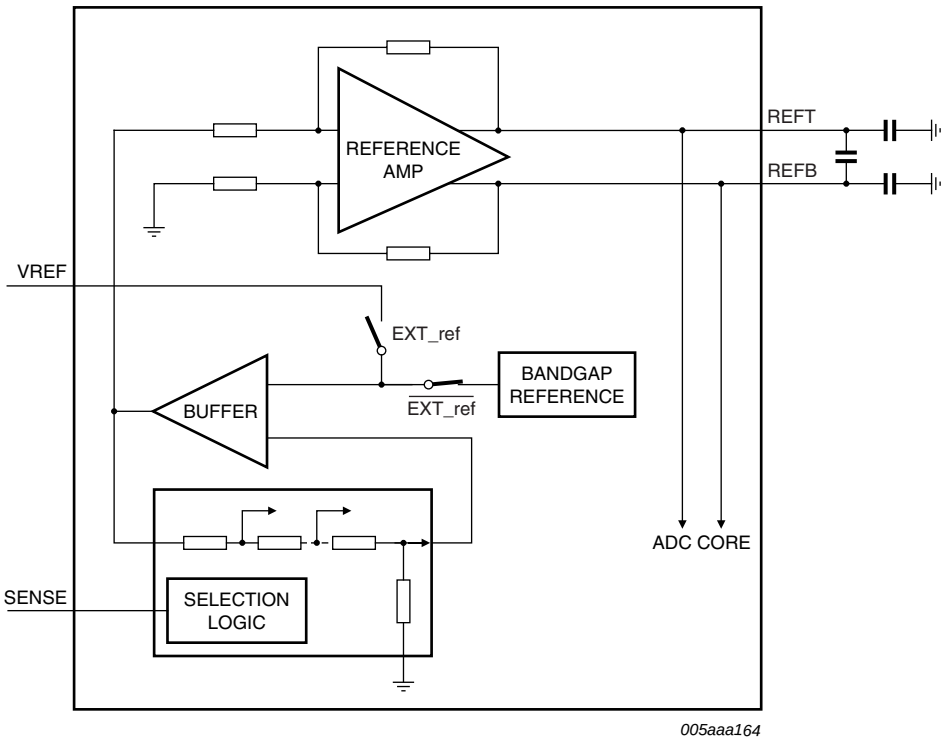


Fig 10. Reference equivalent schematic

Table 10 shows how to choose between the different internal/external modes:

Table 10. Reference modes

Mode	SPI Bit, "Internal reference"	SENSE pin	VREF pin	Full Scale, V (p-p)
Internal (Figure 11)	0	GND	330 pF capacitor to GND	2
Internal (Figure 12)	0	VREF pin = SENSE pin and 330 pF capacitor to GND		1
External (Figure 13)	0	V_{DDA}	External voltage from 0.5 V to 1 V	1 to 2
Internal, SPI mode (Figure 14)	1	VREF pin = SENSE pin and 330 pF capacitor to GND		1 to 2

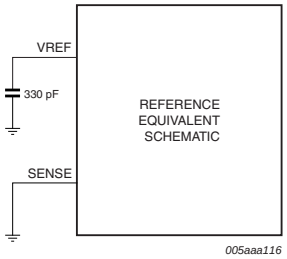


Fig 11. Internal reference, 2 V (p-p) full scale

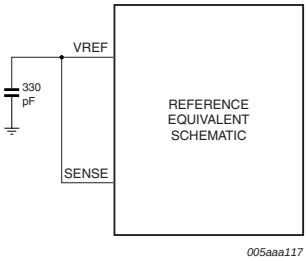


Fig 12. Internal reference, 1 V (p-p) full scale

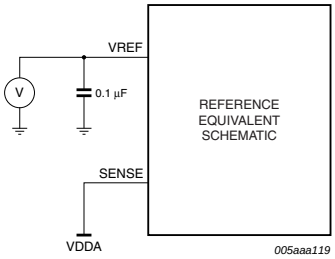


Fig 13. External reference, 1 V (p-p) to 2 V (p-p) full-scale

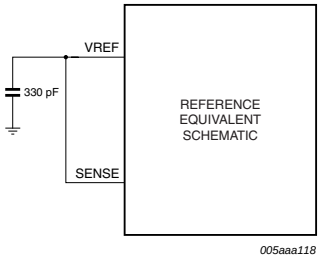


Fig 14. Internal reference via SPI, 1 V (p-p) to 2 V (p-p) full-scale

Figure 11 to Figure 14 indicate how to connect the SENSE and VREF pins.

13.2.2 Reference gain control

The reference gain is programmable between 0 dB to −6 dB in steps of 1 dB via the SPI (see Table 21). The corresponding full scale input voltage range varies between 2 V (p-p) and 1 V (p-p), as shown in Table 11:

Table 11. Reference SPI gain control

INTREF[2:0]	Level	Full Scale, V (p-p)
000	0 dB	2
001	−1 dB	1.78
010	−2 dB	1.59
011	−3 dB	1.42
100	−4 dB	1.26
101	−5 dB	1.12
110	−6 dB	1
111	not used	x

13.2.3 Common-mode output voltage ($V_{I(cm)}$)

An 0.1 μF filter capacitor should be connected between on the one hand the pins VCMA and VCMB and on the other hand ground to ensure a low-noise common-mode output voltage. When AC-coupled, these pins can be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.

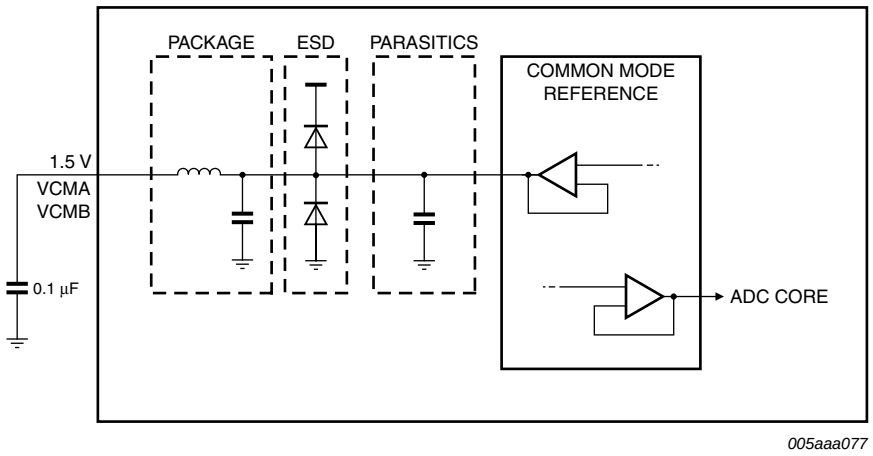


Fig 15. Reference equivalent schematic

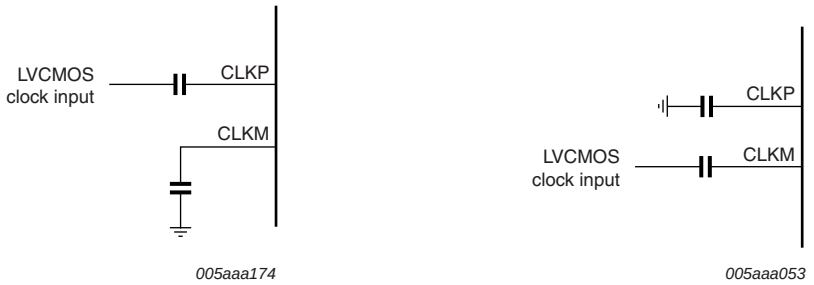
13.2.4 Biasing

The common-mode output voltage, $V_{O(cm)}$, should be set externally to 1.5 V (typical). The common-mode input voltage, $V_{I(cm)}$, at the inputs to the sample and hold stage (pins INAM, INBM, INAP, and INBP) must be between 0.9 V and 2 V for optimal performance.

13.3 Clock input

13.3.1 Drive modes

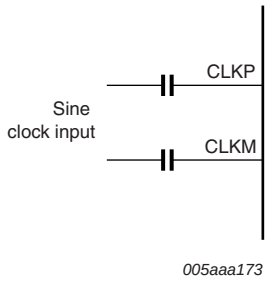
The ADC1113D125 can be driven differentially (SINE, LVPECL or LVDS) with little or no influence on dynamic performances. It can also be driven by a single-ended LVCMOS signal connected to pin CLKP (CLKM should be connected to ground via a capacitor).



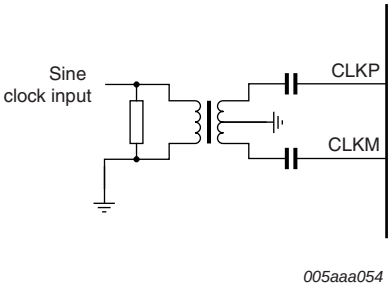
a. Rising edge LVCMOS

b. Falling edge LVCMOS

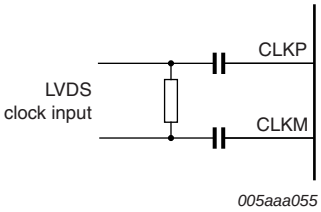
Fig 16. LVCMOS single-ended clock input



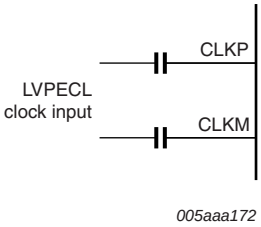
a. Sine clock input



b. Sine clock input (with transformer)



c. LVDS clock input



d. LVPECL clock input

Fig 17. Differential clock input

13.3.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 18. The common-mode voltage of the differential input stage is set via internal resistors of 5 kΩ resistors.

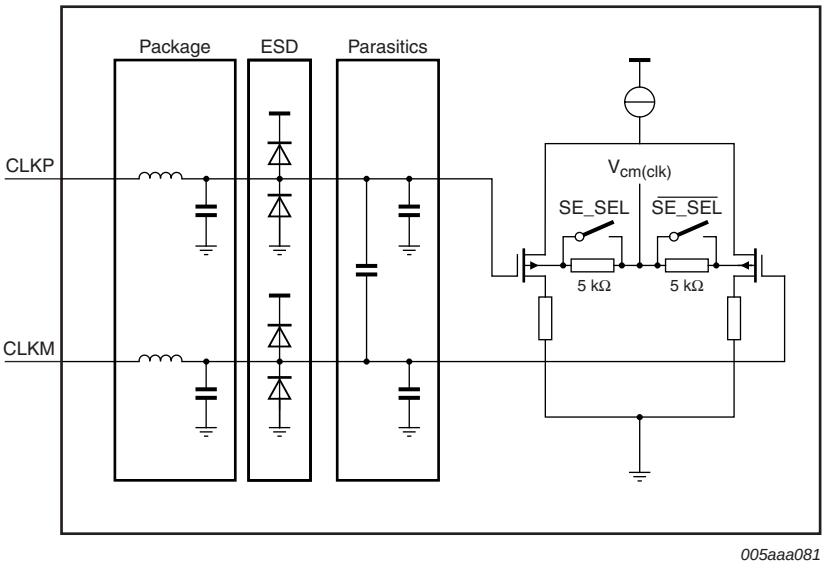


Fig 18. Equivalent input circuit

Single-ended or differential clock inputs can be selected via the SPI (see Table 20). If single-ended is selected, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting SE_SEL accordingly, the unused pin should be connected to ground via a capacitor.

13.3.3 Clock input divider

The ADC1113D125 contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = 1; see Table 20). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

13.3.4 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the input clock signal duty cycle. When the duty cycle stabilizer is active (bit DCS_EN = 1; see Table 20), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

Table 12. Duty cycle stabilizer

DCS_enable SPI	Description
0	duty cycle stabilizer disable
1	duty cycle stabilizer enable

13.4 Digital outputs

13.4.1 Serial output equivalent circuit

The JESD204A standard specify that in case of connecting the receiver and the transmitter in DC coupling, both of them need to be provided by the same supply.

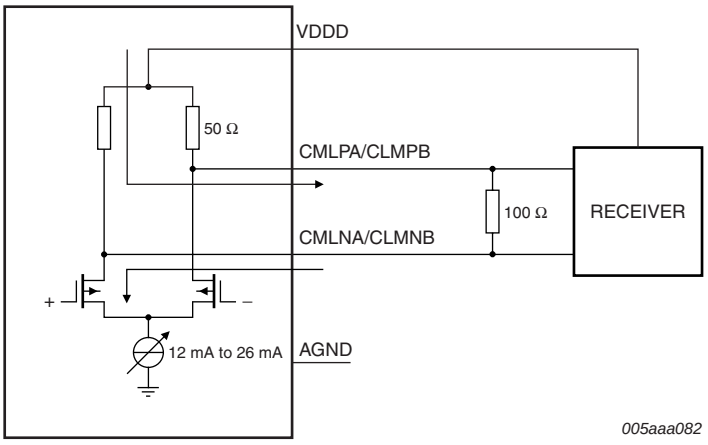


Fig 19. CML output connection to the receiver in DC coupling

The output should be terminated when 100 Ω (typical) has been reached at the receiver side.

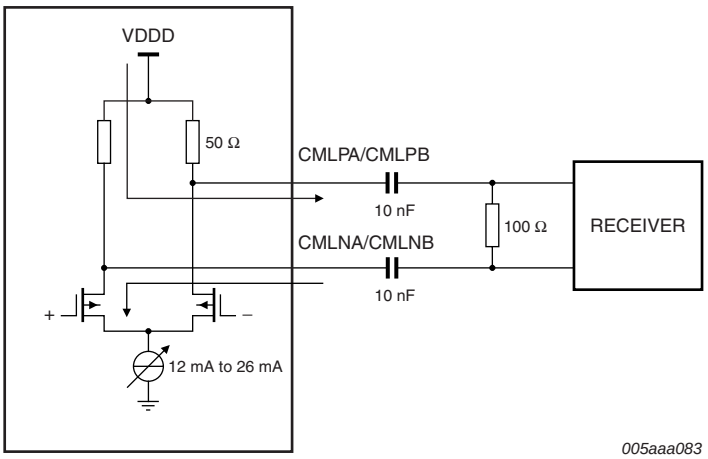


Fig 20. CML output connection to the receiver in AC coupling

13.5 JESD204A serializer

13.5.1 Digital JESD204A formatter

The block placed after the ADC cores is used to implement all functionalities of the JESD204A standard. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly parameterized and can be configured in various ways depending on the sampling frequency and the number of lanes used.

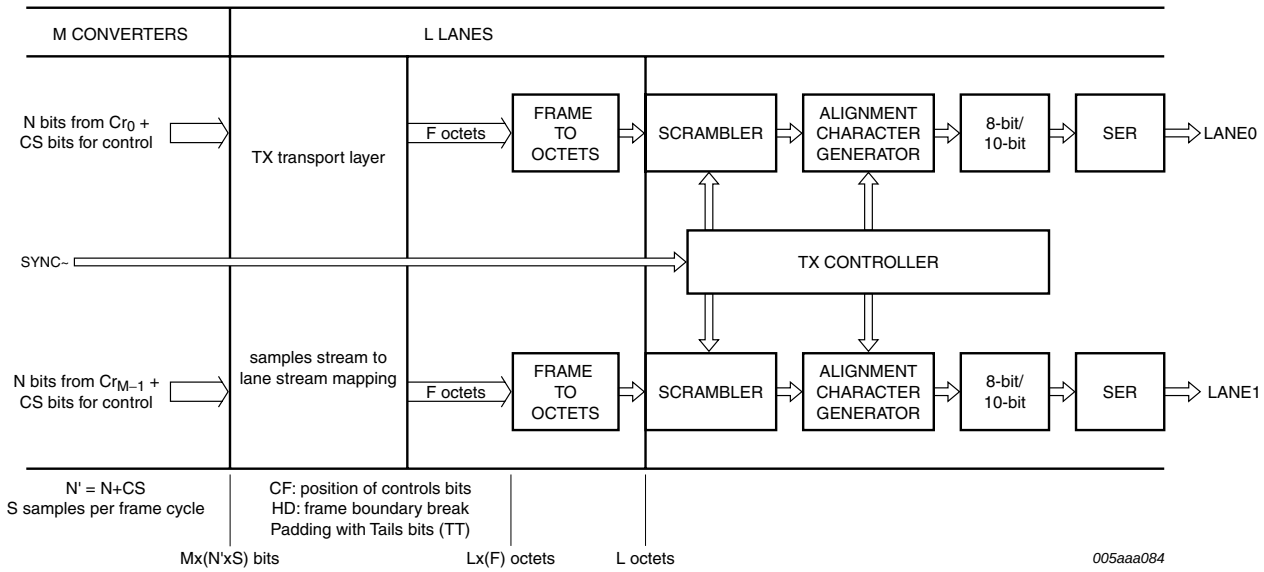


Fig 21. General overview of the JESD204A serializer

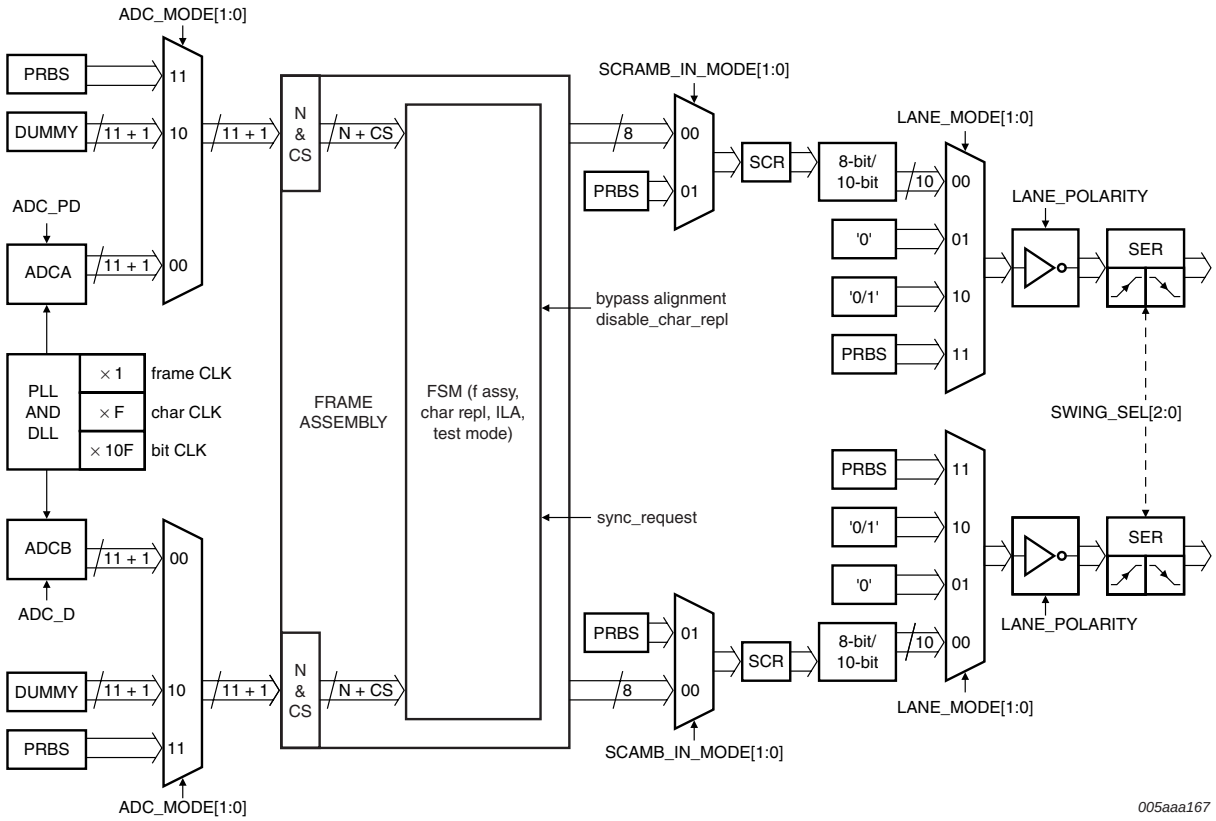


Fig 22. Detailed view of the JESD204A serializer with debug functionality

13.5.2 ADC core output codes versus input voltage

Table 13 shows the data output codes for a given analog input voltage.

Table 13. Output codes

$V_{INP} - V_{INM}$	Offset binary	Two's complement	OTR pin
< –1	000 0000 0000	100 0000 0000	1
–1.0000000	000 0000 0000	100 0000 0000	0
–0.9990234	000 0000 0001	100 0000 0001	0
–0.9980469	000 0000 0010	100 0000 0010	0
–0.9970703	000 0000 0011	100 0000 0011	0
–0.996093	000 0000 0100	100 0000 0100	0
....	....	....	0
–0.0019531	011 1111 1110	111 1111 1110	0
–0.0009766	011 1111 1111	111 1111 1111	0
0.0000000	**100 0000 0000**	**000 0000 0000**	0
+0.0009766	100 0000 0001	000 0000 0001	0
+0.0019531	100 0000 0010	000 0000 0010	0
....	....	....	0
+0.9960938	111 1111 1011	011 1111 1011	0

Table 13. Output codes

$V_{INP} - V_{INM}$	Offset binary	Two's complement	OTR pin
+0.9970703	111 1111 1100	011 1111 1100	0
+0.9980469	111 1111 1101	011 1111 1101	0
+0.9990234	111 1111 1110	011 1111 1110	0
+1.0000000	111 1111 1111	011 1111 1111	0
> +1	111 1111 1111	011 1111 1111	1

13.6 Serial Peripheral Interface (SPI)

13.6.1 Register description

The ADC1113D125 serial interface is a synchronous serial communications port allowing for easy interfacing with many industry microprocessors. It provides access to the registers that control the operation of the chip in both read and write modes.

This interface is configured as a 3-wire type (SDIO as bidirectional pin).

SCLK acts as the serial clock, and $\overline{CS}$ acts as the serial chip select bar.

Each read/write operation is sequenced by the $\overline{CS}$ signal and enabled by a LOW level to to drive the chip with 2 bytes to 5 bytes, depending on the content of the instruction byte (see Table 14).

Table 14. Instruction bytes for the SPI

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W[1]	W1	W0	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

[1] R/W indicates whether a read or write transfer occurs after the instruction byte

Table 15. Read or Write mode access description

R/W[1]	Description
0	Write mode operation
1	Read mode operation

[1] Bits W1 and W0 indicate the number of bytes transferred after the instruction byte.

Table 16. Number of bytes to be transferred

W1	W0	Number of bytes
0	0	1 byte transferred
0	1	2 bytes transferred
1	0	3 bytes transferred
1	1	4 or more bytes transferred

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is incremented to access subsequent addresses.

The steps involved in a data transfer are as follows:

1. The falling edge on $\overline{CS}$ in combination with a rising edge on SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can be vary in length but will always be a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes):

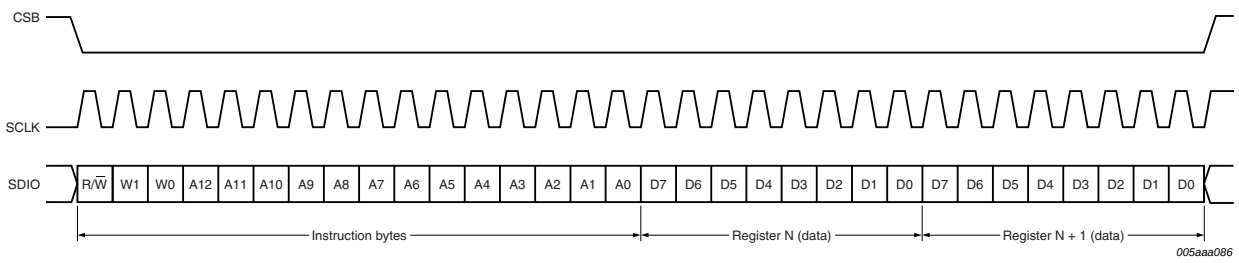


Fig 23. Transfer diagram for two data bytes (3-wire type)

13.6.2 Channel control

The two ADC channels can be configured at the same time or separately. By using the register “Channel index”, the user can choose which ADC channel will receive the next SPI-instruction. By default the channel A and B will receive the same instructions in write mode. In read mode only A is active.

Table 17. Register allocation map

Addr Hex	Register name	R/W[1]	Bit definition								Default[2] Bin
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ADC control registers											
0003	Channel index	R/W	-	-	-	-	-	-	ADCB	ADCA	1111 1111
0005	Reset and Operating modes	R/W	SW_RST	-	-	-	-	-	PD[1:0]		0000 0000
0006	Clock	R/W	-	-	-	SE_SEL	DIFF_SE	-	CLKDIV2_SEL	DCS_EN	0000 000X
0008	Vref	R/W	-	-	-	-	INTREF_EN	INTREF[2:0]			0000 0000
0013	Offset	R/W	-	-	DIG_OFFSET[5:0]						0000 0000
0014	Test pattern 1	R/W	-	-	-	-	-	TESTPAT_1[2:0]			0000 0000
0015	Test pattern 2	R/W	TESTPAT_2[10:3]								0000 0000
0016	Test pattern 3	R/W	TESTPAT_3[2:0]			-	-	-	-	-	0000 0000
JESD204A control											
0801	Ser_Status	R	RXSYNC_ERROR	RESERVED[2:0]			0	0	POR_TST	RESERVED	0000 0000
0802	Ser_Reset	R/W	SW_RST	0	0	0	FSM_SW_RST	0	0	0	0000 0000
0803	Ser_Cfg_Setup	R/W	0	0	0	0	CFG_SETUP[3:0]				0000 ****
0805	Ser_Control1	R/W	0	TriState_CFG_PAD	SYNC_POL	SYNC_SINGLEENDED	1	RESERVED[2:0]			0100 1001
0806	Ser_Control2	R/W	0	0	0	0	0	0	SWAP_LANE_1_2	SWAP_ADC_0_1	0000 00**
0808	Ser_Analog_Ctrl	R/W	0	0	0	0	0	SWING_SEL[2:0]			0000 00**
0809	Ser_ScramblerA	R/W	0	LSB_INIT[6:0]							0000 0000
080A	Ser_ScramblerB	R/W	MSB_INIT[7:0]								1111 1111
080B	Ser_PRBS_Ctrl	R/W	0	0	0	0	0	0	PRBS_TYPE[1:0]		0000 0000
0820	Cfg_0_DID	R/W*	DID[7:0]								1110 1101

Table 17. Register allocation map *…continued*

Addr Hex	Register name	R/W[1]	Bit definition								Default[2] Bin
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0821	Cfg_1_BID	R/W*	0	0	0	0	BID[3:0]				0000 1010
0822	Cfg_3_SCR_L	R/W*	SCR	0	0	0	0	0	0	L	*000 000*
0823	Cfg_4_F	R/W*	0	0	0	0	0	F[2:0]			0000 0***
0824	Cfg_5_K	R/W*	0	0	0	K[4:0]					000* ****
0825	Cfg_6_M	R/W*	0	0	0	0	0	0	0	M	0000 000*
0826	Cfg_7_CS_N	R/W*	0	CS[0]	0	0	N[3:0]				0100 0***
0827	Cfg_8_Np	R	0	0	0	NP[4:0]					0000 1111
0828	Cfg_9_S	R/W*	0	0	0	0	0	0	0	S	0000 0000
0829	Cfg_10_HD_CF	R/W*	HD	0	0	0	0	0	CF[1:0]		*000 0000
082C	Cfg_01_2_LID	R/W*	0	0	0	LID[4:0]					0001 1011
082D	Cfg_02_2_LID	R/W*	0	0	0	LID[4:0]					0001 1100
084C	Cfg01_13_FCHK	R	FCHK[7:0]								**** ****
084D	Cfg02_13_FCHK	R	FCHK[7:0]								**** ****
0870	LaneA_0_Ctrl	R/W	0	SCR_IN_MODE	LANE_MODE[1:0]		0	LANE_POL	LANE_CLK_POS_EDGE	LANE_PD	0000 000*
0871	LaneB_0_Ctrl	R/W	0	SCR_IN_MODE	LANE_MODE[1:0]		0	LANE_POL	LANE_CLK_POS_EDGE	LANE_PD	0000 000*
0890	ADCA_0_Ctrl	R/W	0	0	ADC_MODE[1:0]		0	0	0	ADC_PD	0000 000*
0891	ADCB_0_Ctrl	R/W	0	0	ADC_MODE[1:0]		0	0	0	ADC_PD	0000 000*

[1] an "*" in the Access column means that this register is subject to control access conditions in Write mode.

[2] an "*" in the Default column replaces a bit of which the value depends on the binary level of external pins (e.g. CFG[3:0], Swing[1:0], Scrambler).

13.6.3 Register description

13.6.3.1 ADC control registers

Table 18. Register channel Index (address 0003h)

Bit	Symbol	Access	Value	Description
7 to 2	-	-	111111	not used
1	ADCB	R/W		ADCB will get the next SPI command:
			0	ADCB not selected
			1	ADCB selected
0	ADCA	R/W		ADCA will get the next SPI command:
			0	ADCA not selected
			1	ADCA selected

Table 19. Register reset and Power-down mode (address 0005h)

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W		reset digital part:
			0	no reset
			1	performs a reset of the digital part
6 to 2	-	-	00000	not used
1 to 0	PD[1-0]	R/W		power-down mode:
			00	normal (power-up)
			01	full power-down
			10	sleep
			11	normal (power-up)

Table 20. Register clock (address 0006h)

Bit	Symbol	Access	Value	Description
7 to 5	-	-	000	not used
4	SE_SEL	R/W		select SE clock input pin:
			0	Select CLKM input
			1	Select CLKP input
3	DIFF_SE	R/W		differential/single ended clock input select:
			0	Fully differential
			1	Single-ended
2	-	-	0	not used
1	CLKDIV2_SEL	R/W		select clock input divider by 2:
			0	disable
			1	active
0	DCS_EN	R/W		duty cycle stabilizer enable:
			0	disable
			1	active

Table 21. Register Vref (address 0008h)

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3	INTREF_EN	R/W		enable internal programmable VREF mode:
			0	disable
			1	active
2 to 0	INTREF[2:0]	R/W		programmable internal reference:
			000	0 dB (FS=2 V)
			001	−1 dB (FS=1.78 V)
			010	−2 dB (FS=1.59 V)
			011	−3 dB (FS=1.42 V)
			100	−4 dB (FS=1.26 V)
			101	−5 dB (FS=1.12 V)
			110	−6 dB (FS=1 V)
			111	not used

Table 22. Digital offset adjustment (address 0013h)

Register offset: (address 0013h)		
Decimal	**DIG_OFFSET[5:0]**	
+31	011111	+31 LSB
...	...	...
0	**000000**	0
...	...	...
−32	100000	−32 LSB

Table 23. Register test pattern 1 (address 0014h)

Bit	Symbol	Access	Value	Description
7 to 3	-	-	00000	not used
2 to 0	TESTPAT_1[2:0]	R/W		digital test pattern:
			000	off
			001	mid-scale
			010	− FS
			011	+ FS
			100	toggle ‘1111..1111’/’0000..0000’
			101	custom test pattern, to be written in register 0015h and 0016h
			110	‘010101...’
			111	‘101010...’

Table 24. Register test pattern 2 (address 0015h)

Bit	Symbol	Access	Value	Description
7 to 0	TESTPAT_2[10:3]	R/W	**00000000**	custom digital test pattern (bit 13 to 6)

Table 25. Register test pattern 3 (address 0016h)

Bit	Symbol	Access	Value	Description
7 to 5	TESTPAT_3[2:0]	R/W	**00000**	custom digital test pattern (bit 5 to 0)
4 to 0	-	-	000	not used

13.6.4 JESD204A digital control registers

Table 26. SER status (address 0801h)

Bit	Symbol	Access	Value	Description
7	RXSYNC_ERROR	R/W	0	set to 1 when a synchronization error occurs
6 to 4	RESERVED[2:0]	-	**001**	reserved
3 to 2	-	-	0	not used
1	POR_TST	R	**0**	power-on-reset
0	RESERVED	-	-	reserved

Table 27. SER reset (address 0802h)

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W	**0**	initiates a software reset of the JEDEC204A unit
6 to 4	-	-	000	not used
3	FSM_SW_RST	R/W	**0**	initiates a software reset of the internal state machine of JEDEC204A unit
2 to 0	-	-	000	not used

Table 28. SER cfg set-up (address 0803h)[1]

Bit	Symbol	Access	Value	Description
7 to 4	-	R	0000	not used
3 to 0	CFG_SETUP[3:0]	R/W	0000 (reset)	defines quick JESD204A configuration. These settings overrule the CFG_PAD configuration
			0000	ADC0: ON; ADC1: ON; Lane0: ON; Lane1: ON; F = 2; HD = 0; K = 9; M = 2; L = 2[2]
			0001	ADC0: ON; ADC1: ON; Lane0: ON; Lane1: OFF; F = 4; HD = 0; K = 5; M = 2; L = 1[2]
			0010	ADC0: ON; ADC1: ON; Lane0: OFF; Lane1: ON; F = 4; HD = 0; K = 5; M = 2; L = 1 SWAP_LANE_1_2 = 1[2]
			0011	ADC0: ON; ADC1: OFF; Lane0: ON; Lane1: ON; F = 1; HD = 1; K = 17; M = 1; L = 2[2]
			0100	ADC0: OFF; ADC1: ON; Lane0: ON; Lane1: ON; F = 1; HD = 1; K = 17; M = 1; L = 2; SWAP_ADC_0_1 = 1[2]
			0101	ADC0: ON; ADC1: OFF; Lane0: ON; Lane1: OFF; F = 2; HD = 0; K = 9; M = 1; L = 1[2]
			0110	ADC0: ON; ADC1: OFF; Lane0: OFF; Lane1: ON; F = 2; HD = 0; K = 9; M = 1; L = 1; SWAP_LANE_1_2 = 1[2]
			0111	ADC0: OFF; ADC1: ON; Lane0: ON; Lane1: OFF; F = 2; HD = 0; K = 9; M = 1; L = 1; SWAP_ADC_0_1 = 1[2]
			1000	ADC0: OFF; ADC1: ON; Lane0: OFF; Lane1: ON; F = 2; HD = 0; K = 9; M = 1; L = 1; SWAP_ADC_0_1[2]
			1001 to 1101	reserved
			1110	ADC0: OFF; ADC1: OFF; Lane0: ON; Lane1: ON; F = 2; HD = 0; K = 9; M = 2; L = 2; loop alignment = 1[2]
			1111	ADC0: OFF; ADC1: OFF; Lane0: OFF; Lane1: OFF; F = 2; HD = 0; K = 9; M = 2; L = 2 → PD[2]

[1] The default value for this register depends on the external pull-up/pull-down on CFG0, CFG1, CFG2 or CFG3. Writing to the register overwrites this value.

[2] F: number of byte per frame; HD: High density; K: number of frames per multi frame; M: number of converters; L: number of lanes

See the information about the JESD204A standard on the JEDEC web site.

Table 29. SER control1 (address 0805h)

Bit	Symbol	Access	Value	Description
7	-	R	0	not used
6	TRISTATE_CFG_PAD	R/W	**1**	CFG pads (3 to 0) are set to high-impedance. Switch to 0 automatically after start-up or reset.
5	SYNC_POL	R/W		defines the sync signal polarity:
			0	synchronization signal is active low
			1	synchronization signal is active high
4	SYNC_SINGLE_ENDED	R/W		defines the input mode of the sync signal:
			0	synchronization input mode is set in Differential mode
			1	synchronization input mode is set in Single-ended mode
3	-	R	1	not used

Table 29. SER control1 (address 0805h) *...continued*

Bit	Symbol	Access	Value	Description
2	REV_SCR	-		enables swapping bits at the scrambler input
			0	
			1	LSB are swapped to MSB at the scrambler input
1	REV_ENCODER	-		enables swapping bits at the 8b/10b encoder input:
			0	
			1	LSB are swapped to MSB at the 8b/10b encoder input
0	REV_SERIAL	-		enables swapping bits at the lane input (before serializer):
			0	
			1	LSB are swapped to MSB at the lane input

Table 30. SER control2 (address 0806h)

Bit	Symbol	Access	Value	Description
7 to 2	-	R	000000	not used
1	SWAP_LANE_1_2	R/W		controls the JESD204A output multiplexer:
			0	
			1	outputs of the JESD204A unit are swapped. (Output0 is connected to Lane1, Output1 is connected to Lane0)
0	SWAP_ADC_0_1	R/W		controls the JESD204A input multiplexer:
			0	
			1	inputs of the JESD204A unit are swapped. (ADC0 output is connected to Input1, ADC1 is connected to Input0)

Table 31. SER analog ctrl (address 0808h)

Bit	Symbol	Access	Value	Description
7 to 3	-	R	00000	not used
2 to 0	SWING_SEL[2:0]	R/W	**0****	defines the swing output for the lane pads

Table 32. SER scramblerA (address 0809h)

Bit	Symbol	Access	Value	Description
7	-	R	0	not used
6 to 0	LSB_INIT[6:0]	R/W	**0000000**	defines the initialization vector for the scrambler polynomial (lower)

Table 33. SER scramblerB (address 080Ah)

Bit	Symbol	Access	Value	Description
7 to 0	MSB_INIT[7:0]	R/W	**11111111**	defines the initialization vector for the scrambler polynomial (upper)

Table 34. SER PRBS Ctrl (address 080Bh)

Bit	Symbol	Access	Value	Description
7 to 2	-	R	000000	not used
1 to 0	PRBS_TYPE[1:0]	R/W		defines the type of Pseudo-Random Binary Sequence (PRBS) generator to be used:
			00 (reset)	PRBS-7
			01	PRBS-7
			10	PRBS-23
			11	PRBS-31

Table 35. Cfg_0_DID (address 0820h)

Bit	Symbol	Access	Value	Description
7 to 0	DID[7:0]	R	**11101101**	defines the device (= link) identification number

Table 36. Cfg_1_BID (address 0821h)

Bit	Symbol	Access	Value	Description
7 to 4	-	R	0000	not used
3 to 0	BID[3:0]	R/W	**1010**	defines the bank ID – extension to DID

Table 37. Cfg_3_SCR_L (address 0822h)

Bit	Symbol	Access	Value	Description
7	SCR	R/W	*	scrambling enabled
6 to 1	-	R	000000	not used
0	L	R/W	*	defines the number of lanes per converter device, minus 1

Table 38. Cfg_4_F (address 0823h)

Bit	Symbol	Access	Value	Description
7 to 3	-	R	00000	not used
2 to 0	F[2:0]	R/W	***	defines the number of octets per frame, minus 1

Table 39. Cfg_5_K (address 0824h)

Bit	Symbol	Access	Value	Description
7 to 5	-	R	000	not used
4 to 0	K[4:0]	R/W	*****	defines the number of frames per multiframe, minus 1

Table 40. Cfg_6_M (address 0825h)

Bit	Symbol	Access	Value	Description
7 to 1	-	R	0000000	not used
0	M	R/W	*	defines the number of converters per device, minus 1

Table 41. Cfg_7_CS_N (address 0826h)

Bit	Symbol	Access	Value	Description
7	-	R	0	not used
6	CS[0]	R/W	*	defines the number of control bits per sample, minus 1
5 to 4	-	R	00	not used
3 to 0	N[3:0]	R/W	****	defines the converter resolution

Table 42. Cfg_8_Np (address 0827h)

Bit	Symbol	Access	Value	Description
7 to 5	-	R	000	not used
4 to 0	NP[4:0]	R/W	*****	defines the total number of bits per sample, minus 1

Table 43. Cfg_9_S (address 0828h)

Bit	Symbol	Access	Value	Description
7 to 1	-	R	0000000	not used
0	S	R/W	**1**	defines number of samples per converter per frame cycle

Table 44. Cfg_10_HD_CF (address 0829h)

Bit	Symbol	Access	Value	Description
7	HD	R/W	*	defines high density format
6 to 2	-	R	00000	not used
1 to 0	CF[1:0]	R/W	**	defines number of control words per frame clock cycle per link.

Table 45. Cfg01_2_LID (address 082Ch)

Bit	Symbol	Access	Value	Description
7 to 5	-	R	000	not used
4 to 0	LID[4:0]	R/W	**11011**	defines lane1 identification number

Table 46. Cfg02_2_LID (address 082Dh)

Bit	Symbol	Access	Value	Description
7 to 5	-	R	000	not used
4 to 0	LID[4:0]	R/W	**11100**	defines lane2 identification number

Table 47. Cfg02_13_fchk (address 084Ch)

Bit	Symbol	Access	Value	Description
7 to 0	FCHK[7:0]	R	********	defines the checksum value for lane1 checksum corresponds to the sum of all the link configuration parameters modulo 256 (as defined in JEDEC Standard No.204A)

Table 48. Cfg01_13_fchk (address 084Dh)

Bit	Symbol	Access	Value	Description
7 to 0	FCHK[7:0]	R	********	defines the checksum value for lane1 checksum corresponds to the sum of all the link configuration parameters module 256 (as defined in JEDEC Standard No.204A)

Table 49. LaneA_0_ctrl (address 0870h)

Bit	Symbol	Access	Value	Description
7	-	R	0	not used
6	SCR_IN_MODE	R/W		defines the input type for scrambler and 8-bit/10-bit units:
			0 (reset)	(normal mode) = Input of the scrambler and 8-bit/10-bit units is the output of the frame assembly unit.
			1	input of the scrambler and 8-bit/10-bit units is the PRSB generator (PRBS type is defined with “PRBS_TYPE” (Ser_PRBS_ctrl register)
5 to 4	LANE_MODE[1:0]	R/W		defines output type of Lane output unit:
			00 (reset)	normal mode: Lane output is the 8-bit/10-bit output unit
			01	constant mode: Lane output is set to a constant (0×0)
			10	toggle mode: Lane output is toggling between 0×0 and 0×1
			11	PRBS mode: Lane output is the PRBS generator (PRBS type is defined with “PRBS_TYPE” (Ser_PRBS_ctrl register)
3	-	R	0	not used
2	LANE_POL	R/W		defines lane polarity:
			0	lane polarity is normal
			1	lane polarity is inverted
1	LANE_CLK_POS_EDGE	R/W		defines lane clock polarity:
			0	lane clock provided to the serializer is active on positive edge
			1	lane clock provided to the serializer is active on negative edge
0	Lane_PD	R/W		lane power-down control:
			0	lane is operational
			1	lane is in Power-down mode

Table 50. LaneB_0_ctrl (address 0871h)

Bit	Symbol	Access	Value	Description
7	-	R	0	not used
6	SCR_IN_MODE	R/W		defines the input type for scrambler and 8b/10b units:
			0 (reset)	(normal mode) = Input of the scrambler and 8b/10b units is the output of the Frame Assembly unit.
			1	input of the scrambler and 8b/10b units is the PRSB generator (PRBS type is defined with “PRBS_TYPE” (Ser_PRBS_ctrl register)

Table 50. LaneB_0_ctrl (address 0871h) *...continued*

Bit	Symbol	Access	Value	Description
5 to 4	LANE_MODE[1:0]	R/W		defines output type of lane output unit:
			00 (reset)	normal mode: Lane output is the 8b/10b output unit
			01	constant mode: Lane output is set to a constant (0x0)
			10	toggle mode: Lane output is toggling between 0x0 and 0x1
			11	PRBS mode: Lane output is the PRBS generator (PRBS type is defined with “PRBS_TYPE” (Ser_PRBS_ctrl register)
3	-	R	0	not used
2	LANE_POL	R/W		defines lane polarity:
			0	lane polarity is normal
			1	lane polarity is inverted
1	LANE_CLK_POS_EDGE	R/W		defines lane clock polarity:
			0	lane clock provided to the serializer is active on positive edge
			1	lane clock provided to the serializer is active on negative edge
0	Lane_PD	R/W		lane power-down control:
			0	lane is operational
			1	lane is in Power-down mode

Table 51. ADCA_0_ctrl (address 0890h)

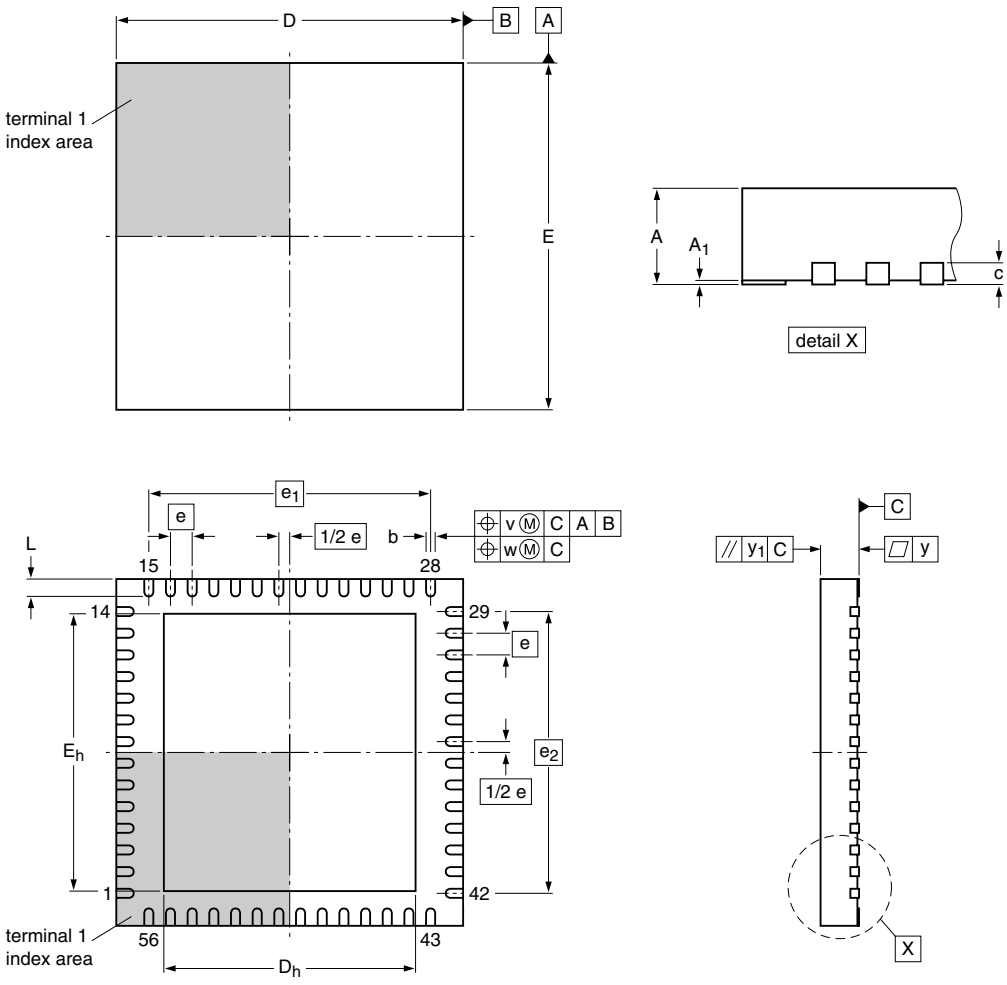
Bit	Symbol	Access	Value	Description
7 to 6	-	R	00	not used
5 to 4	ADC_MODE[1:0]	R/W		defines input type of JESD204A unit:
			00 (reset)	ADC output is connected to the JESD204A input
			01	not used
			10	JESD204A input is fed with a dummy constant, set to: OTR = 0 and ADC[10:0] = “1001101110”
			11	JESD204A is fed with a PRBS generator (PRBS type is defined with “PRBS_TYPE” (Ser_PRBS_ctrl register)
3 to 1	-	R	000	not used
0	ADC_PD	R/W		ADC power-down control:
			0	ADC is operational
			1	ADC is in Power-down mode

Table 52. ADCB_0_ctrl (address 0891h)

Bit	Symbol	Access	Value	Description
7 to 6	-	R	00	not used
5 to 4	ADC_MODE[1:0]	R/W		defines input type of JESD204A unit
			00 (reset)	ADC output is connected to the JESD204A input
			01	not used
			10	JESD204A input is fed with a dummy constant, set to: OTR = 0 and ADC[10:0] = “1001101110”
			11	JESD204A is fed with a PRBS generator (PRBS type is defined with “PRBS_TYPE” (Ser_PRBS_ctrl register)
3 to 1	-	R	000	not used
0	ADC_PD	R/W		ADC power-down control:
			0	ADC is operational
			1	ADC is in Power-down mode

14. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-7**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		8.1	5.95	8.1	6.55				0.5				
mm	nom	0.85	0.02	0.21	0.2	8.0	5.80	8.0	6.40	0.5	6.5	6.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		7.9	5.65	7.9	6.25				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot684-7_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT684-7	- - -	MO-220	- - -			~~08-11-19~~ 09-03-04

Fig 24. Package outline SOT684-7 (HVQFN56)

15. Revision history

Table 53. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1113D125_2	20100423	Preliminary data sheet	-	ADC1113D125_1
Modifications:	Product status changed from Objective to Preliminary			
ADC1113D125_1	20100412	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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