



TC1412/TC1412N

2A High-Speed MOSFET Drivers

Features

- Latch-Up Protected: Will Withstand 500 mA Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected: 4 kV
- High Peak Output Current: 2A
- Wide Input Supply Voltage Operating Range:
 - 4.5V to 16V
- High Capacitive Load Drive Capability:
 - 1000 pF in 18 nsec
- Short Delay Time: 35 nsec Typ.
- Matched Delay Times
- Low Supply Current:
 - With Logic '1' Input: 500 μ A
 - With Logic '0' Input: 100 μ A
- Low Output Impedance: 4 Ω
- Available in Space-Saving 8-pin MSOP Package
- Pinout Same as TC1410/TC1411/TC1413

General Description

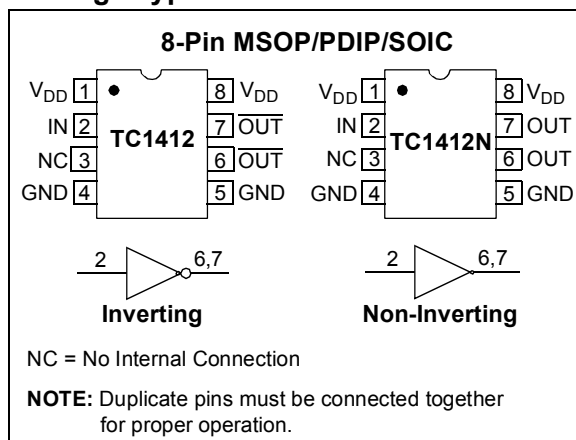
The TC1412/TC1412N are 2A CMOS buffers/drivers. They will not latch-up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the TC1412/TC1412N can easily charge a 1000 pF gate capacitance in 18 nsec with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The leading and trailing edge propagation delay times are also matched to allow driving short-duration inputs with greater accuracy.

Applications

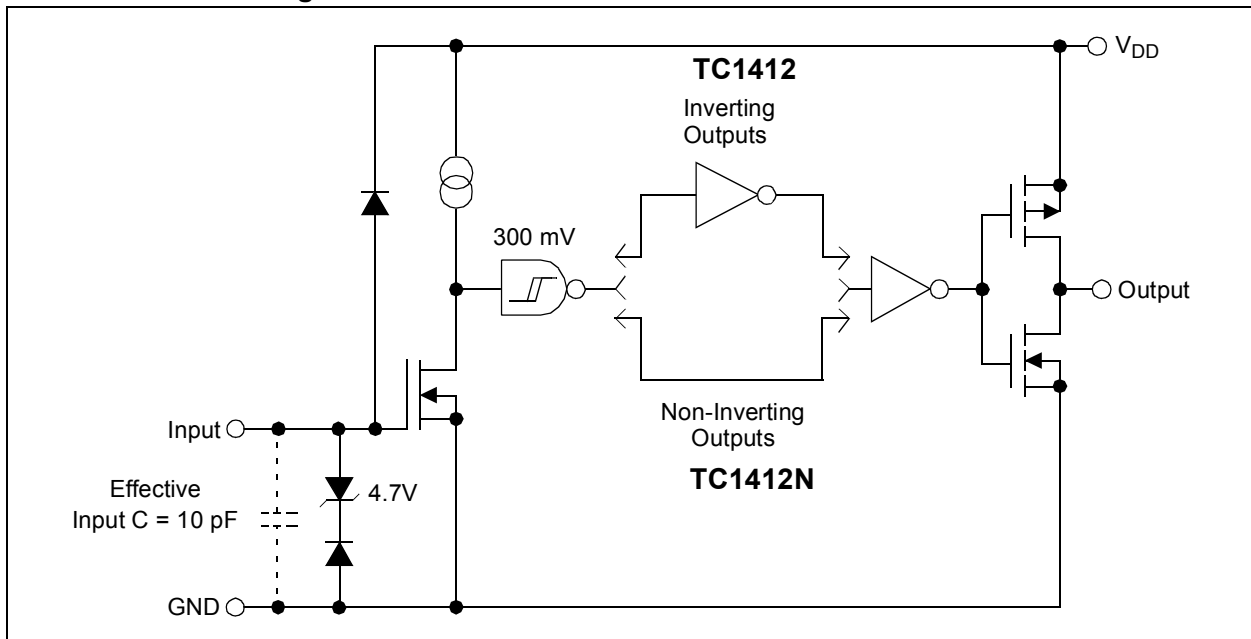
- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Relay Driver

Package Type



TC1412/TC1412N

Functional Block Diagram



TC1412/TC1412N

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage +20V

Input Voltage $V_{DD} + 0.3V$ to GND – 5.0V

Power Dissipation ($T_A \leq 70^\circ\text{C}$)

MSOP 340 mW

PDIP 730 mW

SOIC 470 mW

Storage Temperature Range -65°C to $+150^\circ\text{C}$

Maximum Junction Temperature $+150^\circ\text{C}$

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Symbol	Description
V_{DD}	Supply input, 4.5V to 16V
INPUT	Control input
NC	No connection
GND	Ground
GND	Ground
OUTPUT	CMOS push-pull output, common to pin 7
OUTPUT	CMOS push-pull output, common to pin 6
V_{DD}	Supply input, 4.5V to 16V

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, over operating temperature range with $4.5V \leq V_{DD} \leq 16V$. Typical values are measured at $T_A = +25^\circ\text{C}$, $V_{DD} = 16V$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.0	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1.0 -10	—	1.0 10	μA	$0V \leq V_{IN} \leq V_{DD}$, $T_A = +25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Output						
High Output Voltage	V_{OH}	$V_{DD} - 0.025$	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	—	4 5 5	6 7 7	Ω	$V_{DD} = 16V$, $I_O = 10\text{ mA}$, $T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Peak Output Current	I_{PK}	—	2.0	—	A	$V_{DD} = 16V$
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	0.5	—	A	Duty cycle $\leq 2\%$, $t \leq 300\ \mu\text{sec}$, $V_{DD} = 16V$
Switching Time (Note 1)						
Rise Time	t_R	—	18 20 22	26 31 31	nsec	$T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, Figure 4-1
Fall Time	t_F	—	18 20 22	26 31 31	nsec	$T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, Figure 4-1

Note 1: Switching times ensured by design.

TC1412/TC1412N

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, over operating temperature range with $4.5V \leq V_{DD} \leq 16V$. Typical values are measured at $T_A = +25^\circ C$, $V_{DD} = 16V$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Delay Time	t_{D1}	—	35	45	nsec	$T_A = +25^\circ C$, $0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$, Figure 4-1
		—	40	50		
		—	40	50		
Delay Time	t_{D2}	—	35	45	nsec	$T_A = +25^\circ C$ $0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$, Figure 4-1
		—	40	50		
		—	40	50		
Power Supply						
Power Supply Current	I_S	—	0.5	1.0	mA	$V_{IN} = 3V$, $V_{DD} = 16V$ $V_{IN} = 0V$
		—	0.1	0.15		

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	$^\circ C$	
Specified Temperature Range (E)	T_A	-40	—	+85	$^\circ C$	
Maximum Junction Temperature	T_J	—	—	+150	$^\circ C$	
Storage Temperature Range	T_A	-65	—	+150	$^\circ C$	
Package Thermal Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	$^\circ C/W$	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	$^\circ C/W$	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	$^\circ C/W$	

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with $4.5V \leq V_{DD} \leq 16V$.

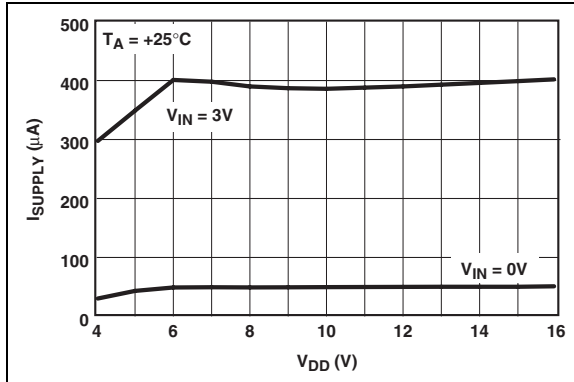


FIGURE 2-1: Quiescent Supply Current vs. Supply Voltage.

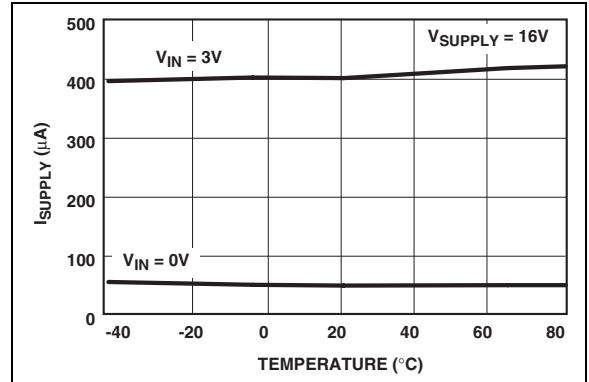


FIGURE 2-4: Quiescent Supply Current vs. Temperature.

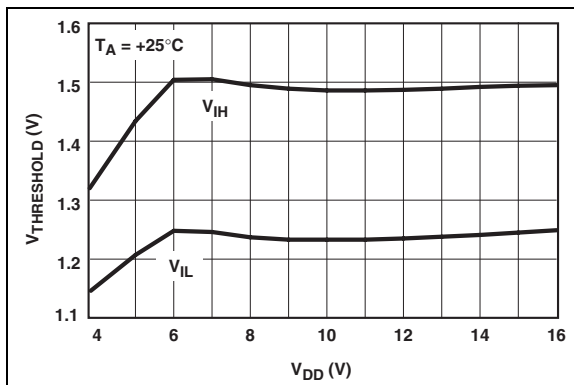


FIGURE 2-2: Input Threshold vs. Supply Voltage.

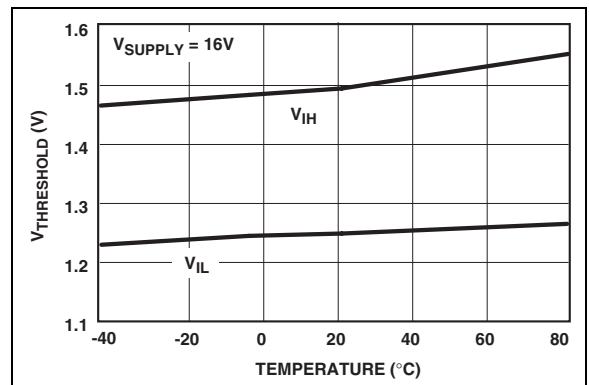


FIGURE 2-5: Input Threshold vs. Temperature.

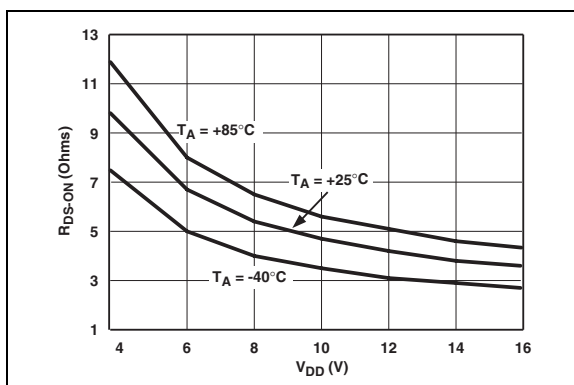


FIGURE 2-3: High-State Output Resistance vs. Supply Voltage.

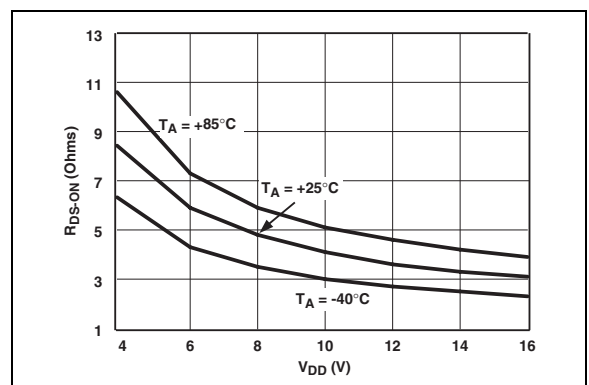


FIGURE 2-6: Low-State Output Resistance vs. Supply Voltage.

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Note: Unless otherwise indicated, over operating temperature range with $4.5V \leq V_{DD} \leq 16V$.

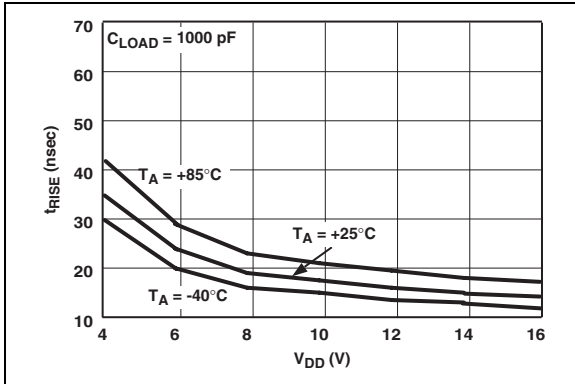


FIGURE 2-7: Rise Time vs. Supply Voltage.

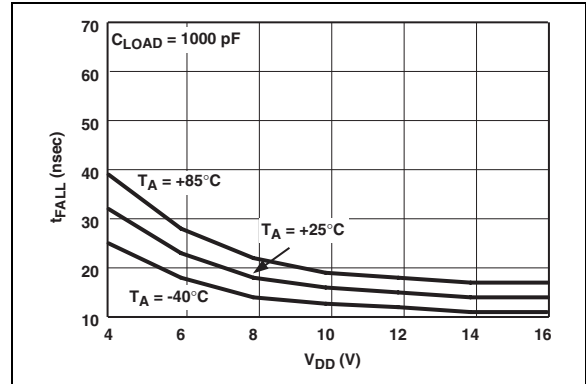


FIGURE 2-10: Fall Time vs. Supply Voltage.

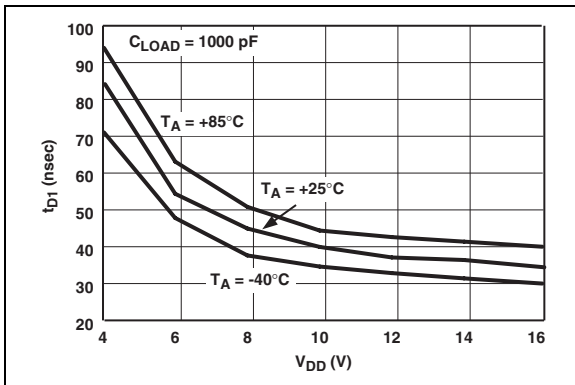


FIGURE 2-8: Propagation Delay vs. Supply Voltage.

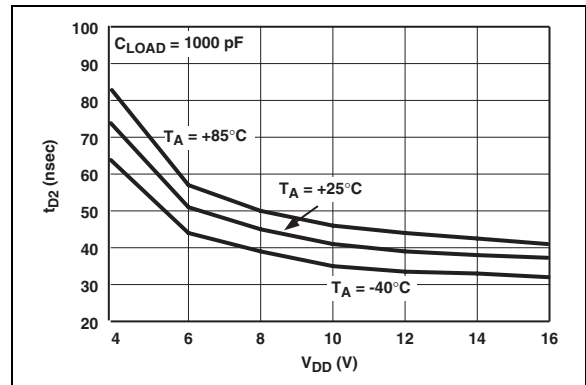


FIGURE 2-11: Propagation Delay vs. Supply Voltage.

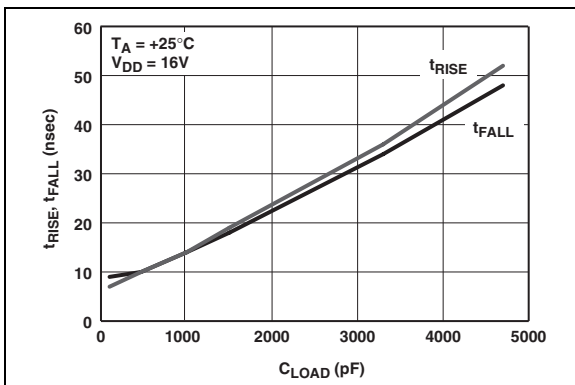


FIGURE 2-9: Rise and Fall Times vs. Capacitive Load.

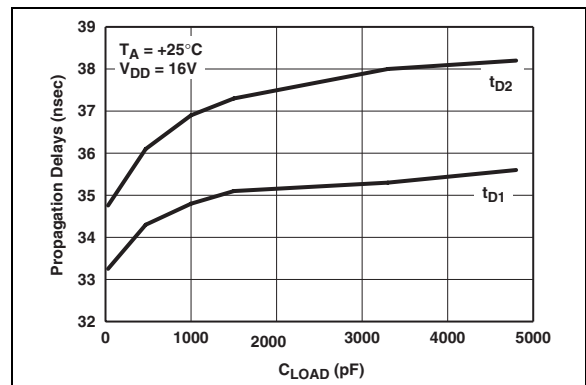


FIGURE 2-12: Propagation Delays vs. Capacitive Load.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Symbol	Description
1	V _{DD}	Supply input, 4.5V to 16V
2	INPUT	Control input
3	NC	No connection
4	GND	Ground
5	GND	Ground
6	OUTPUT	CMOS push-pull output, common to pin 7
7	OUTPUT	CMOS push-pull output, common to pin 6
8	V _{DD}	Supply input, 4.5V to 16V

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 16V with respect to the ground pin. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A value of 1.0 μ F is suggested.

3.2 Control Input (INPUT)

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input has 300 mV of hysteresis between the high and low thresholds which prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-Pull Output (OUTPUT)

The MOSFET driver output is a low-impedance, CMOS push-pull style output, capable of driving a capacitive load with 2A peak currents.

3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

3.5 No Connect (NC)

No internal connection.

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4.0 APPLICATION INFORMATION

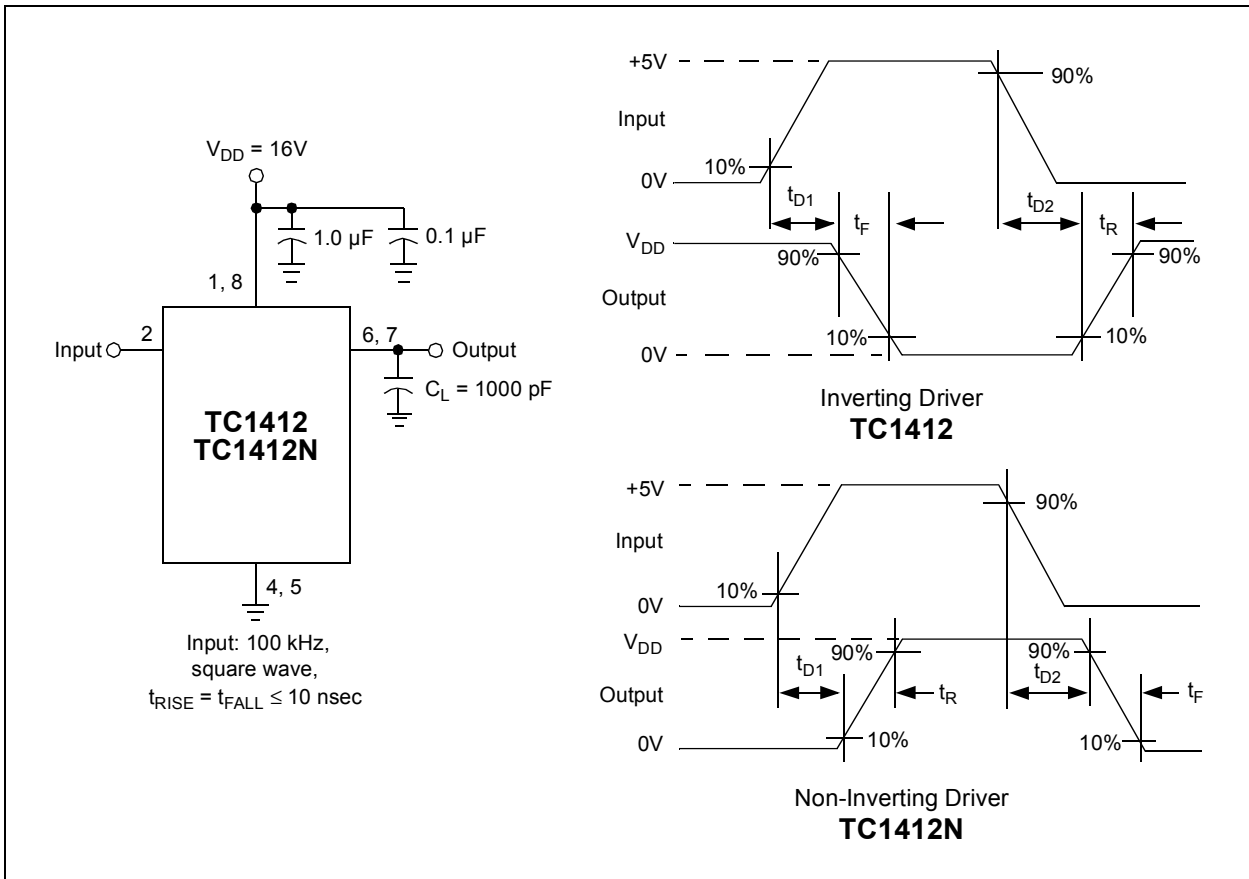


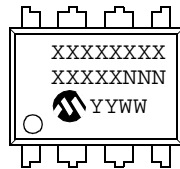
FIGURE 4-1: Switching Time Test Circuit.

TC1412/TC1412N

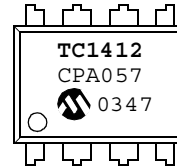
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

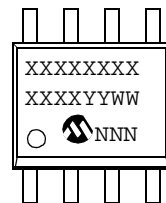
8-Lead PDIP (300 mil)



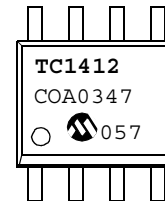
Example:



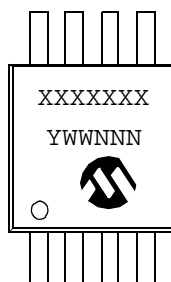
8-Lead SOIC (150 mil)



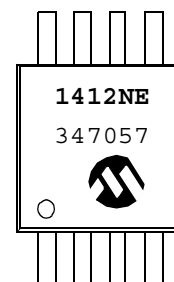
Example:



8-Lead MSOP



Example:

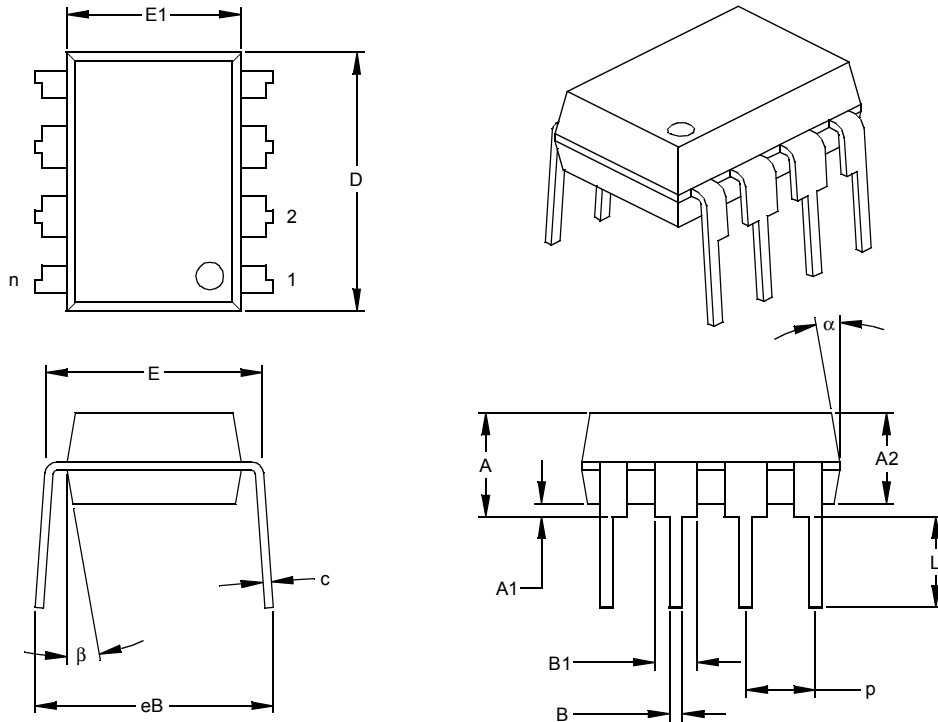


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

TC1412/TC1412N

8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)



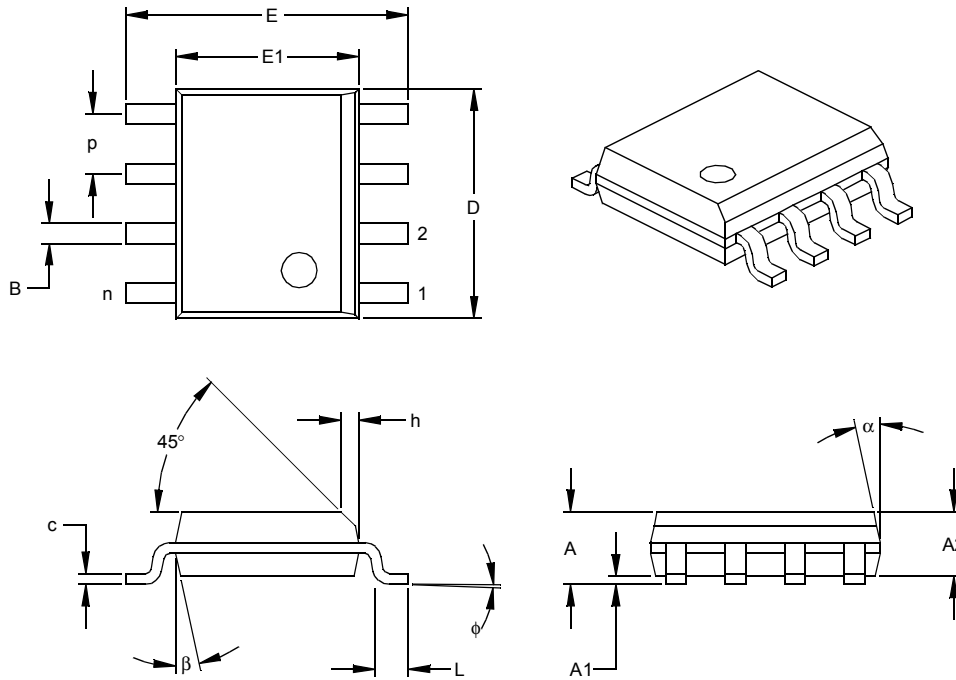
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-001
 Drawing No. C04-018

TC1412/TC1412N

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

Notes:

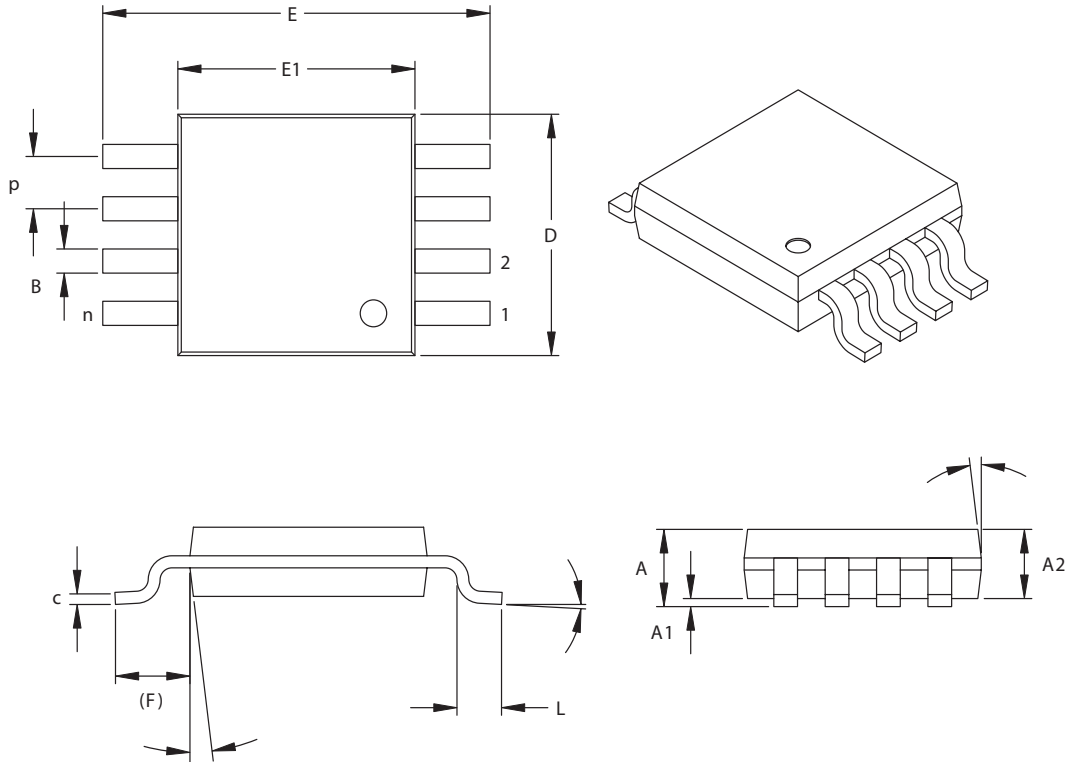
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

TC1412/TC1412N

8-Lead Plastic Micro Small Outline Package (UA) (MSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n			8			8
Pitch	P	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 BSC			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle		0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top		5°	-	15°	5°	-	15°
Mold Draft Angle Bottom		5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

TC1412/TC1412N

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
Device:	TC1412: 2 A Single MOSFET Driver, Inverting TC1412N: 2 A Single MOSFET Driver, Non-Inverting	
Temperature Range:	C = 0°C to +70°C E = -40°C to +85°C	
Package:	OA = Plastic SOIC, (150 mil Body), 8-lead OA713 = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel) UA = Plastic Micro Small Outline (MSOP), 8-lead * UA713 = Plastic Micro Small Outline (MSOP), 8-lead * (Tape and Reel) PA = Plastic DIP (300 mil Body), 8-lead * MSOP package is only available in E-Temp.	

Examples:

- a) TC1412COA: 2A Single MOSFET driver, SOIC package, 0°C to +70°C.
- b) TC1412CPA: 2A Single MOSFET driver, PDIP package, 0°C to +70°C.
- c) TC1412EUA713: Tape and Reel, 2A Single MOSFET driver, MSOP package, -40°C to +85°C.

- a) TC1412NCPA: 2A Single MOSFET driver, PDIP package, 0°C to +70°C.
- b) TC1412NEPA: 2A Single MOSFET driver, PDIP package, -40°C to +85°C.
- c) TC1412NEUA: 2A Single MOSFET driver, MSOP package, -40°C to +85°C.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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TC1412/TC1412N

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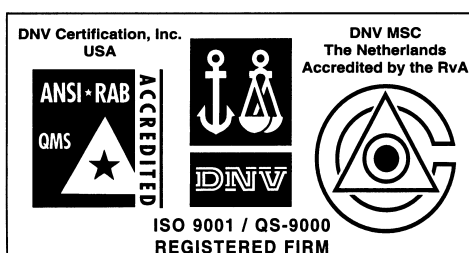
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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Atlanta

3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034 Fax: 770-640-0307

Boston

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Kokomo

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Los Angeles

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Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

Phoenix

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Marketing Support Division
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Hong Kong SAR

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380 Fax: 86-755-82966626

China - Qingdao

Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Microchip Technology Inc.
India Liaison Office
Marketing Support Division
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Microchip Technology Austria GmbH
Dürisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611 Fax: 39-0331-466781

United Kingdom

Microchip Ltd.
505 Eskdale Road
Widdersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869 Fax: 44-118-921-5820

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