CA82C12

8-BIT INPUT/OUTPUT PORT

- **High performance pin and function compatible replacement for the industry standard 8212**
- **TTL compatible input/output voltages**
- **Low power consumption**
- **8-bit parallel data register and buffer**
- **Interrupt generation logic using a service request flipflop**
- **Tri-state outputs**
- **Asynchronous register clear**
- **Ideal for reducing parts count in microcomputer system applications**
- **Manufactured using proven CMOS process technology**

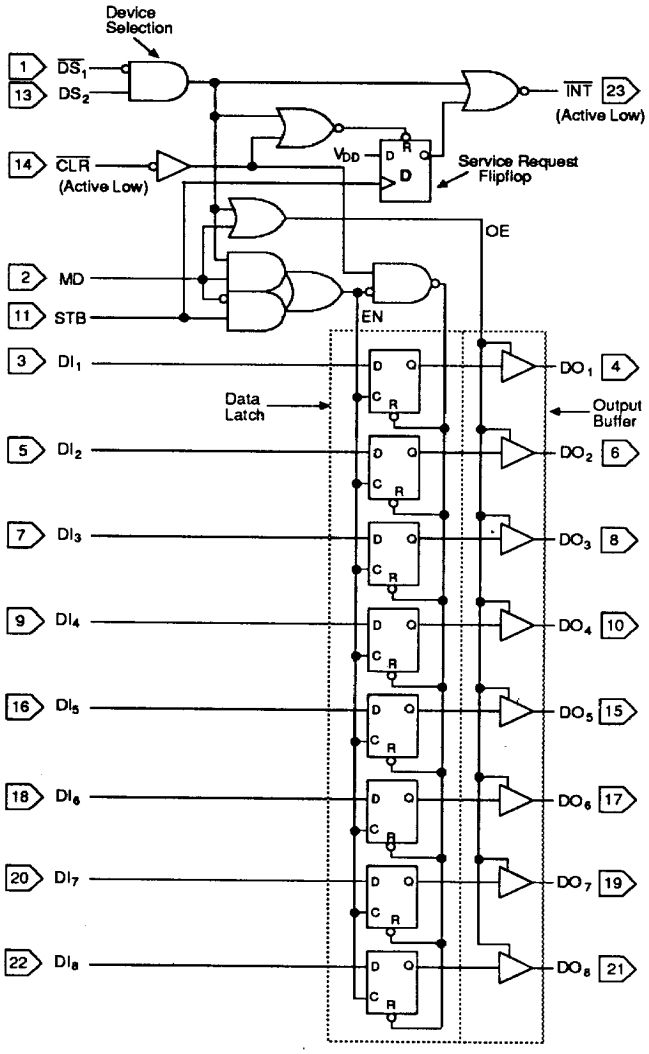

Figure 1 : CA82C12 LOGIC DIAGRAM

The CA82C12 Input/Output Port combines an 8-bit data latch and tri-state output buffers, with device selection and control logic. In addition, interrupt generation and control logic is provided for applications which require interfacing to microprocessor systems.

The CA82C12 is manufactured using proven CMOS process technology to produce a solid, reliable product. It is supplied in a selection of packages that are pin compatible with the industry standard 8212.

Overall, the CA82C12 is versatile component which can be used to implement many of the peripheral and input/output functions within high speed microcomputer systems, including latches, bus drivers, gated buffers and multiplexors. Featuring TTL compatibility and particularly low power consumption, this chip is ideally suited to portable or standby type applications.

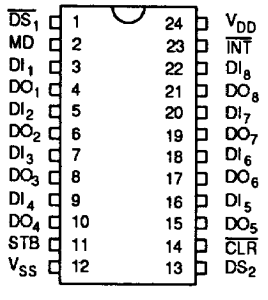

Figure 2 : PIN CONFIGURATION

FUNCTIONAL DESCRIPTION

The elements of the CA82C12 are shown in the logic diagram of Figure 1, with pin configuration and pin descriptions given in Figure 2 and Table 1 respectively. Note that three major functional areas comprise the chip: the data latch, data output buffer and control and interrupt logic.

Data Latch

Eight "D"-type latches, controlled by the "EN" signal, comprise the data latch. When EN is high, the output of each latch follows the corresponding data input (DI_{1-8}). The data at DO_{1-8} is latched when EN goes low.

The latched data is cleared by the active low $\overline{CLR}$ signal, if EN is low. If EN is high, $\overline{CLR}$ will be ignored since the data must be in a latched state before the data latches

Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s) DIP Package	Type	Name and Function
$\overline{CLR}$	14	I	**Clear:** This active low signal is used to reset the data latch and reset the D flipflop. It has NO effect on the output buffer. $\overline{CLR}$ overrides STB when generating an interrupt ($\overline{INT}$).
DI_1 - DI_8	3, 5, 7, 9, 16, 18, 20, 22	I	**Data In:** An 8-bit data field into the CA82C12. It can be connected directly to the system bus.
DO_1 - DO_8	4, 6, 8, 10, 15, 17, 19, 21	O	**Data Out:** Tri-state output lines which either display the contents of the data buffer, or are disabled by OE set low, (high impedance state)
$\overline{DS_1} \cdot DS_2$	1, 13	I	**Device Select:** The AND function of these two inputs is used for device selection. When ($\overline{DS_1} \cdot DS_2$) is high, the CA82C12 is selected, the output buffer is enabled, and the D flipflop is asynchronously reset. Note that $\overline{DS_1}$ is active low.
$\overline{INT}$	23	O	**Interrupt:** This active low signal is generated by either a device select, or by a strobe signal if $\overline{CLR}$ is high.
MD	2	I	**Mode:** This signal is used to determine both the state of the output buffer and the source of the data latch enable clock (EN). The CA82C12 is in input mode when MD is low, and in output mode when MD is high.
STB	11	I	**Strobe:** This input is used as the data latch enable clock when the CA82C12 is in input mode (MD is low), and to synchronously set the D flipflop.
V_{DD}	24	-	**Power:** 5.0v ± 10% VDC Supply
V_{SS}	12	-	**Ground:** 0v

can be cleared (reset). If the data is not latched (EN is high) when CLR goes low, then the outputs of the data latch (Q) will continue to follow their corresponding data inputs, overriding the reset signal.

Data Output Buffer

The output of each data latch (Q) is connected to a tri-state, non-inverting output buffer. Each of these buffers is controlled through a common control line, "output enable" (OE). When OE is high, the data output buffer is enabled, and data can be transferred from the data latch outputs (Q). When OE is low, the data output buffers are disabled, forcing the buffer outputs into a high impedance state. Thus, the CA82C12 can be connected directly onto a microprocessor bi-directional data bus.

Table 2 shows the data output buffer states under different control signal conditions.

Control and Interrupt Logic

The CA82C12 has four control signal inputs ($\overline{DS_1}$, DS_2, MD and STB), and an interrupt output ($\overline{INT}$). The inputs are used to control device selection, data latching, output buffer state and to generate interrupts.

Device Select ($\overline{DS_1}$, DS_2): The AND function of these two signals is used to select the device. That is, when $\overline{DS_1} \cdot DS_2$ is high, the device is selected. When selected, the output buffer is enabled (OE is high), and the service request flipflop "D" is cleared (reset) asynchronously.

Mode (MD): This input is used to generate the data buffer output enable signal (OE), and to determine the source of the data latch enable signal (EN).

When MD is high, the device is in "output mode," the data output buffers are enabled (OE is high), and the data latch enable signal (EN) is generated by the device select ($\overline{DS_1} \cdot DS_2$).

Table 2 : CONTROL LOGIC

STB	MD	$\overline{DS_1} \cdot DS_2$	Data Out Equals
0	0	0	Disabled (high impedance)
1	0	0	Disabled (high impedance)
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

Note that $\overline{CLR}$ resets both the data latch and the D flipflop, without affecting the output buffer.

Table 3 : INTERRUPT SIGNAL LOGIC

CLR	$\overline{DS_1} \cdot DS_2$	STB	Q[1]	$\overline{INT}$
0	0	0	0	1
0	0	H->L	0	1
0	1	0	0	0
1	0	0	0	1
1	0	H->L	1	0
1	1	0	0	0
1	1	H->L	0	0

Note: 1. Internal D flipflop signal

Figure 3 : TIMING DIAGRAMS

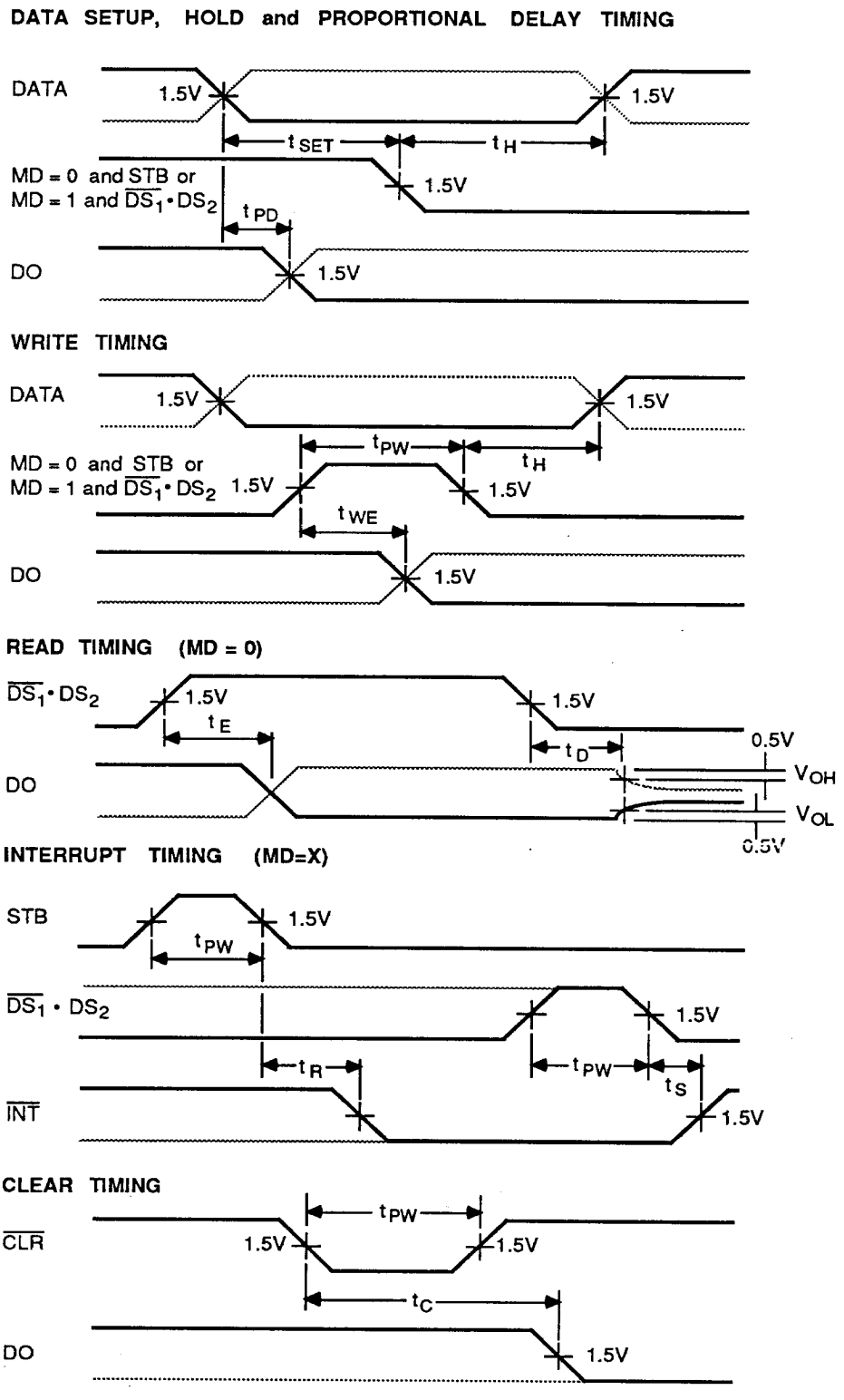

Table 4 : AC CHARACTERISTICS

T_A = 0 °C to +70 °C, V_{DD} = +5v ± 10%, C_L = 50 pF, R_L = 10K

Symbol	Parameter	Limits		Units
		Min	Max	
t_C	Clear to Output Delay	-	45	ns
t_D	Output Disable Time	-	45	ns
t_E	Output Enable Time	-	30	ns
t_H	Data Hold Time	10	-	ns
t_{PD}	Data to Output Delay	-	30	ns
t_{PW}	Pulse Width	25	-	ns
t_R	Reset to Output Delay	-	40	ns
t_S	Set to Output Delay	-	30	ns
t_{SET}	Data Set Up Time	15	-	ns
t_{WE}	Write Enable to Output Delay	-	40	ns

Table 5 : DC CHARACTERISTICS

T_A = -40 °C to +85 °C, V_{DD} = +5v ± 10%

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DD}	Power Supply Current	Active		1	mA
I_{IL}	Input Leakage Current	$0V \le V_{IN} \le V_{DD}$	-10	10	µA
I_{SC}	Short Circuit Output Current	V_{OUT} = 0v, V_{DD} = 5v	-15	-75	mA
V_{IL}	Input Low Voltage			0.85	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	3.7		V

Table 6 : ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias Plastic	0 °C to +70 °C
Storage Temperature	-65 °C to +160 °C
All Input Voltages	-1.0 to +5.5 Volts
All Output or Supply Voltages	-0.5 to +7 Volts
Output Currents	100mA

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.