SONY CXB1141Q/Q-Y

Hex 2 : 1 Multiplexer with D-FF

T-68-11-51

Description

The CXB1141Q is an ultra high speed monolithic ECL IC, which contains six 2 : 1 multiplexers followed by D type flip flops. The data select (SEL) input determines which data is enabled. The selected data is transferred to the flip flops output by the positive transition of clock (C1,C2) inputs. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

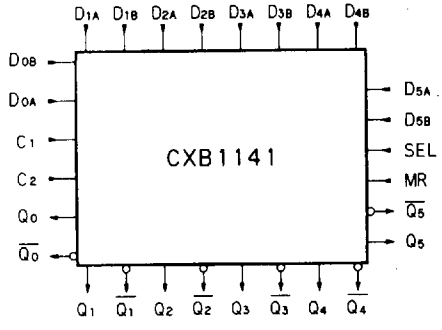
Features

- Typical clock rate up to 2.6 GHz
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

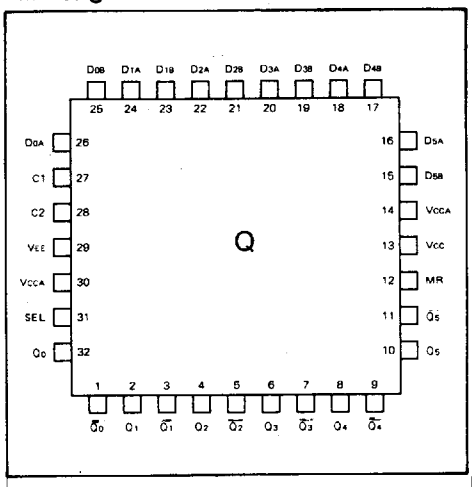
Pin Names

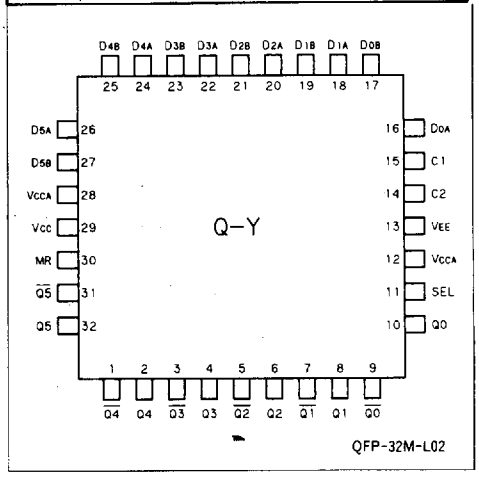
D_{nA}, D_{nB}	Data inputs
Qn, $\overline{Q_n}$	Data outputs
SEL	Data select input
Cn	Clock inputs
MR	Direct Master Reset input
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment





Truth Table

Select input	Outputs
SEL	Qn
L	D_{nA}
H	D_{nB}

Note : H ; HIGH voltage Level
L ; LOW voltage Level

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DC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−196	−144	−100	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	Cn	Qn		650	870	1130	ps
	T_{PHL}				670	900	1170	
	T_{PLH}	MR			780	1050	1370	
	T_{PHL}				780	1050	1370	
Gate-to-Gate skew	T_{SG-G}	Cn				50	100	
Set up time	Ts	D, Cn			100			
		SEL, Cn			300			
Hold time	Th	Cn, D			150			
		Cn, SEL			−50			
Release time	T_R	MR, Cn			340			
Min. Pulse width	T_{PW}	MR			610			
Max. Clock frequency	f_{MAX}	Cn			2.0	2.6		GHz
Rise time	T_{TLH}			20% to 80%		320	420	ps
Fall time	T_{THL}					290	380	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

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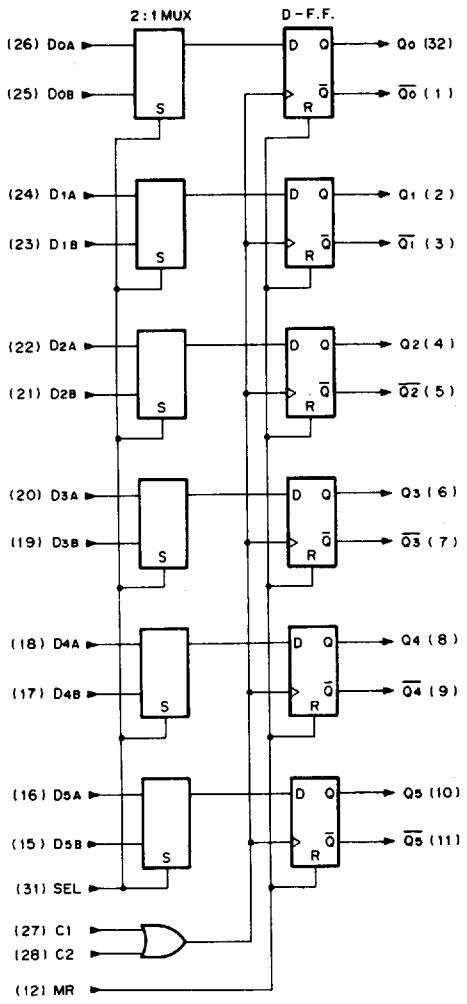
Block Diagram



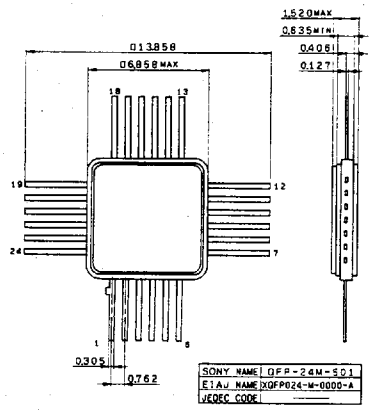
Package Data

T-90-20

Package Outline Uuit: mm

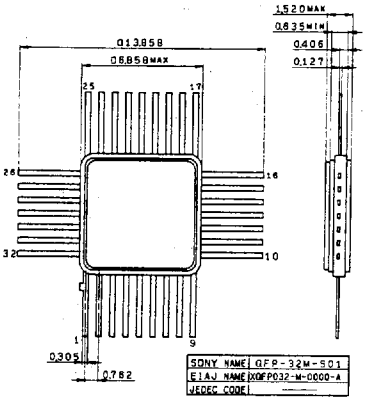
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



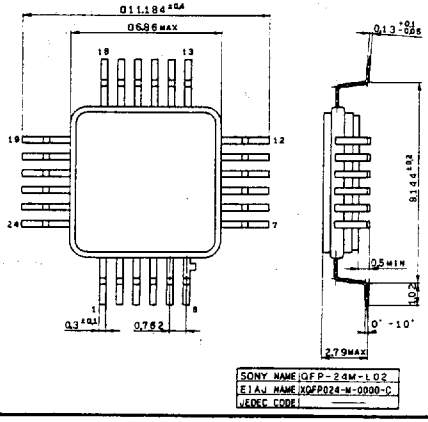
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



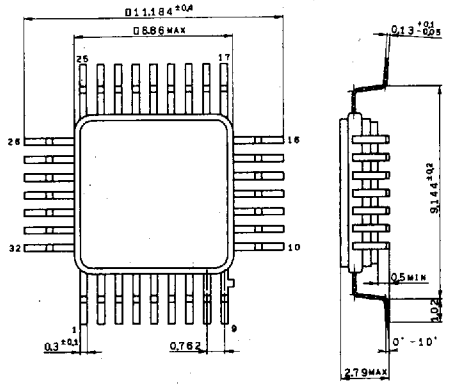
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

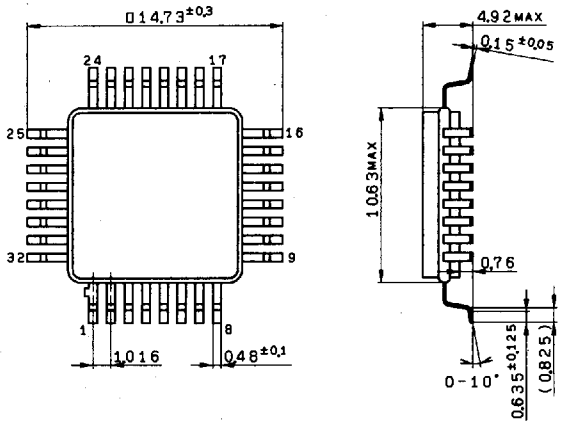
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

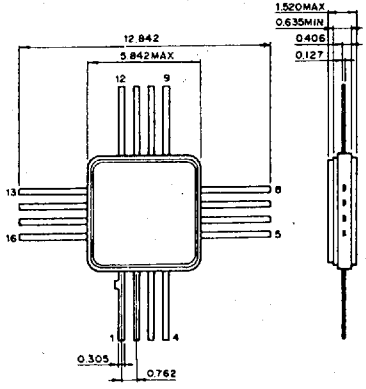
32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

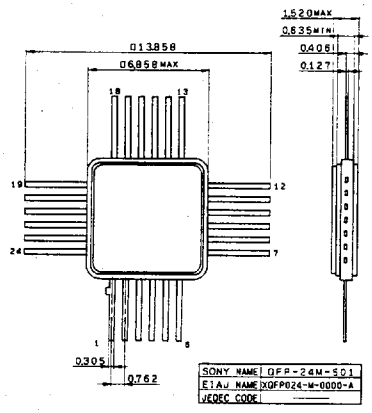
Package Data

T-90-20

Package Outline Uuit: mm

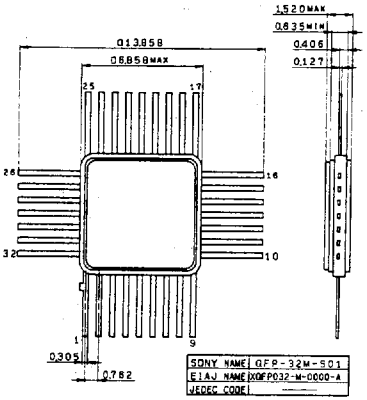
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



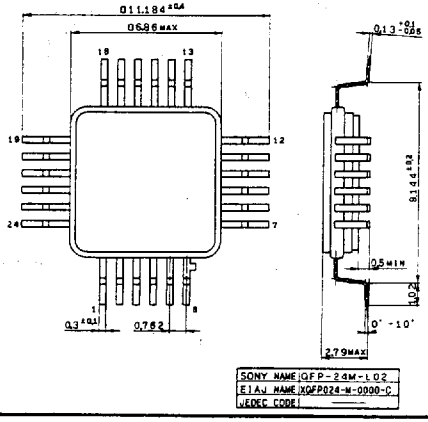
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



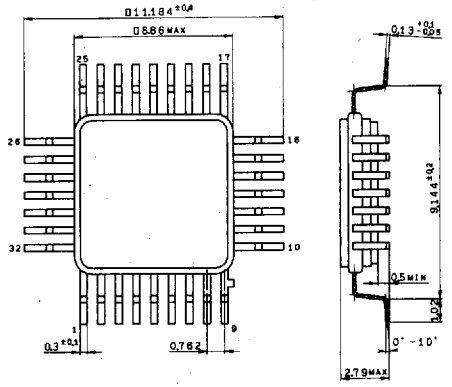
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

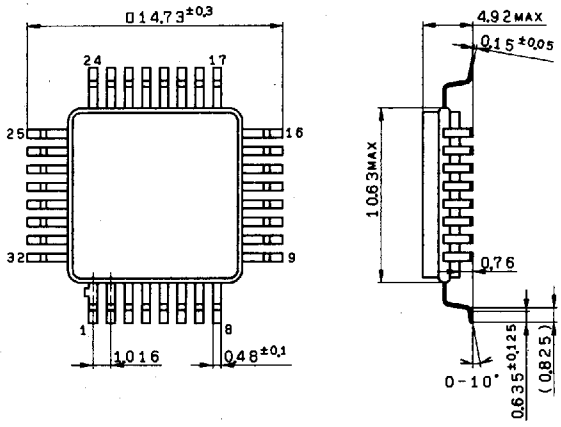
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP