Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY
IDT10496RL
IDT100496RL
IDT101496RL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed, with registers on inputs and latches on outputs
- Balanced Read/Write cycle time: 10/12/15 ns
- Access time: 10/12/15 ns (max.)
- Fully compatible with ECL logic levels
- Through-hole DIP and surface-mount packages

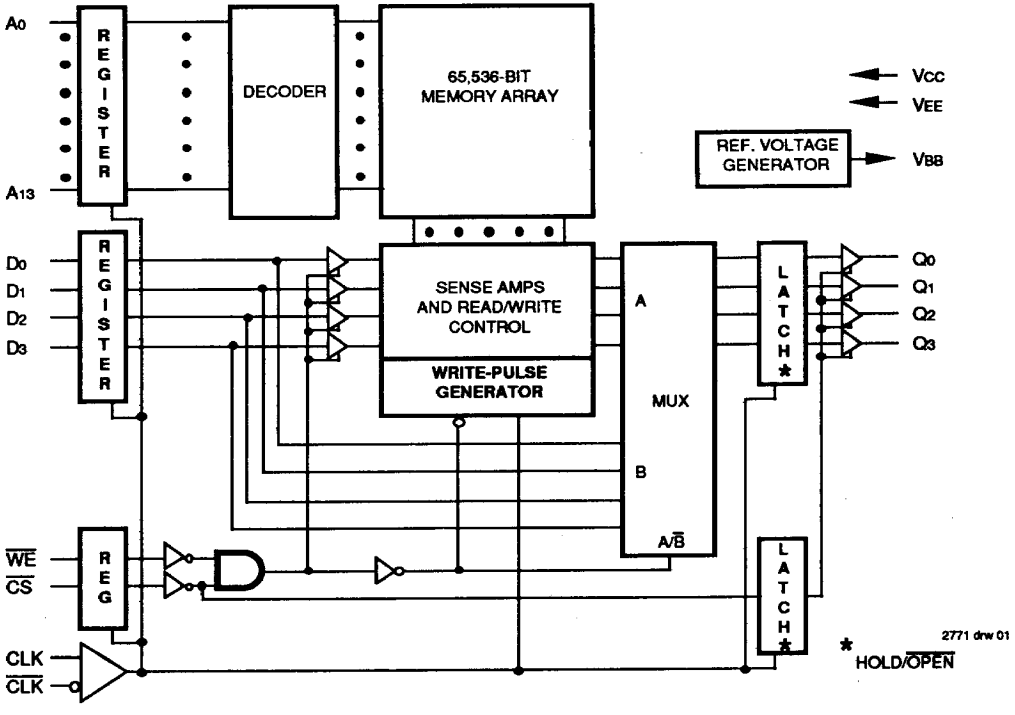
DESCRIPTION:

The IDT10496RL, IDT100496RL and IDT101496RL are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Clocked registers on inputs and latches on outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

Inputs are captured by the leading edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM



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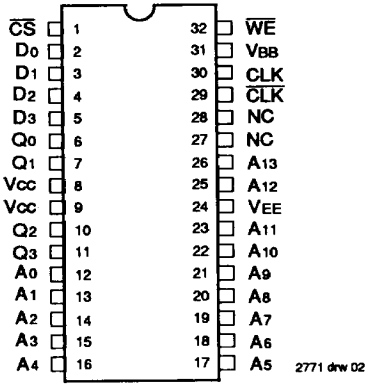
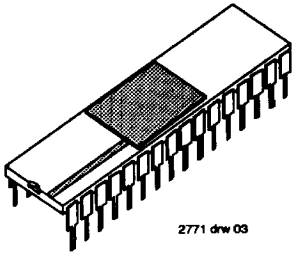
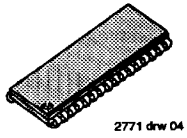
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



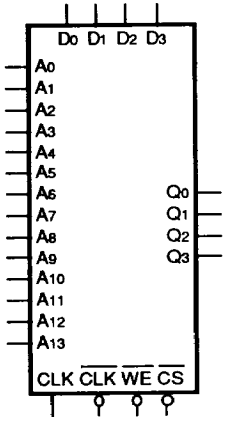
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTION

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
CLK, $\overline{CLK}$	Differential Clock Inputs
VBB	Reference Voltage Output (≈1.32V)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage
NC	No Connect - not internally bonded

2771 tbl 01

LOGIC SYMBOL



16Kx4
STRAM

2771 drw 05

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2764 tbl 02

NOTE:
1. Referenced to VCC

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CINCLK	Input Capacitance CLK/$\overline{CLK}$	6	–	3	–	pF
CIN	Input Capacitance except CLK/$\overline{CLK}$	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2773 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DataOUT(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

2773 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT initiated by falling edge of CLK.

ECL-10K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2771 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-260	-200	–	mA	–

2771 tbl 06

NOTES:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

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ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2771 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-240	-180	–	mA

2771 tbl 08

NOTES:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2771 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL =50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open(2)		-260	-200	–	mA

2771 tbl 10

NOTES:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

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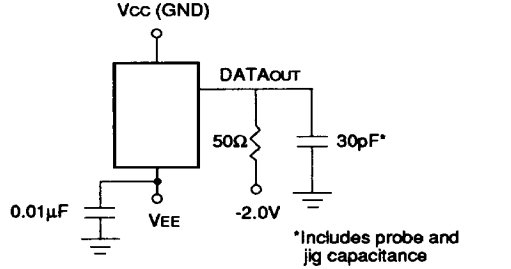
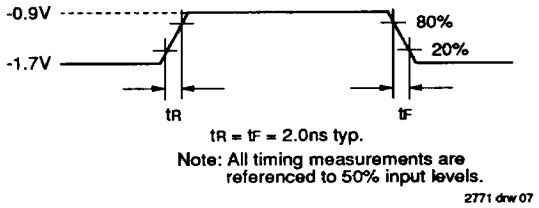
AC TEST LOAD CONDITION



AC TEST INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2771 tbl 11

FUNCTIONAL DESCRIPTION

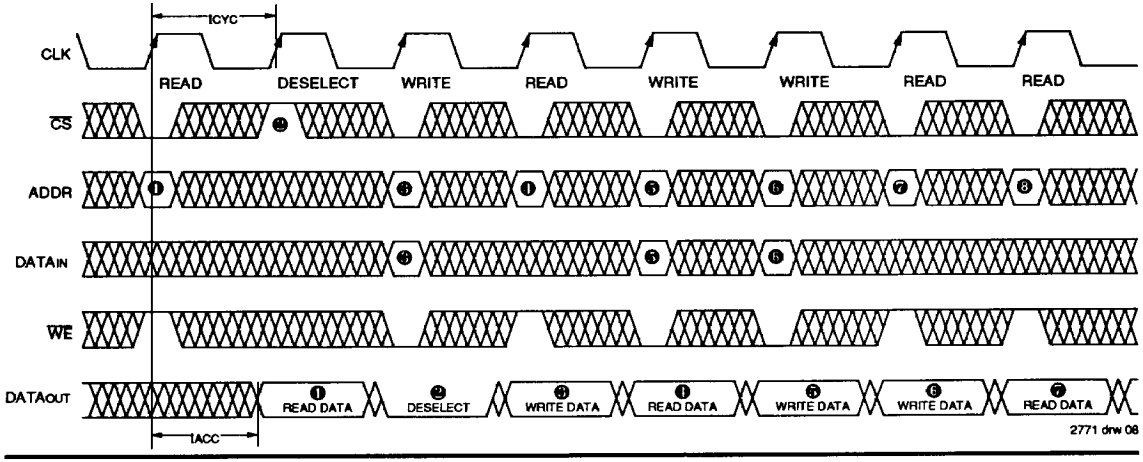
The IDT10496RL, IDT100496RL and IDT101496RL Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains clocked input registers to sample and hold addresses, input data, and control status. Inputs are sampled on the rising edge of the clock (CLK) input (falling edge of $\overline{CLK}$). In the case of a write cycle, the memory cell is written during the clock-high time, and write data conducted to the outputs. Output data flows out the output latch and is held into the next cycle.

READ TIMING

In a typical read cycle, the read address is captured by the rising edge of clock, as at ❶ below. Then, when clock goes low, the read data for the read address clocked in at ❶ is gated through the output latch to the output pins. There is a short delay from falling clock to output ready, called tDR (see Read Cycle Timing). If the clock-high time (tWH) is shorter than the inherent access-time of the cell, output is guaranteed valid after the specified tACC. But if tWH is longer than the cell access-time, output data will be valid tDR after clock goes low. Thus, the time it takes from clock-to-output for any given

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



address (the latency, or t_{ACC}) is

$$t_{ACC} = t_{ACC} \text{ or } (t_{WH} + t_{DR}),$$

whichever is larger.

The output latch takes some time to change state for the next cycle, but this time is very short. Therefore, data hold time from clock low (t_{DH}) is specified as zero minimum hold time.

DESELECT TIMING

Because the outputs are latched, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) at rising edge of clock. This case occurs at ❷ below. Outputs then attain the disable state (low) t_{ACC} later. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses the clock-high time as the write pulse, and thus determines the minimum clock-high time, t_{WH}.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins in the appropriate time slot (i.e. after $t_{WH} + t_{DR}$). This function is sometimes called "Transparent Write," and is useful for write-through cache applications. Thus the input data sampled at ❸ is available on the output at the end of the cycle.

There are no restrictions on the order of read cycles and write cycles.

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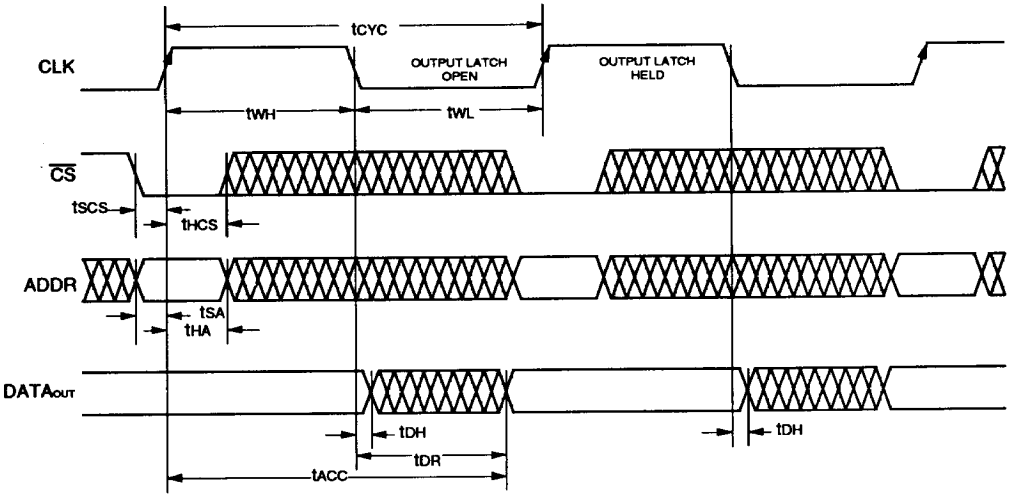
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
tCYC	Cycle Time	–	10	–	12	–	15	–	ns
tACC[2]	Access Time from Clock High	–	–	10	–	12	–	15	ns
tWL	Clock Low Pulse Width	–	5	–	5	–	6	–	ns
tWH	Clock High Pulse Width	–	5	–	5	–	6	–	ns
tSCS	Setup Time for Chip Select	–	1	–	1	–	1	–	ns
tSA	Setup Time for Address	–	1	–	1	–	1	–	ns
tHCS	Hold Time for Chip Select	–	2	–	2.5	–	2.5	–	ns
tHA	Hold Time for Address	–	2	–	2.5	–	2.5	–	ns
tDH	Data Hold from Clock Low	–	2	–	2	–	2	–	ns
tDR	Data Ready from Clock Low	–	0	5	0	5	0	5	ns

2771 tbl 11

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Access time is the larger of tACC or tWH + tDR.

READ CYCLE TIMING DIAGRAM



2771 drw 09

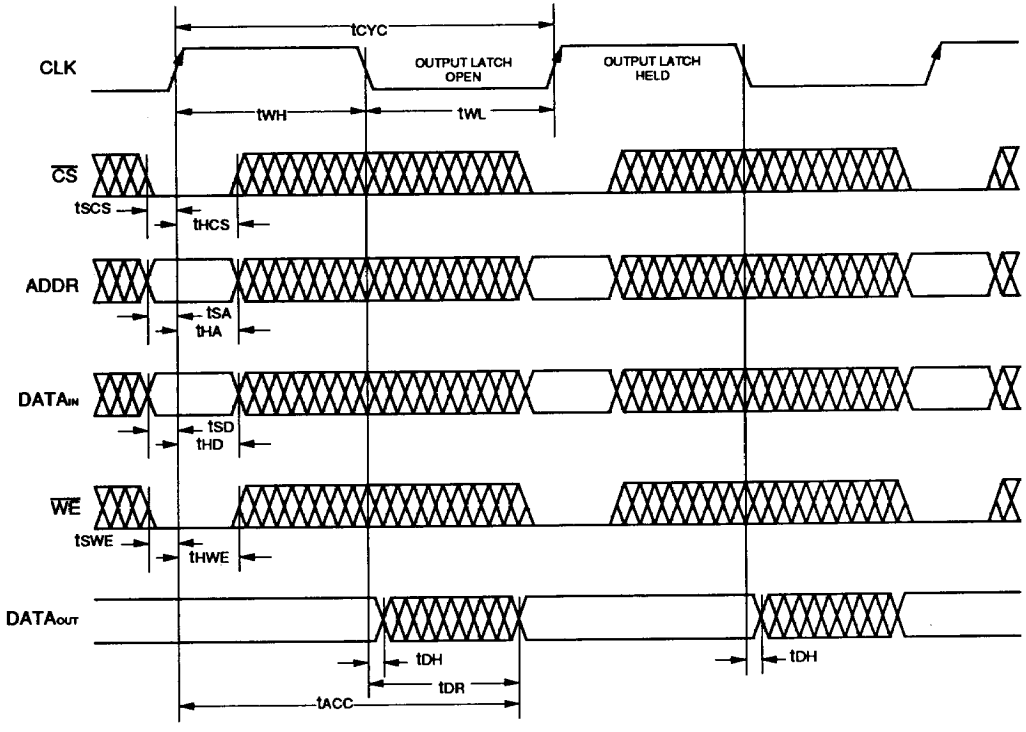
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496RL10 100496RL10 101496RL10		10496RL12 100496RL12 101496RL12		10496RL15 100496RL15 101496RL15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle[2]									
tSWE	Setup Time for Write Enable	–	1	–	1	–	1	–	ns
tSD	Setup Time for Data In	–	1	–	1	–	1	–	ns
tHWE	Hold Time for Write Enable	–	2	–	2.5	–	2.5	–	ns
tHD	Hold Time for Data In	–	2	–	2.5	–	2.5	–	ns

2771 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and Access timing are the same as the Read Cycle with the addition of above requirements. Write Data appears on output pins after falling edge of clock.

WRITE CYCLE TIMING DIAGRAM



2771 drw 10

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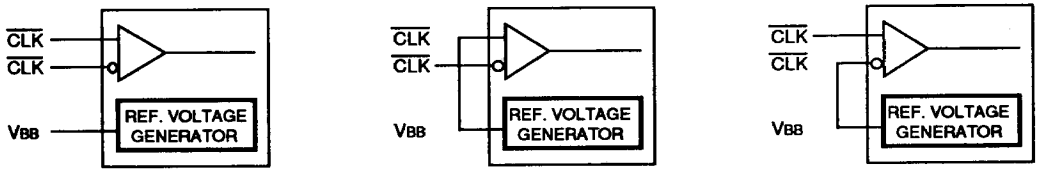
CLOCK INPUT

The clock input circuit has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better common-mode noise rejection and is obtained by driving both true and complement clock lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising-edge-active, as shown in Figures (b) and (c), respectively. VBB is designed to drive clock input only and is not intended to be used for any other purpose.



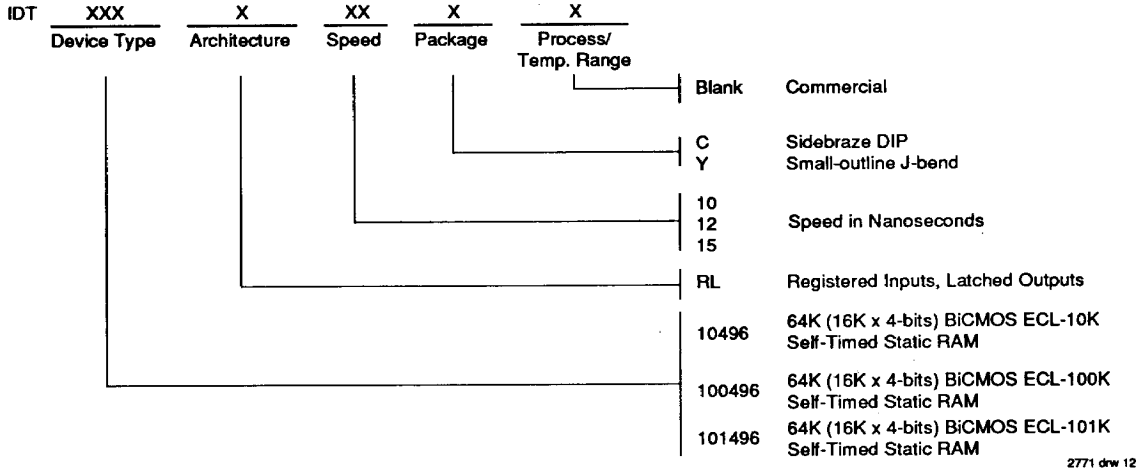
(a) Differential Mode

(b) Falling-Edge-Active Single-Ended Mode

(c) Rising-Edge-Active Single-Ended Mode

2771 drw 11

ORDERING INFORMATION



2771 drw 12