



Integrated Device Technology, Inc.

# BiCMOS STATIC RAM 64K (8K x 8-BIT)

IDT71B64

### FEATURES:

- 8K x 8 organization
- JEDEC standard 28-pin DIP and SOJ
- Fast access time and cycle time  
— Commercial: 8/10/12 (max.)
- Produced with advanced BiCMOS high-performance technology
- Bidirectional inputs and outputs directly TTL compatible

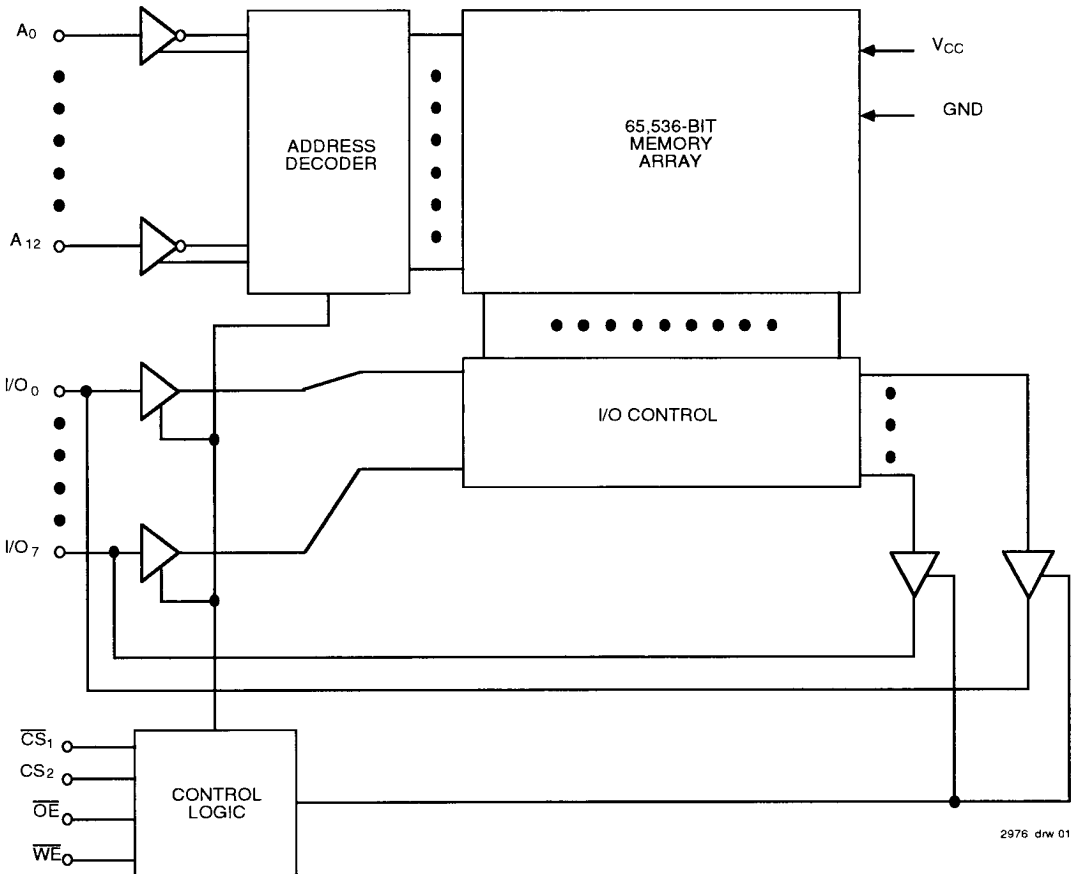
### DESCRIPTION:

The IDT71B64 is a 65,536-bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability BiCMOS technology.

The IDT71B64 offers address access times as fast as 8ns. All inputs and outputs of the IDT71B64 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

The IDT71B64 is packaged in JEDEC standard 300-mil 28-pin plastic DIP and SOJ packages.

### FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

**COMMERCIAL TEMPERATURE RANGE**

**AUGUST 1992**

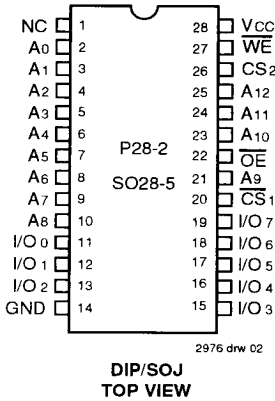
©1992 Integrated Device Technology, Inc.

6.9-1

DSC-1071/2

1

PIN CONFIGURATIONS



DIP/SOJ  
TOP VIEW

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

- NOTE:** 2976 tbl 02
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
  - VTERM must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

- NOTE:** 2976 tbl 03
- This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE<sup>(1,2)</sup>

INPUTS				I/O	FUNCTION
WE	CS1	CS2	OE		
X	H	X	X	High-Z	Deselected-Standby (ISB)
X	VHC <sup>(3)</sup>	X	X	High-Z	Deselected-Standby (ISB1)
X	X	L	X	High-Z	Deselected-Standby (ISB)
X	X	VLC <sup>(3)</sup>	X	High-Z	Deselected-Standby (ISB1)
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

- NOTES:** 2976 tbl 01
- H = VIH, L = VIL, X = Don't care.
  - VLC = 0.2V, VHC = Vcc - 0.2V.
  - Other inputs ≥ VHC or ≤ VLC.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%

2976 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

- NOTE:** 2976 tbl 04
- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

6

**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$ )

Symbol	Parameter	71B64S8 <sup>(3)</sup>	71B64S10	71B64S12	Unit
		Com'l.	Com'l.	Com'l.	
ICC	Dynamic Operating Current, $CS_2 \geq V_{IH}$ and $CS_1 \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	180	170	170	mA
ISB	Standby Power Supply Current (TTL Level) $CS_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	50	50	50	mA
ISB1	Full Standby Power Supply Current (CMOS Level) $CS_1 \geq V_{HC}$ or $CS_2 \leq V_{LC}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = 0^{(2)}$ , $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	20	20	20	mA

**NOTES:**

1. All values are maximum guaranteed values.
2.  $f_{MAX} = 1/t_{RC}$  (all address inputs are cycling at  $f_{MAX}$ );  $f = 0$  means no address input lines are changing.
3. Preliminary only.

2896 tbl 05

**AC TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 and 3

2976 tbl 06

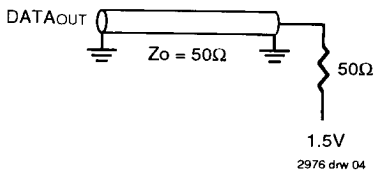
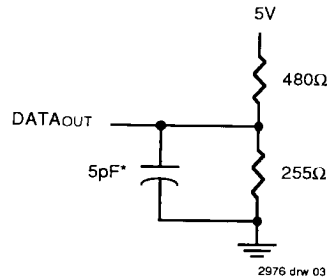


Figure 1. AC Test Load



\*Includes jig and scope capacitance.

Figure 2. AC Test Load  
 (for tCLZ 1,2, tOLZ, tCHZ 1, 2, tOHZ, tWHZ, tOW)

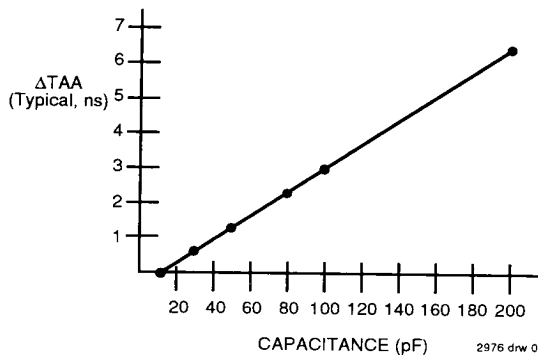


Figure 3. Lumped Capacitive Load, Typical Derating

### DC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B64S		Unit
			Min.	Max.	
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	—	5	μA
I <sub>ILO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS}_1 = V_{IH}$ , $CS_2 = V_{IL}$ , V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	5	μA
VOL	Output LOW Voltage	I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.	—	0.5	V
		I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	0.4	V
VOH	Output HIGH Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	V

2976 tbl 07

### AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.0V ± 10%, Commercial Temperature Ranges)

Symbol	Parameter	71B64S8 <sup>(3)</sup>		71B64S10		71B64S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
t <sub>RC</sub>	Read Cycle Time	8	—	10	—	12	—	ns
t <sub>AA</sub>	Address Access Time	—	8	—	10	—	12	ns
t <sub>ACS1,2</sub>	Chip Select-1, 2 Access Time <sup>(1)</sup>	—	8	—	10	—	12	ns
t <sub>CLZ1,2<sup>(2)</sup></sub>	Chip Select-1, 2 to Output in Low-Z	2	—	2	—	2	—	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	4	—	5	—	6	ns
t <sub>OLZ<sup>(2)</sup></sub>	Output Enable to Output in Low-Z <sup>(2)</sup>	2	—	2	—	2	—	ns
t <sub>CHZ1,2<sup>(2)</sup></sub>	Chip Deselect-1, 2 to Output in High-Z <sup>(2)</sup>	—	4	—	5	—	6	ns
t <sub>OHZ<sup>(2)</sup></sub>	Output Disable to Output in High-Z <sup>(2)</sup>	—	4	—	4	—	5	ns
t <sub>OH</sub>	Output Hold from Address Change	2	—	2	—	3	—	ns
t <sub>PU<sup>(2)</sup></sub>	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t <sub>PD<sup>(2)</sup></sub>	Chip Deselect to Power-Up Time	—	8	—	10	—	12	ns
<b>Write Cycle</b>								
t <sub>WC</sub>	Write Cycle Time	8	—	10	—	12	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	7	—	8	—	10	—	ns
t <sub>CW1</sub>	Chip Select to End-of-Write ( $\overline{CS}_1$ )	7	—	8	—	10	—	ns
t <sub>CW2</sub>	Chip Select to End-of-Write (CS2)	7	—	7	—	9	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	7	—	7	—	9	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>WHZ<sup>(2)</sup></sub>	Write Enable to Output in High-Z <sup>(2)</sup>	—	4	—	5	—	6	ns
t <sub>DW</sub>	Data Valid to End-of-Write	5	—	5	—	6	—	ns
t <sub>DH</sub>	Data Hold from Write Time	0	—	0	—	0	—	ns
t <sub>OW<sup>(2)</sup></sub>	Output Active from End-of-Write <sup>(2)</sup>	2	—	2	—	2	—	ns

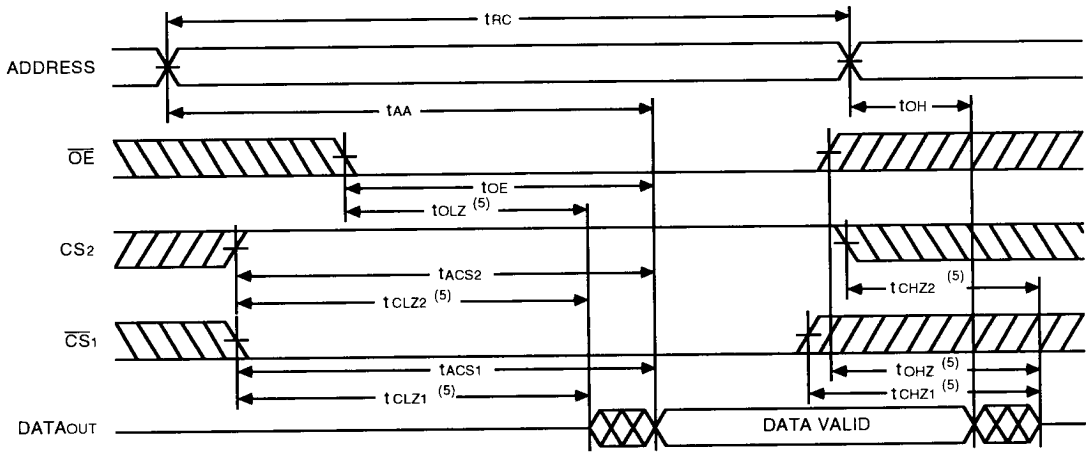
**NOTES:**

- Both chip selects must be active for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.
- Preliminary only.

2976 tbl 08

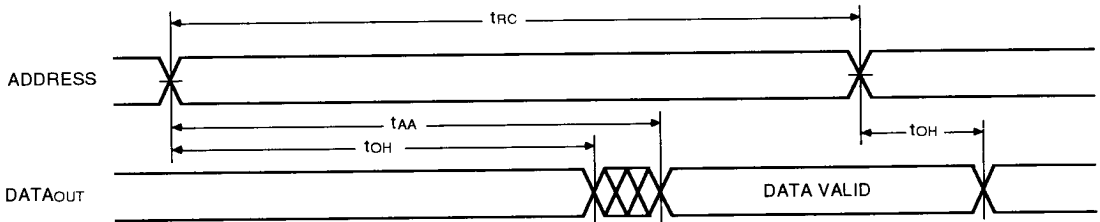


**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



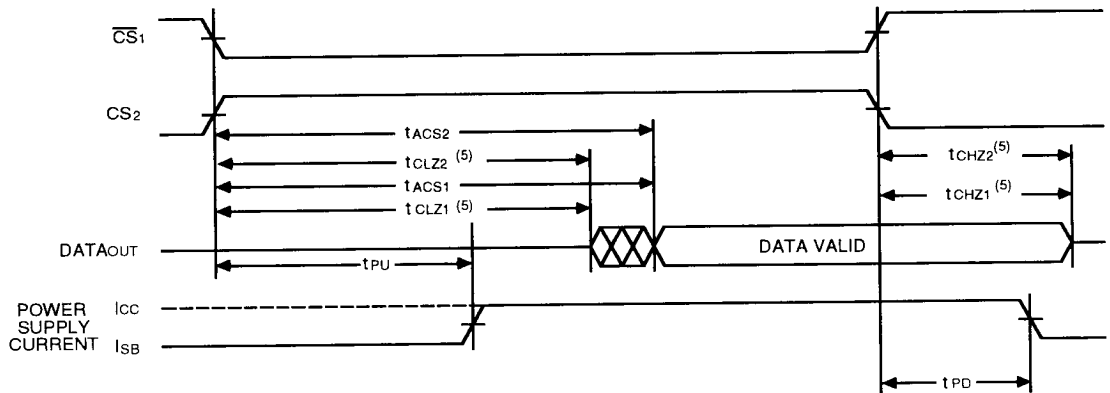
2976 drw 06

**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>**



2976 drw 07

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>**

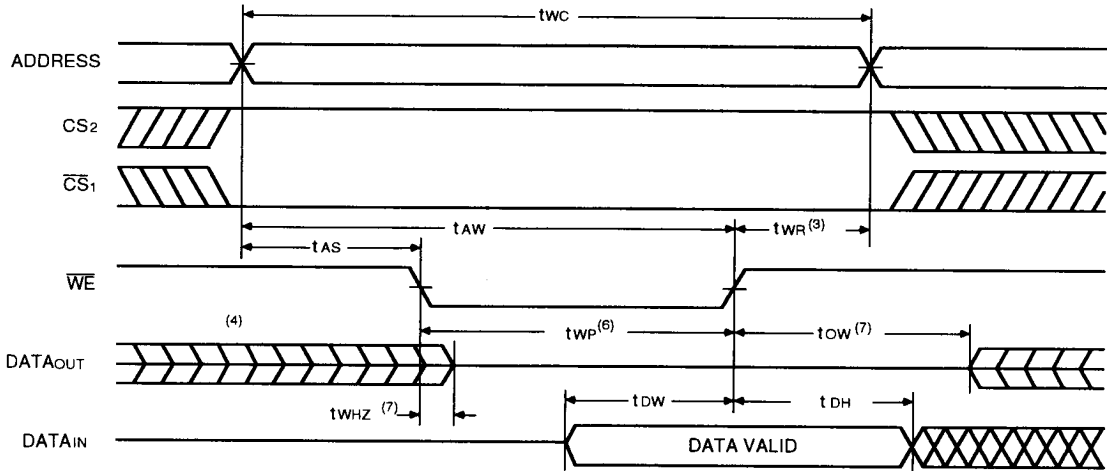


2976 drw 08

**NOTES:**

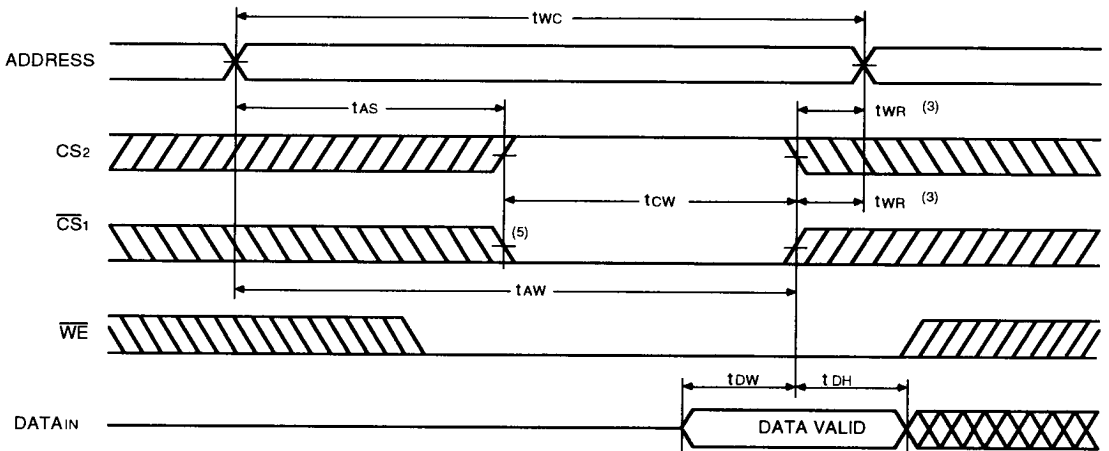
1. WE is HIGH for read cycle.
2. Device is continuously selected, CS1 = VIL, CS2 = VIH.
3. Address valid prior to or coincident with CS1 transition LOW and CS2 transition HIGH.
4. OE is LOW.
5. Transition is measured ±200mV from steady state.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1, 2, 6)</sup>**



2976 drw 09

**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1, 2)</sup>**

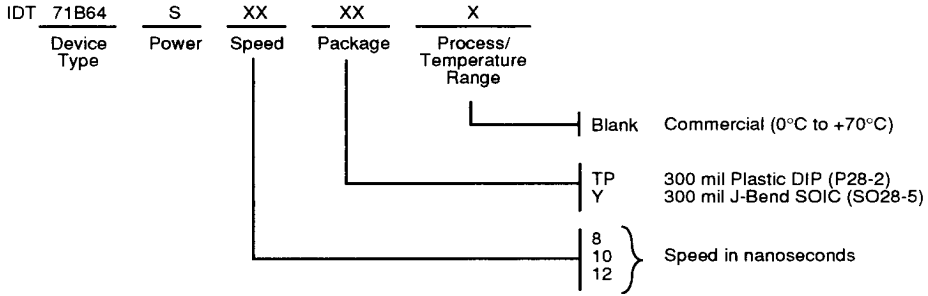


2976 drw 10

- NOTES:**
1.  $\overline{WE}$ ,  $\overline{CS1}$  or  $CS2$  must be inactive during all address transitions.
  2. A write occurs during the overlap of a LOW  $\overline{WE}$ , a LOW  $\overline{CS1}$  and a HIGH  $CS2$ .
  3.  $tWR1, 2$  is measured from the earlier of  $\overline{CS1}$  or  $\overline{WE}$  going HIGH or  $CS2$  going LOW to the end of the write cycle.
  4. During this period, I/O pins are in the output state so that the input signals must not be applied.
  5. If the  $\overline{CS1}$  LOW transition or  $CS2$  HIGH transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
  6.  $\overline{OE}$  is continuously HIGH. If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be greater than or equal to  $tWHZ + tOW$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $tWP$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified  $tWP$ .
  7. Transition is measured  $\pm 200mV$  from steady state.

6

**ORDERING INFORMATION**



2976 drw 11