IMI145152 FREQUENCY SYNTHESIZER

CMOS LSI

February 1996 ***PARALLEL TUNING PLL FREQUENCY SYNTHESIZER***

PRODUCT DESCRIPTION

The IMI145152 is a member of a family of phase lock loop synthesizer Ics from International Microcicruicts. This part is pin-for-pin compatible with the Motorola MC145152 series of parts. The IMI145152 is an improved version of this device, and designing to take advantage of these improvements will provide a synthesizer with noticeably improved performance.

The IMI145152 is programmed with parallel input data lines. Since it does not require a microcontroller as serial and bus programming units do, the IMI145152 is an excellent choice for synthesizers requiring independence from digital controllers. Such applications particularly include fixed local oscillator signals, who tuning never changes, and signal sources, which have few operating frequencies.

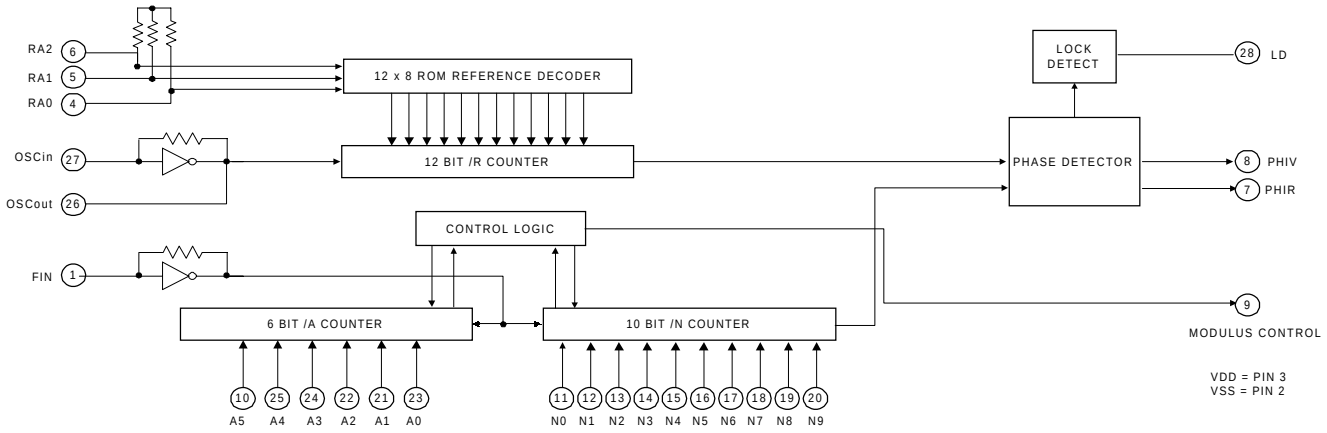
Blocks in the IMI145152 include a dual modulus feedback divider for use with an external dual modulus prescaler. Prescaler ratios can very from 3/4 through 64/65. The reference divider is set by three select lines to one of eight ROM encloded values. Both counter inputs are biased for high sensitivity to sinewave input signals, and the reference divider input is also configured to operate as an oscillator if desired. The phase detector is a Type IV phase-frequency design, which has inherently eliminated the dead zone and indeed any crossover distortion, as is often noticed on other PLL devices.

Performance improvements are in the operating bandwidth and phase detector noise floor. With its extremely low phase noise floor and wider input bandwidth, prescaler ratios can be minimized to allow wide loop bandwidths for faster settlign and lower phase noise.

PRODUCT FEATURES

- > 150 Mhz typical input frequency
- -163 dBc/Hz total phaswe noise floor
- No dead zone, by design
- Unambiguous PLL acquisition
- Parrallel programming, dual modulus PLL
- 8 user-selectable reference divider ratios: 8, 64, 128, 256, 512, 1024, 1160, and 2048
- Lock detect signal
- Compatible with dual-modulus prescalers from ÷3/4 to ÷64/65
- 10-bit N counter, 6-bit A counter
- On- or off-chip reference oscillator operation
- 3-volt and 5-volt characterizations

BLOCK DIAGRAM



Note: N0 through N9 have pullup resistors not shown.

INTERNATIONAL MICROCIRCUITS, INC. 525 LOS COCHES ST.
MILPITAS, CA 95035 TEL: 408-263-6300 FAX 408-263-6571

MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65°C to 150°C
Ambient Temperature:	-55°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum reated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$V_{SS} < (Vin \text{ or } Vout) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

PIN DESCRIPTIONS

PinNo.	Name	Description
1	Fin	Feedback divider input signal. Applied to both the N and A positive edge triggered counters, this signal is intended to be AC coupled. For CMOS logic level input signals, DC coupling can be used.
2	Vss	Circuit ground.
3	Vdd	Circuit positive power supply.
4 5 6	RA0 RA1 RA2	The three reference divisor ratio select pins. Pull-up resistors RA1 are included on each of these pins to insure that, if left RA2 unconnected, they will raimain at a logic ONE. The reference divider ratio is set accourding to the following table

RA2	RA1	RA0	Reference Divider Ratio
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

7	PHIR	Phase detector output. This signal goes LOW when the feedback frequency is too low.
8	PHIV	Phase detector output. This signal goes LOW when the feedback frequency is too high.
9	MC	Prescaler modulus control output signal. MC is HIGH when the prescaler is to devide by its base modulus (P). MC is LOW when the prescaler is to divide by P+1.
10	A5	MSB of the A counter programming input bits. Pull-up resistor included.
11	N0	LSB of the N counter programming input bits. Pull-up resistor included.

PIN DESCRIPTIONS (Cont.)

PinNo.	Name	Description
12	N1	LSB + 1 of the N counter programming input bits. Pull-up resistor included.
13	N2	LSB + 2 of the N counter programming input bits. Pull-up resistor included.
14	N3	LSB + 3 of the N counter programming input bits. Pull-up resistor included
15	N4	LSB + 4 of the N counter programming input bits. Pull-up resistor included
16	N5	LSB + 5 of the N counter programming input bits. Pull-up resistor included
17	N6	LSB + 6 of the N counter programming input bits. Pull-up resistor included
18	N7	LSB + 7 of the N counter programming input bits. Pull-up resistor included
19	N8	LSB + 8 of the N counter programming input bits. Pull-up resistor included
20	N9	MSB of the N counter programming input bits. Pull-up resistor included
21	A1	LSB + 1 of the A counter programming input bits. Pull-up resistor included
22	A2	LSB + 2 of the A counter programming input bits. Pull-up resistor included
23	A0	LSB of the A counter programming input bits. Pull-up resistor included
24	A3	LSB + 3 of the A counter programming input bits. Pull-up resistor included
25	A4	LSB + 4 of the A counter programming input bits. Pull-up resistor included
26	OSCout	Reference signal output or output of the oscilator inverter.
27	OSCin	AC-coupled reference signal input or input to the oscillator inverter.
28	LD	Lock detect output. When the PLL is locked, this signal will be essentially HIGH, with very narrow negative spikes at the phase detection frequency. If the PLL is out of lock, this signal will pulse LOW.

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PLL OPERATING CHARACTERISTICS

VDD = 5 VOLTS

Characteristics		Symbol		-40ºC		0ºC		25ºC			70ºC		85ºC		Unit	Conditions
				Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max		
Dynamic	Operating Frequency	fin,	Sine	180	-	170	-	160	180	-	150	-	140	-	Mhz	
			Square	180	-	170	-	160	200	-	150	-	140	-	Mhz	
		fosc													Mhz	
	Modulus Control Prop. Dealy	Mcpd		-	6.5	-	7	-	6.8	7.5	-	8	-	8	ns	
	Synthesizer Phase Noise Floor	PDNF							-160						dBc/ Hz	
	Pin Capacitance	Cin		-	10			-	6	10			-	10	pF	
		Cout		-	10			-	6	10			-	10	pF	
Static	Input Voltages	VIL		1	1.5	-	1.5	-	2.75	1.5	-	1.5	-	1.5	Vdc	
		VIH		3.5	-	3.5	-	3.5	2.75	-	3.5	-	3.5	-		
	Output Voltages	VOL		-	0.05	-	0.05	-	0.0	0.05	-	.05	-	0.05	Vdc	
		VOH		4.95	-	4.95	-	4.95	5.0	-	4.95	-	4.95	-		
	Output Current	IOL	Logic	2.4	-			2.0	2.8	-			1.6	-	mA	
			OSCout	1.2	-			2.0	1.4	-			0.8	-		VOL = 0.40
		IOH	Logic	-2.4	-			-2.0	-2.8	-			-1.6	-	mA	VOH = 4.0
			OSCout	-1.2	-			-1.0	-1.4	-			-0.8	-	mA	VOH = 4.0
	Supply Currents	IDD													mA	fosc=fin=10 MHz
		ISB		-	150			-	40	150			-	150	uA	fosc=fin=0
		IPU							50						uA	VIL = 0

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PLL OPERATING CHARACTERISTICS

VDD = 3 VOLTS

Characteristics		Symbol		-40ºC		0ºC		25ºC			70ºC		85ºC		Unit	Conditions
				Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max		
Dynamic	Operating Frequency	fin,	Sine	140	-	130	-	130	140	-	120	-	110	-	Mhz	
			Square	140	-	130	-	130	150	-	120	-	110	-	Mhz	
		fosc													Mhz	
	Modulus Control Prop. Dealy	Mcpd		-	10	-	10.5	-	10.5	11	-	12	-	12.5	ns	
	Synthesizer Phase Noise Floor	PDNF							-155						dBc/ Hz	
	Pin Capacitance	Cin		-	10			-	6	10			-	10	pF	
		Cout		-	10			-	6	10			-	10	pF	
Static	Input Voltages	VIL		-	0.9			-	1.35	0.9			-	0.9	Vdc	
		VIH		2.1	-			2.1	1.65	-			2.1	-		
	Output Voltages	VOL		-	0.05	-	0.05	-	0.0	0.05	-	0.05	-	0.05	Vdc	
		VOH		2.95	-	2.95	-	2.95	3.0	-	2.95	-	2.95	-		
	Output Current	IOL	Logic	1.6	-			1.4	2.0	-			0.8	-	mA	
			OSCout	0.8	-			0.7	1.0	-			0.4	-		VOL = 0.30
		IOH	Logic	-1.6	-			-1.4	-2.0	-			-0.8	-	mA	VOH=2.4
			OSCout	-0.8	-			-0.7	-1.0	-			-0.4	-	mA	VOH = 2.4
	Supply Currents	IDD													mA	fosc=fin=10 MHz
		ISB		-	150			-	40	150			-	150	uA	fosc=fin=0
		IPU							30						uA	VIL = 0

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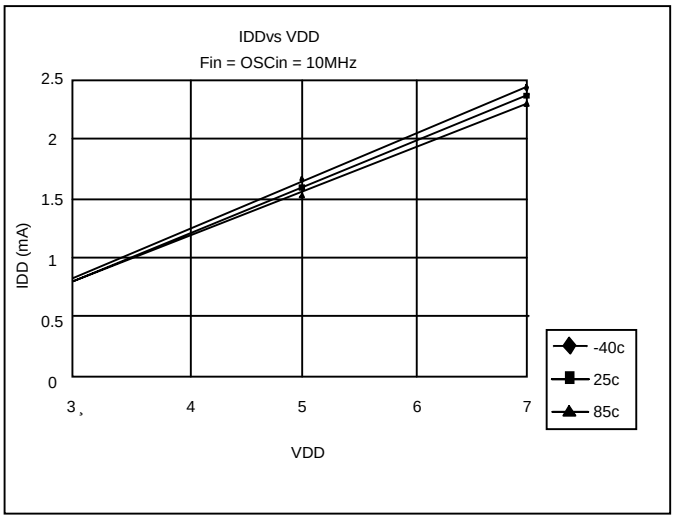
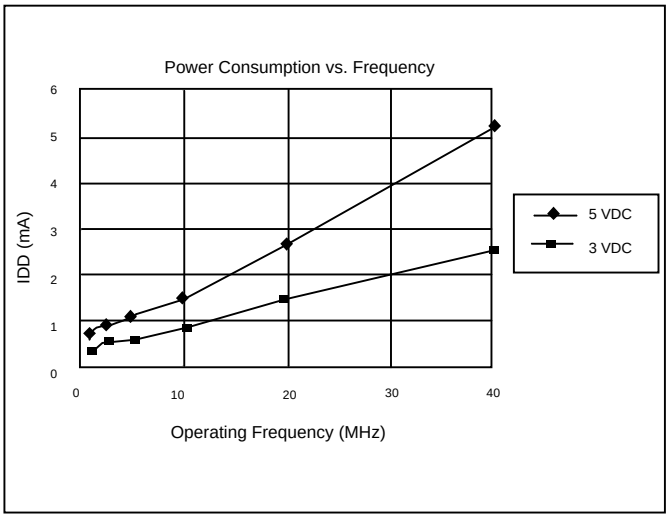
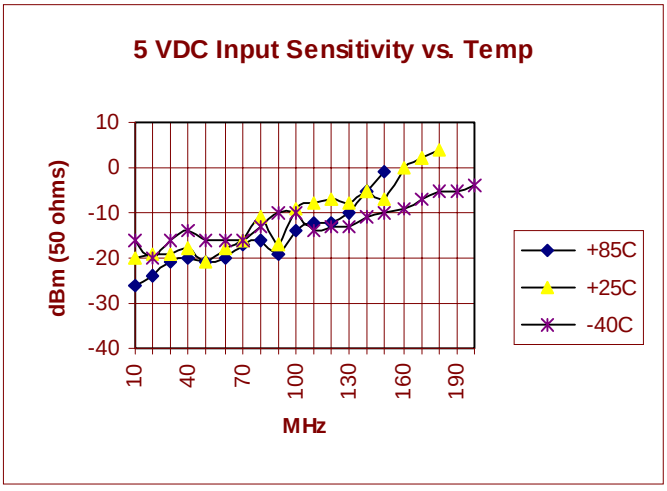
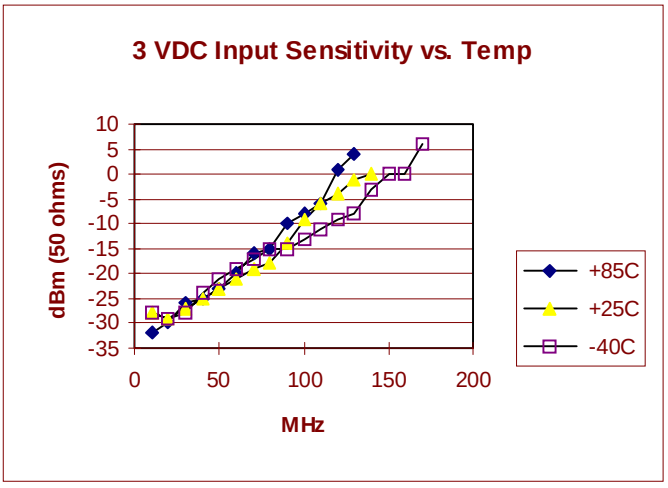
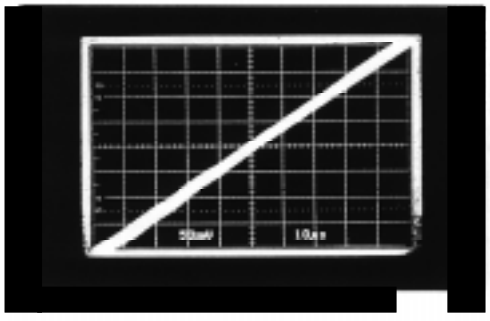




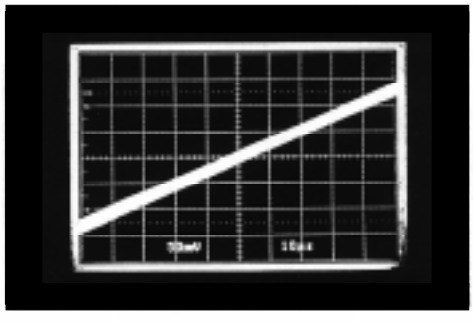




PD LINEARITY 5 VOLTS



PD LINEARITY 3 VOLTS



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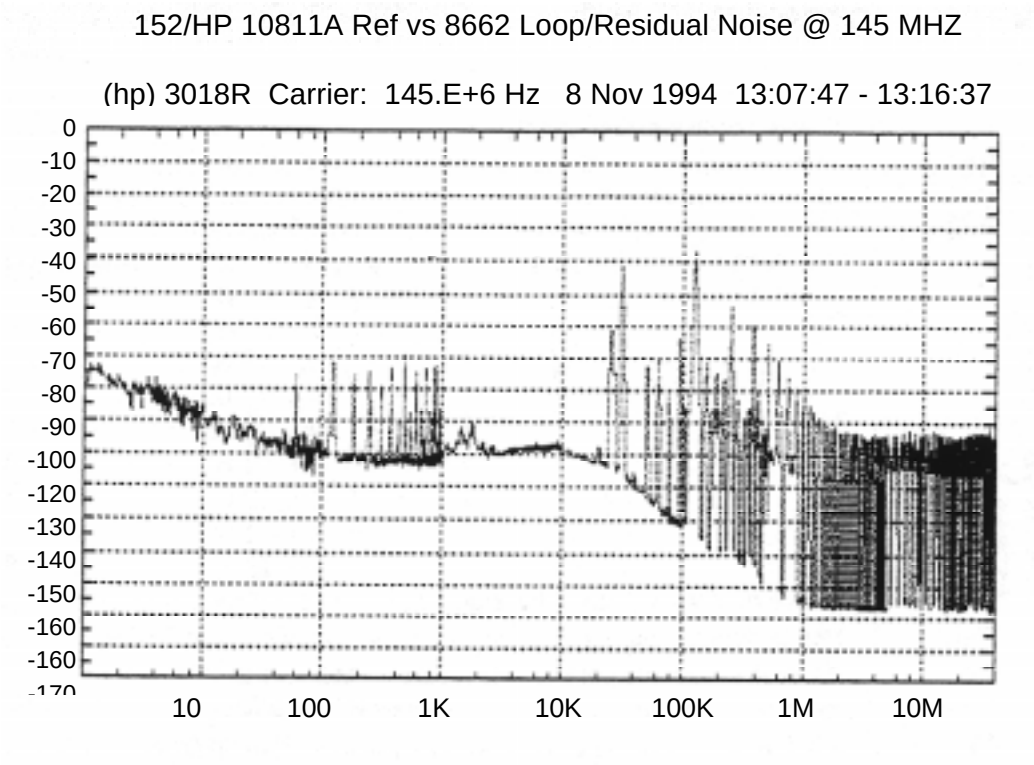
PHASE NOISE FLOOR



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DUAL MODULUS PRESCALING

Dual modulus prescaling is a widespread method used to effectively extend the operating frequency of a digital counter without sacrificing any frequency resolution. The key to understanding ths method is to remember the basics of division: When any two integers are divided, a quotient and a remainder will result.

When used here in a PLL, the numerator of this division is the required PLL total feedback divider ratio, called N_{tot}. The denominator is the base modulus of the dual modulus prescaler, P. The quotient is applied idrectly to the N counter, and the remainder is applied directly to the A counter. Both counters count down together toward zero. While the A counter counts, the MC (modulus control) output signal is LOW, setting the prescaler to divide by P+1. When the A counter reaches zero, the MC output is set HIGH while the N counter reaches zero, both counters are reset to theprogrammed inputs and the cycle is repeated.

Two particular things should be noticed about this process. First, the remainder counts are spread among an equal number of quotient counts by the use of the prescaler modulus P+1. When the remainder has been counted, any remaining quotient counts are handled normally by prescaling with modulus P. This counter is thus performing

$$Ntot = A(P+1) + (N-A)P$$

Some algebra on this relation yields

$$Ntot = AP + A + NP - AP$$
$$Ntot = NP + A$$

which is just the definition of integer division. Second, for this to work, there must be more quotient ocunts than remainder counts for all possible values of N_{tot} in the synthesizer desing. If this wer enot true, then the N counter will reach zero and the cause the entire divider to be reset before the A counter is finished. there is a minimum value for N_{tot} for which this requirement will always hold: $N_{tot} > P^2 - 2$.

PROGRAMMING GUIDELINES APPLICABLE TO THE IMI145152

The system total divide value (Ntotal) will be dictated by the application:

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N*P + A$$

N is the number programmed in the ÷ N counter; A is the number programmed into ÷ A counter. P and P + ! are two selectable divide ratios available in the two modulus prescaler. To have a range of Ntotal values in sequence, the ÷ A counter is programmed from zero through P-1 for a particular value N in the N counter. N is then incremented to N + !, and the ÷ A is sequenced from zero through P-1 again.

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P + !. input cycles. The prescaler should divide by P when its modulus control line is high, and by P + 1 when its modulus control is low.

A. Fvco max divided by P may not exceed the frequency capability of Pin 1 of the IMI145152.
B. The period of Fvco divided by P must be greater than the sum of the times:
    a. Propagation delay through the dual modulus prescaler.
    b. Prescaler setup or release time relative to its modulus control signal.
    c. Propagation time for Fin to the modulus control output for the IMI145152.

A usefull simplication in the IMI145152 programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the ÷ N and ÷ A counters in the following manner.

A. Assume the A counter contains "b" bits when $2^b = P$.
B. Always program all higher order ÷ A counter bits above "b" to zero.
C. Assume the ÷ N counter and ÷ A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+b bits in length. The MSB of this hypothetical counter is to correspond to the LSB of ÷ A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "new" 10+b bit counter.

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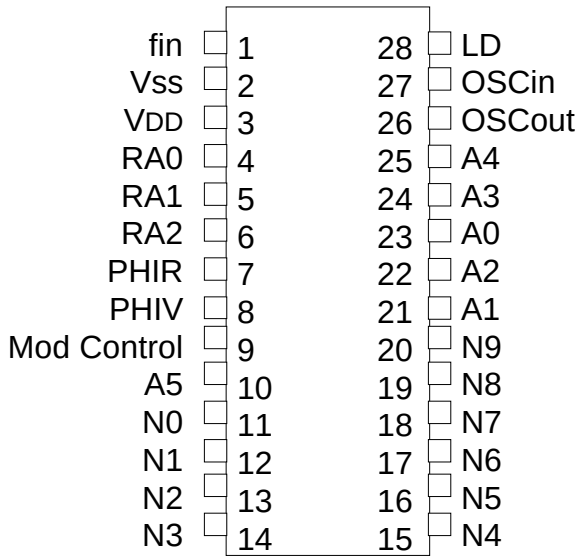
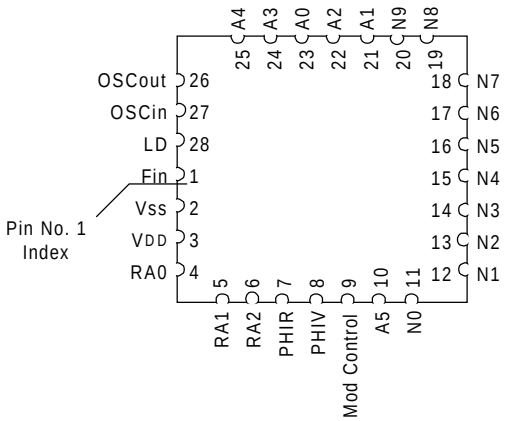
CONNECTIONS DIAGRAMS

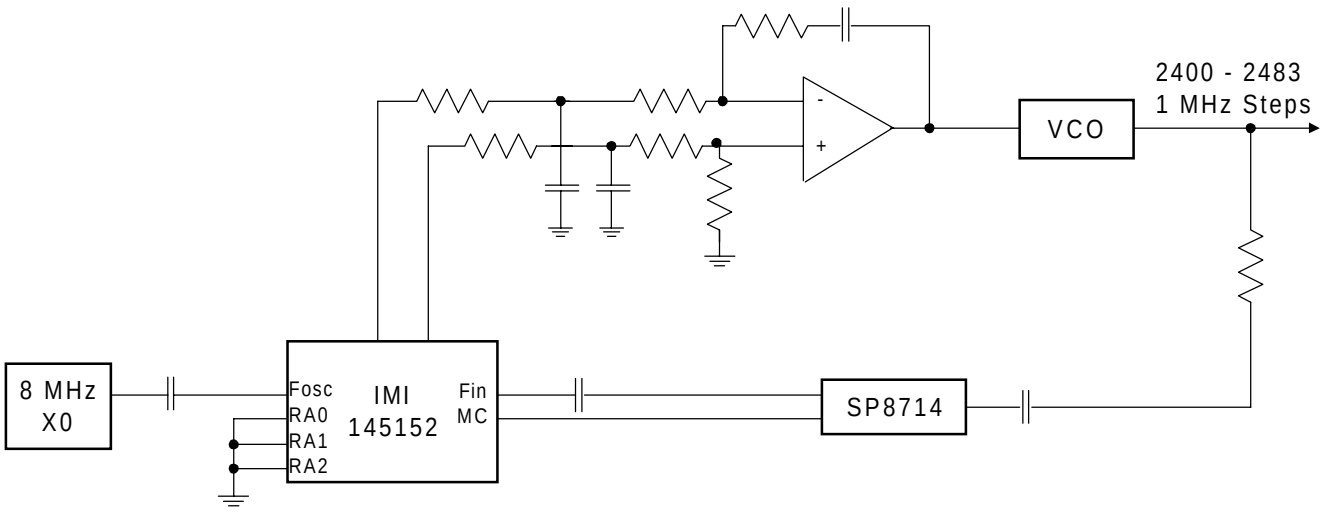
SSOP, SOIC AND PDIP PACKAGES



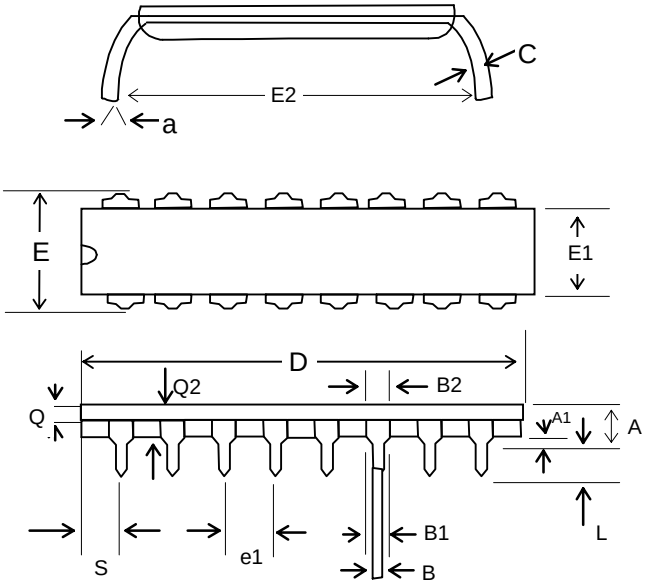
PLCC PACKAGE



TYPICAL APPLICATION CIRCUIT

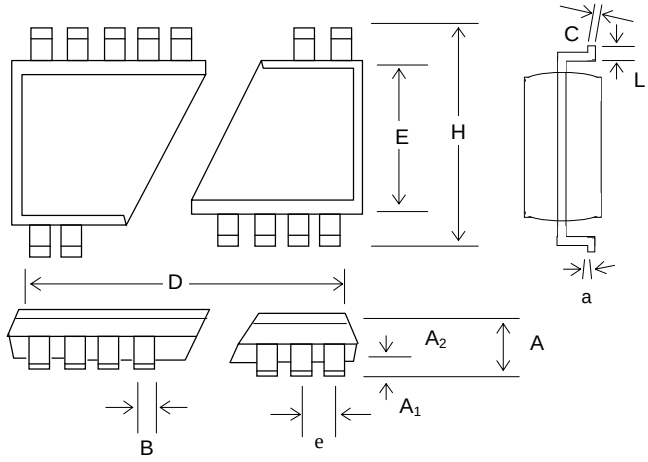


PACKAGE DRAWING AND DIMENSIONS



P-DIP

28 PIN PLASTIC DIP DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.180	-	-	4.57
A_1	0.020	-	-	0.51	-	-
B	0.015	0.0.8	0.020	0.38	0.46	0.51
B_1	0.045	0.050	0.055	1.14	1.27	1.40
B_2	0.035	0.040	0.045	0.89	1.02	1.14
C	0.008	0.010	0.012	0.20	0.25	0.30
D	1.360	1.365	1.370	34.54	34.67	34.80
E	0.300	-	0.325	7.62	-	8.255
E_1	0.280	0.282	0.284	7.11	7.16	7.2`
E_2	0.282	0.284	0.286	7.16	7.21	7.25
e_1	0.100 BSC			2.54 BSC		
L	0.128	0.130	0.135	3.18	3.30	3.43
a	0°	7°	15°	0°	7°	15°
Q_1	0.055	0.060	0.065	1.40	1.52	1.65
Q_2	-	130	-	-	3.30	-
S	0.028	0.033	0.038	0.71	0.84	0.97



SSOP

28 PIN SSOP OUTLINE DIMENSIONS						
	MILLIMETERS			INCHES		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.08	0.073	0.078	1.73	1.8	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301`	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

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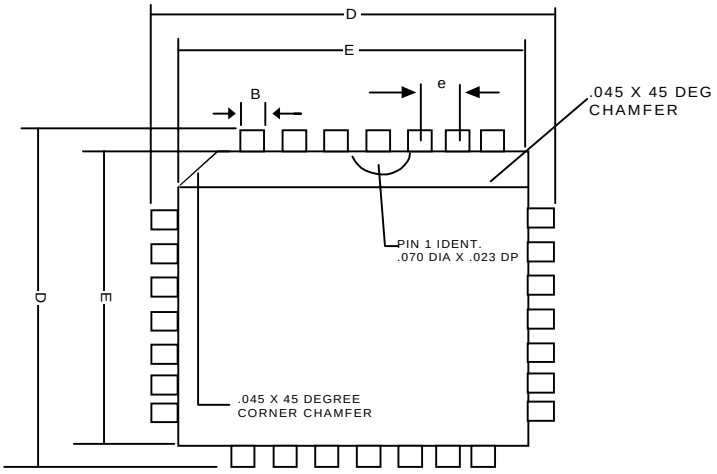
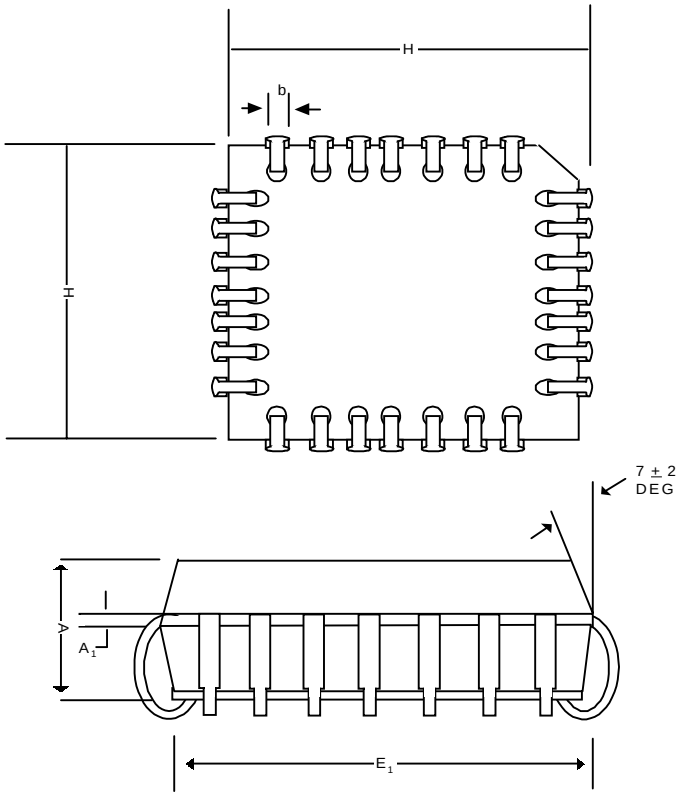
PACKAGE DRAWING AND DIMENSIONS (Cont.)



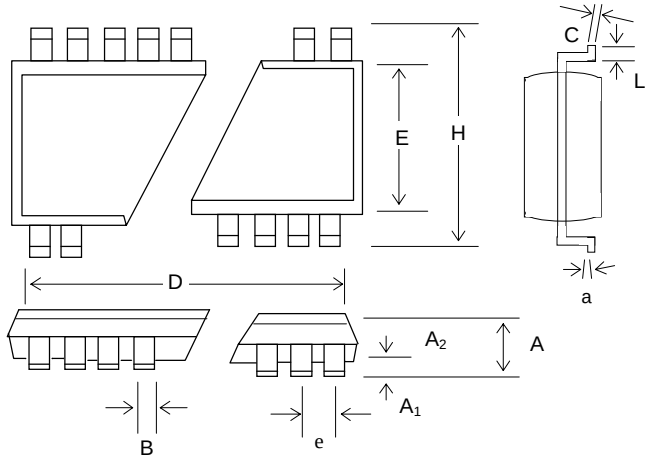
28 PIN PLCC PACKAGE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.147	0.152	0.157	3.73	3.86	3.99
A_1	.0085	.0100	.0115	0.215	0.254	0.292
B	0.026	0.029	0.032	0.660	0.736	0.813
b	0.013	0.017	0.021	0.330	0.432	0.533
D	0.485	0.490	0.495	12.32	12.44	12.57
E	0.443	0.448	0.453	11.25	11.38	11.51
E_1	0.410	0.420	0.430	10.41	10.67	10.92
e	0.048	0.050	0.052	1.22	1.27	1.32
H	0.448	0.453	0.458	11.38	11.51	11.63



PLCC

PACKAGE DRAWING AND DIMENSIONS (Cont.)



SOIC

28 PIN SOIC OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.097	0.101	0.104	2.46	2.56	2.64
A_1	0.005	0.009	0.0115	0.127	0.22	0.29
A2	0.090	0.092	0.094	2.29	2.34	2.39
B	0.014	0.016	0.019	0.35	0.41	0.48
C	0.0091	0.010	0.0125	0.23	0.25	0.32
D	0.701	0.706	0.711	17.81	17.93	18.06
E	0.292	0.296	0.299	7.42	7.52	7.59
e	.050 BSC			1.27 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0°	5°	8°	0°	5°	8°
L	0.024	0.032	0.40	0.61	0.81	1.02

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMI145152xPB	28 PIN Plastic Dip	Industrial, -40°C to + 85°C
IMI145152xXB	28 PIN SOIC	Industrial, -40°C to + 85°C
IMI145152xQB	28 PIN PLCC	Industrial, -40°C to + 85°C
IMI145152xYB	28 PIN SSOP	Industrial, -40°C to + 85°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
IMI145152xXB
Date Code, Lot #

IMISC498xXB

Flow
B = Industrial, -40°C to + 85°C

Package
P = Plastic Dip
X = SOIC
Q = PLCC
Y = SOIC

Revision

IMI Device Number

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