MC33567

Dual Linear Controller for High Current Voltage Regulation

The MC33567 Dual Linear Power Supply Controller is designed to facilitate power management for motherboard applications where reliable regulation of high current supply planes is required. It provides the Drive, Sense and Control signals to interface two external, N–channel MOSFETs for regulating two different supply planes. Undervoltage, short circuit detection places the operation of the system into a protected mode pending removal of the short.

Features

- MC33567–1: Two, Independent Regulated Supplies
  - 1.515 V – Supply for GTL and AGP Planes
  - 1.818 V – Supply for I/O Plane and Memory Termination
- MC33567–2: Dual 2.525 V Supplies for Clock and Memory
- Undervoltage Detection and Protection Mode
- Drive Capability for SOT–223, DPAK, and D^2PAK MOSFETs
- Bypass Function for 3.3 V AGP Card Detection

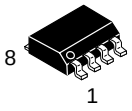
Applications

- Motherboards
- Dual Power Supplies

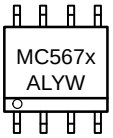
ON Semiconductor™

http://onsemi.com

MARKING DIAGRAM

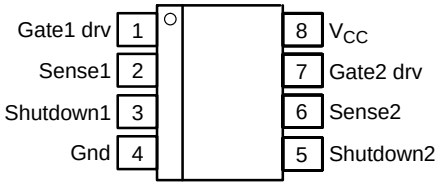


SO–8
D SUFFIX
CASE 751

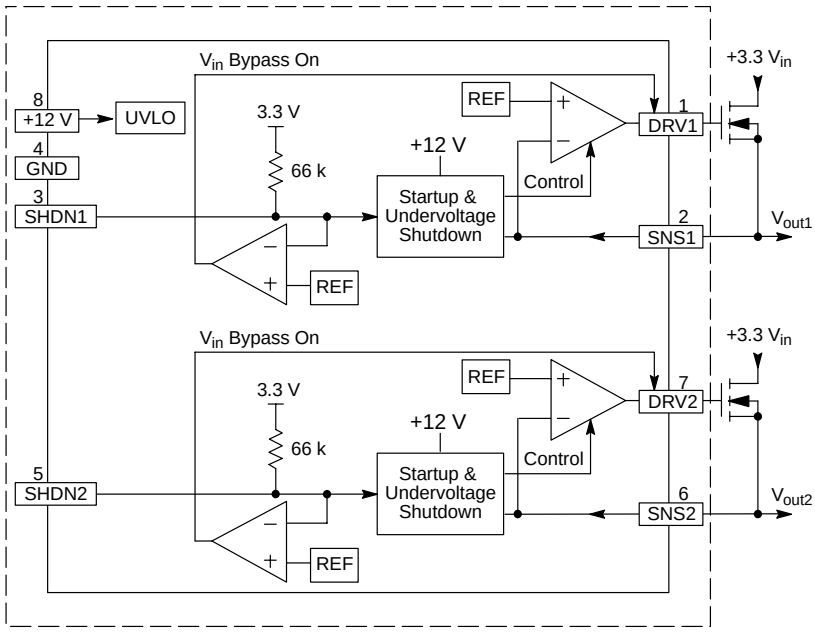


x = 1 or 2
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



Simplified Functional Block Diagram



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

MAXIMUM RATINGS*

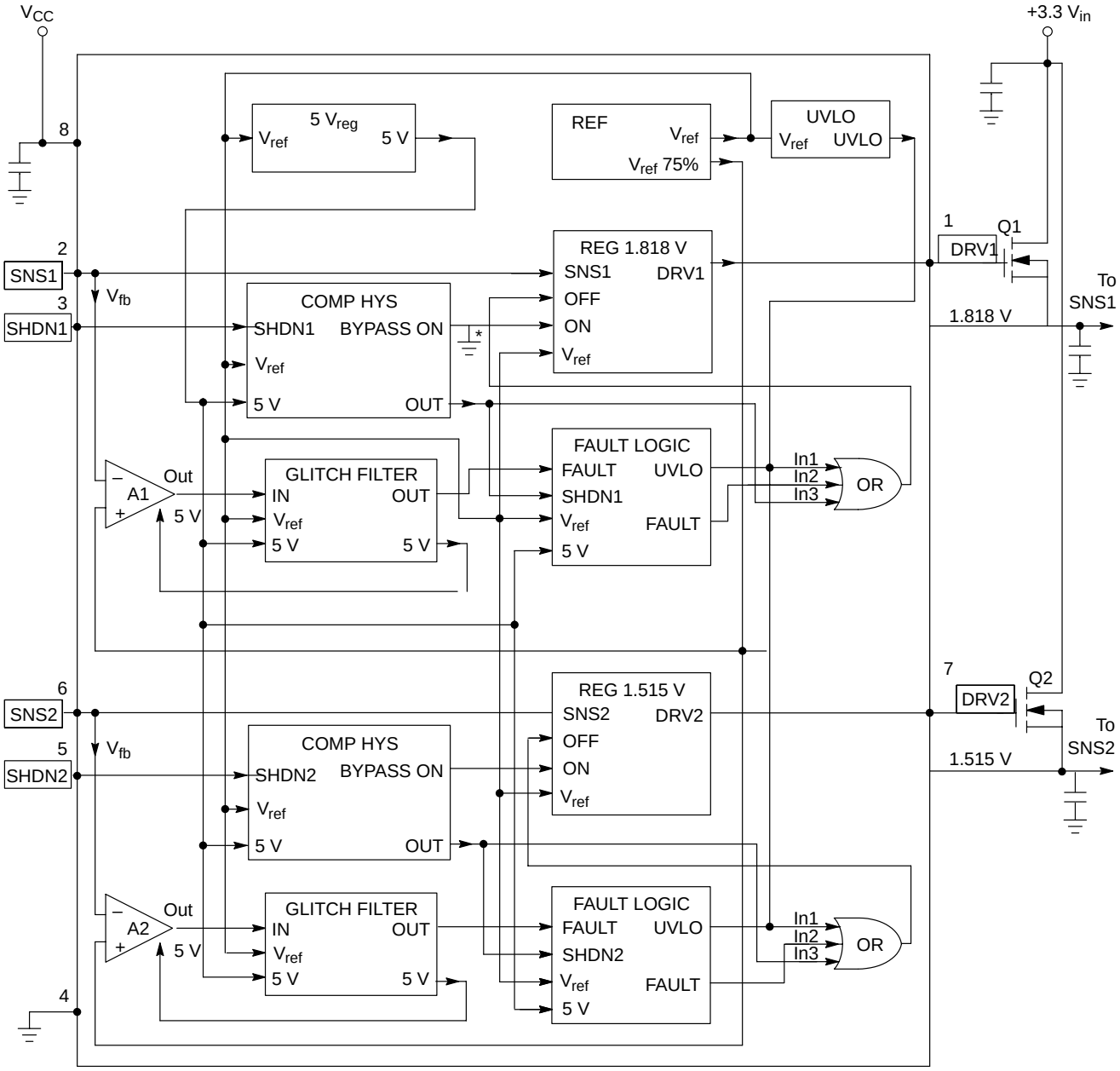
Rating	Symbol	Value	Unit
Supply Voltage	V_{cc}	12.5	Vdc
Operating Ambient Temperature	T_a	0 to +80	°C
Operating Junction Temperature	T_J	– 5 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ Note 1.	159	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	28	°C/W

1. Minimum pad test board with 5 MIL wide and 2.8 MIL thick copper traces1 inch long.

*All characterizing done with MTD3055VL N–Channel MOSFETs.

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{cc}	9.0	12	12.5	V
Quiescent Current	I_{qL} I_{qH}	– –	6.0 7.0	9.0 10	mA
UNDER VOLTAGE LOCKOUT					
Undervoltage Lockout	UVLO	7.0	8.5	9.0	V
Hysteresis	V_{hys}	0.2	0.5	0.9	V
DRIVE					
Drive Voltage (Gate to Ground)	V_{drv}	–	–	10.5	V
Gate Drive Source Output Current (Pin 1, Pin 7)	I_{pkdrv}	10	20	30	mA
Gate Drive Sink Current (Steady State)	I_{sink}	5.0	7.0	10	mA
SHUTDOWN					
Shutdown Threshold	SHDN	0.8	1.13	1.3	V
Shutdown Hysteresis	$SHDN_{hys}$	–	130	–	mV
Shutdown Disable Time	$SHDN_{tdis}$	–	0.5	2.0	μs
Shutdown Current Threshold	I_{SHDN}	–	37	–	μA
SHORT CIRCUIT					
Short Circuit Response Time	SC_{td}	–	250	–	μs
Short Circuit On Time	SC_{ton}	0.5	0.8	1.5	ms
Short Circuit Off Time	SC_{toff}	20	40	60	ms
Short Circuit/Undervoltage Detect (Load current increased until output drops)	SC_{uvd}	70	–	80	%Vout
OUTPUT REGULATION					
MC33567–1 Regulator 1 Regulator 2 MC33567–2	 V_{reg1} V_{reg2} –	 – – –	 1.818 1.515 2.525	 – – –	V
Output Voltage Regulation (Full–Load to No–Load @ 25–70°C)	$V_{reg\%}$	–2.5	–	+2.5	%



* Internal ground disables bypass on function on the 1.818 V regulator in the MC33567–1 and on the 2.525 V regulators in the MC33567–2.
A1 and A2 are undervoltage comparators.

Figure 1. Functional Block Diagram

PIN ASSIGNMENTS AND FUNCTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	Gate 1 drive	Drives MOSFET into linear region. Is internally clamped to ground in power down mode.
2	Sense 1 line	Returns regulated output from MOSFET.
3	Shutdown 1	At TTL high level turns off regulation for gate 1. Effectively grounds gate 1. (Internal pull–up to 3.3 V)
4	Ground	
5	Shutdown 2	At TTL high level turns off regulation for gate 2. Effectively grounds gate 2. (Internal pull–up to 3.3 V)
6	Sense 2 line	Returns regulated output from MOSFET.
7	Gate 2 drive	Drives MOSFET into linear region for 1.515 V operation. Saturates external FET in bypass mode. Is internally clamped to ground in power down mode.
8	12 volt input	Supply voltage for operation and gate drive output.

OPERATING DESCRIPTION

The MC33567 Dual Linear Controller is designed for power management applications where high current, voltage regulation is needed. Some computer applications include:

- 1.515 V – AGP (Advanced Graphic Port) and GTL+ (Gunning Transistor Logic – Intel's electrical bus technology)
- 1.818 V – I/O planes on motherboard
- 2.525 V – Clock and memory

Hiccup Mode

If the output drops below 75% of the regulated threshold for greater than 250 μs or a short circuit condition exists, that output will go into hiccup mode. This means that the output is turned ON for 1.0 ms and OFF for 40 ms for a duty cycle of 1:40. Please refer to Figure 2. Each transition from low to high of the input restarts the hiccup mode holdoff period. Once the short circuit is removed or the output comes back to the regulated threshold, it will operate under normal operating conditions.

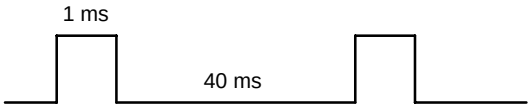
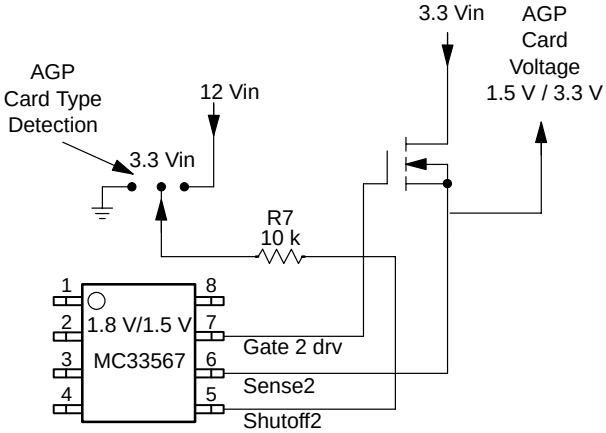


Figure 2. Hiccup Mode Duty Cycle

Shutdown

The SHUTDOWN pin is connected to the external board (AGP or GTL+). Please refer to Figure 3.



PIN 5 TRUTH TABLE
Pin 5 No connect = 1.515 V LDO drive out active
Pin 5 < 0.8V = shutdown (drive out 0 V)
1.3 V < pin 5 < 4.1 V = 1.515 V LDO drive out active
Pin 5 > 4.2 V = 3.3 V bypass mode (drive out = V_{in} for FET)

Figure 3. 1.5 V/3.3 V AGP Card Detection

The way in which the external board is wired to the shutdown pin will determine the output of the MC33567. Listed are the conditions the external board is wired and the corresponding output voltages:

1. If there is no connection on the external board, there is an open and the output will be the regulated output voltage.
2. If there is a ground on the external board which will cause the SHUTDOWN pin to be less than 0.8 V, the MOSFET turns off and there is no output voltage.
3. If there is a resistor on the external board pulling the SHUTDOWN pin above 4.1 V, the output will be in the bypass mode. In this mode, the MOSFET is fully on, or fully enhanced, and the output will be whatever voltage is supplied to the input voltage of the MOSFET, V_{in}.
4. If the SHUTDOWN pin is between 1.3 V and 4.1 V, the output will be the regulated voltage.

Tables 1 and 2 are the logic tables for the SHUTDOWN pins. Note that the logic tables are not the same for the 1.515 V regulator and the 1.818 V regulator. The MC33567–2 does not have the Full–On Bypass feature.

Table 1. Logic Table for Shutdown (Pin 5) on the 1.515 V Regulator

SHUTDOWN Pin	1.515 V Regulator Output
No Connect	1.515 V
< 0.8 V	Shutdown
1.3 V < SHDN < 4.1 V	1.515 V
> 4.2 V	V_{in} = Bypass

Table 2. Logic Table for Shutdown (Pin 3) on the 1.818 V Regulator

SHUTDOWN Pin	1.818 V Regulator Output
No Connect	1.818 V
< 0.8 V	Shutdown
> 1.3 V	1.818 V

Sense

The SENSE pins provide tight regulation of the load voltages with varying load currents. When the load is located at a distance, there will be a voltage drop due to the resistance loss of the trace. If the load is not near the MC33567, it is recommended that the SENSE pins be used. Connect the SENSE pins as close to the load as possible. Use a separate trace to connect the source of the N–Channel MOSFET to the load. Refer to Figure 4.

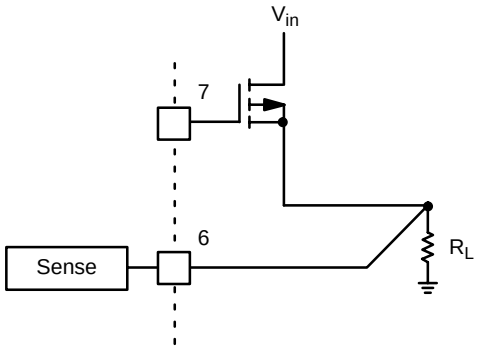


Figure 4.

Capacitor Selection

Stable operation is achieved by preserving an adequate phase margin. A rule of thumb for preserving an adequate phase margin is:

$$C \cdot R \geq 10 \times 10^{-6}$$

$$R \geq \frac{10 \times 10^{-6}}{C}$$

Where:

C = load capacitance

R = equivalent series resistance (ESR) of the capacitor

For example, if the load capacitor is 400 μF, then the ESR of the capacitor would need to be no less than 25 mΩ.

$$25\ m\Omega \geq \frac{10 \times 10^{-6}}{400\ \mu F}$$

This rule of thumb assumes that all capacitors across the load are the same type and value. If different types and values are used in parallel across the load, then each individual capacitor must meet the requirements of the given equation.

PCB Layout Guidelines

It is recommended that the MC33567 be placed as physically close as possible to the external series pass MOSFET transistors. Use short traces to minimize extraneous signals from being magnetically or electrostatically induced on the sense or drive lines. Place the sense trace and power trace in the same plane and same direction. The power trace is to be placed from the series pass transistor source lead to the load. Avoid routing the sense lead near the load current return path. Also avoid unterminated runs of the sense leads. If it is desired to have options where the sense lead is placed on the board, use 0 Ω resistor jumpers to make the alternate sense lead connection near the sense pin.

N–Channel MOSFET Selection

The ON Semiconductor MTD3055VL N–Channel MOSFET was used in the characterization of the MC33567. To select a N–Channel MOSFET the drain–source on–resistance, $R_{DS(on)}$, must be considered. For best results, $R_{DS(on)}$ needs to be low. Below is the calculation for $R_{DS(on)}$. The 0.5 in the equation is to prevent saturation and to account for tolerance build–up.

$$R_{DS(on)} \leq 0.5\ \frac{V_{in} - V_{out}}{I_{Load}}$$

Where:

V_{in} = 3.3 V typically

V_{out} = 1.515 V, 1.818 V, or 2.525 V

I_{Load} = Current at load

Select a N–channel MOSFET that has a $R_{DS(on)}$ lower than the calculated value.

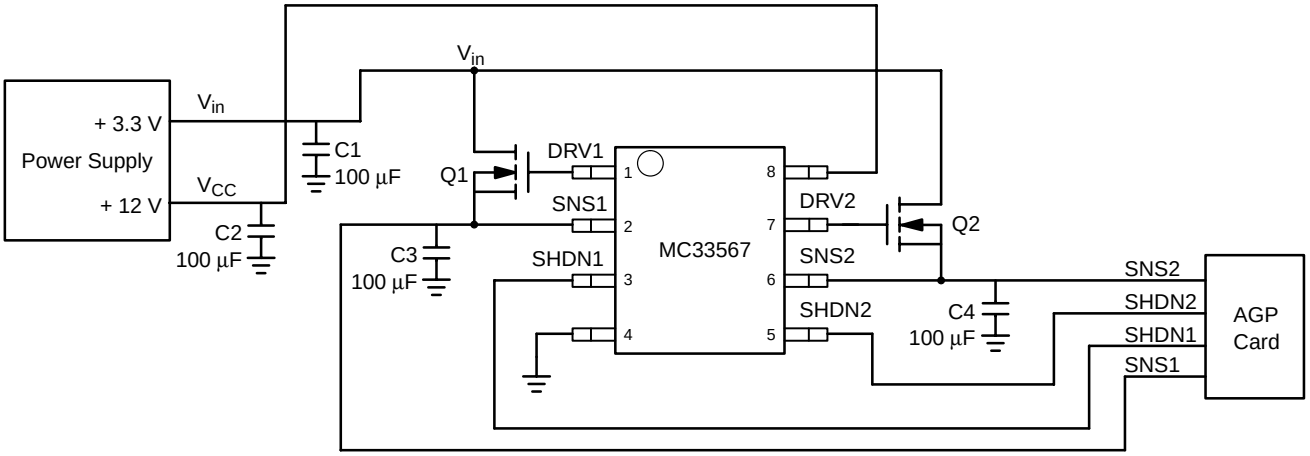


Figure 5. Application Block Diagram

Parts List

Qty	Reference	Part/Description	Vendor	Notes
4	C1, C2, C3, C4	100 µF Electrolytic Capacitor	Various	
1	U1	MC33567	ON Semiconductor	
2	Q1, Q2	MTD3055VL	ON Semiconductor	N–Channel MOSFET

MC33567 TYPICAL CHARACTERISTICS

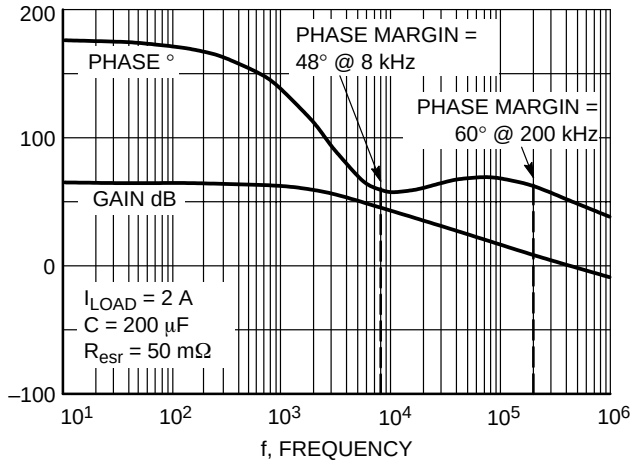


Figure 6. Gain–Phase Plot @ 50 mΩ

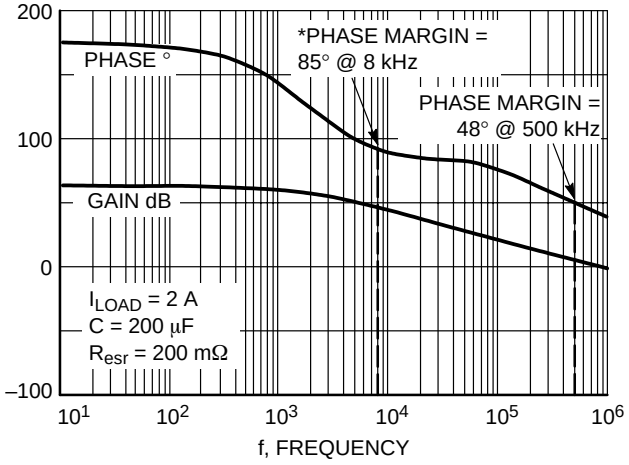


Figure 7. Gain–Phase Plot @ 200 mΩ

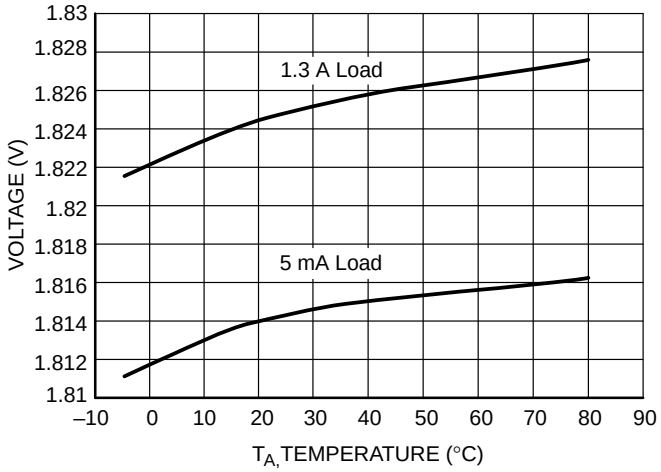


Figure 8. Regulator 1 Load Regulation vs. Temperature Gate Drive 2 Open

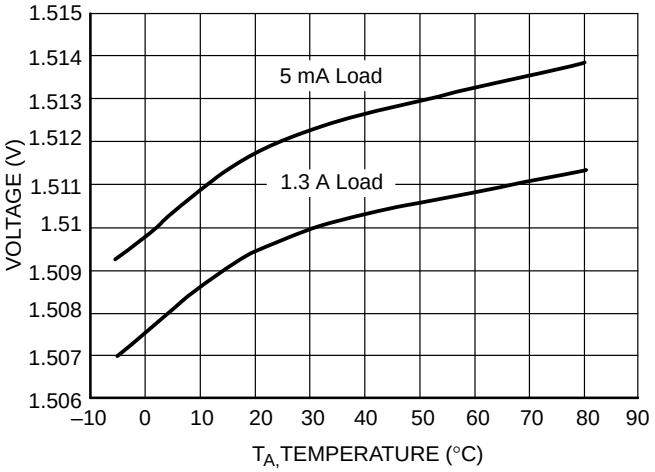


Figure 9. Regulator 2 Load Regulation vs. Temperature Gate Drive 1 is Open

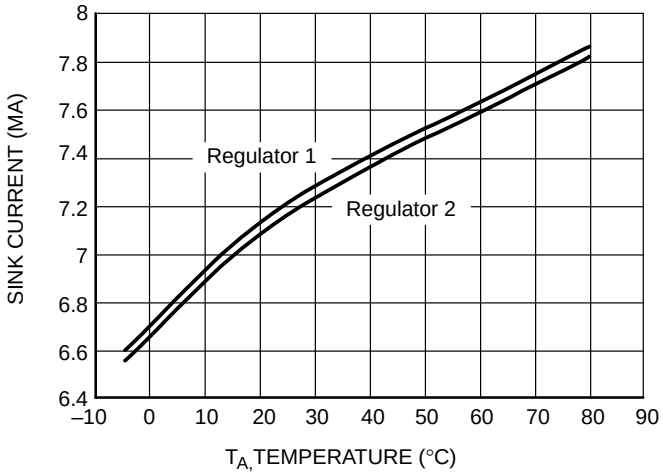


Figure 10. Gate Drive Sink Current vs. Temperature

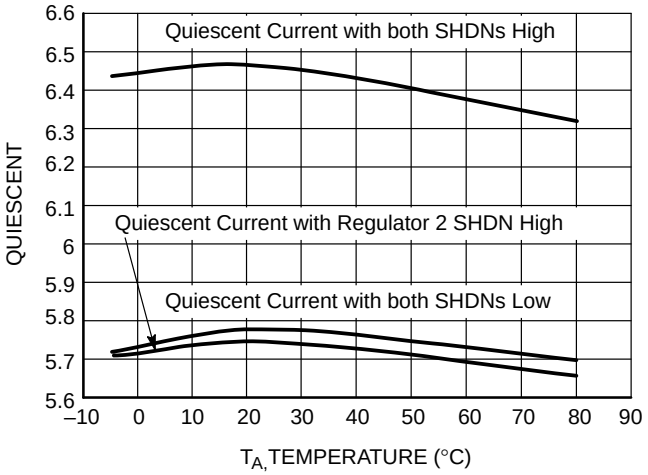


Figure 11. SHDN Quiescent Current vs. Temperature 50 mA Load

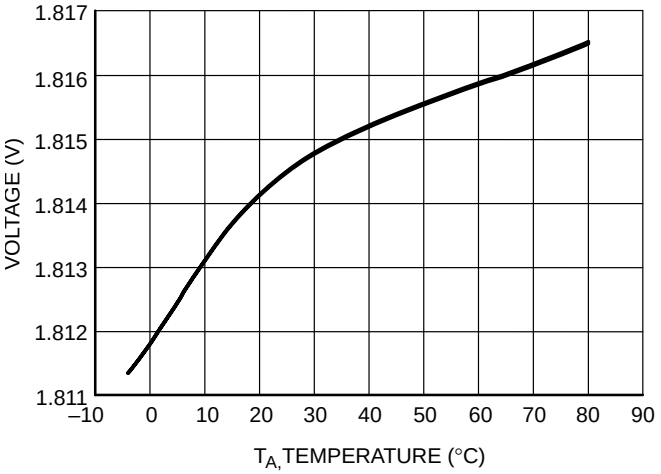


Figure 12. Regulator 1 Line Regulation vs. Temperature 50 mA Load (3.0 V to 3.6 V)

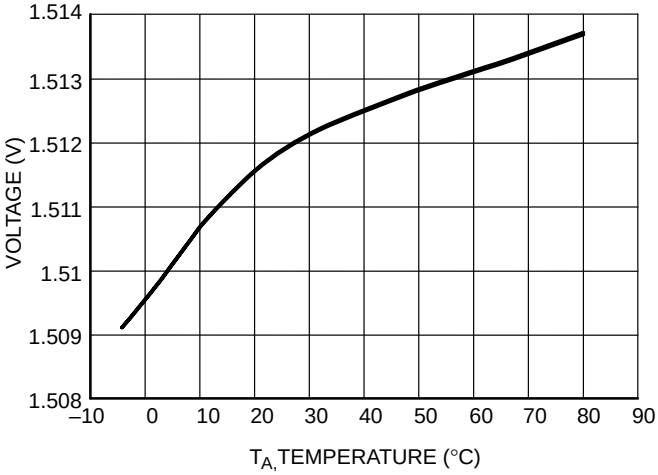


Figure 13. Regulator 2 Line Regulation vs. Temperature 50 mA Load (3.0 V to 3.6 V)

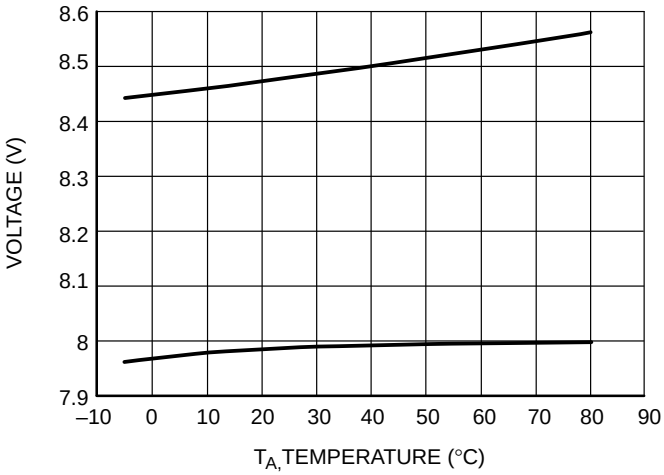


Figure 14. Under Voltage Lock Out Threshold vs. Temperature

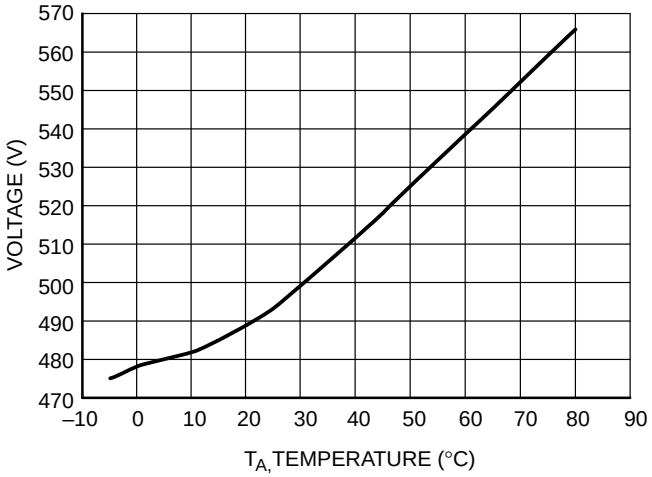


Figure 15. Under Voltage Hysteresis vs. Temperature

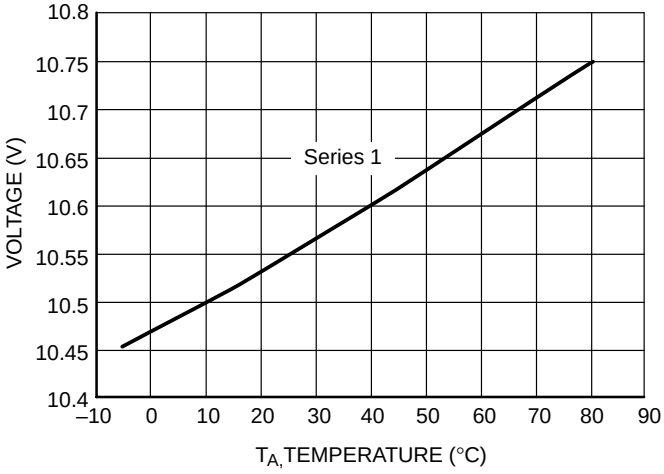


Figure 16. Regulator 2 Maximum Gate Voltage with SHDN = 4.2 V vs. Temperature V_{CC} = 12 V

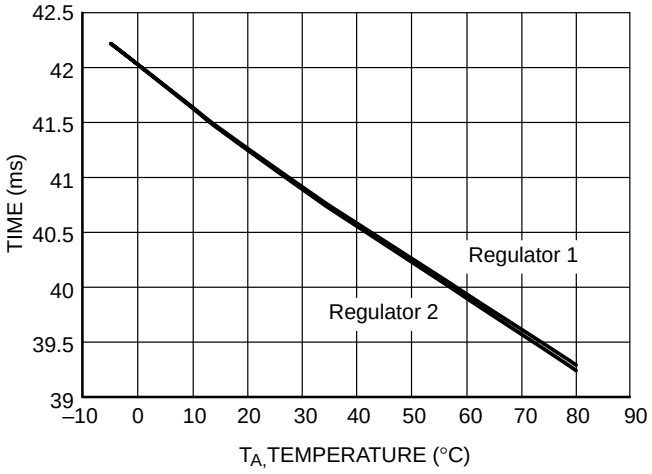


Figure 17. Hiccup Off Time Temperature

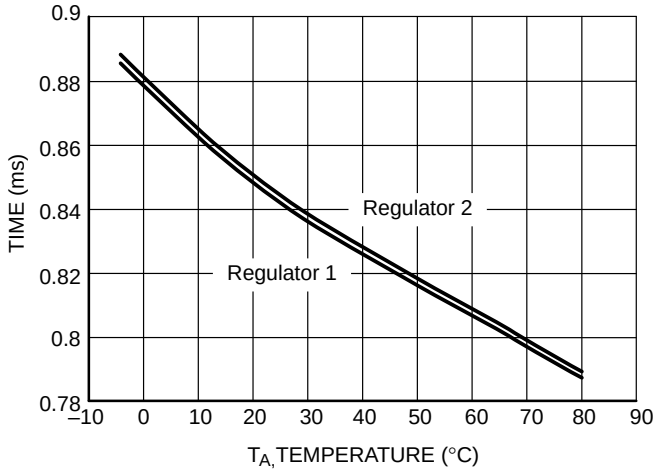


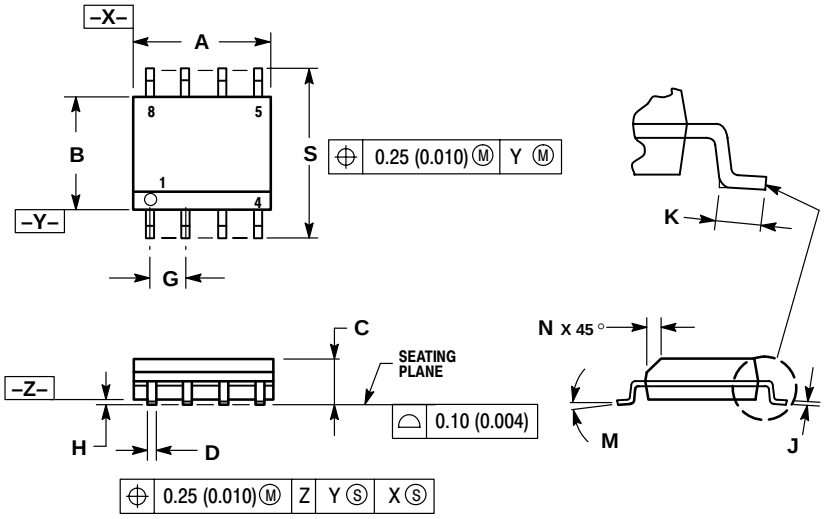
Figure 18. Hiccup On Time vs. Temperature

ORDERING INFORMATION

Device	Output Voltage (V_{out1})	Regulated/Bypass (V_{out2})	Package	Shipping
MC33567D–1	1.8 V	1.5 V/3.3 V	SO–8	98 Units/Rail
MC33567D–1R2	1.8 V	1.5 V/3.3 V	SO–8	2500 Tape & Reel
MC33567D–2	2.5 V	2.5 V	SO–8	98 Units/Rail
MC33567D–2R2	2.5 V	2.5 V	SO–8	2500 Tape & Reel

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–07
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

Notes

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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ON Semiconductor Website: http://onsemi.com

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Sales Representative.