MV1815

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

(Supersedes June 1990 Edition and Version in Satellite, Cable and T.V. Handbook October 1988)

The MV1815 is an advanced CMOS single chip Teletext decoder for 625 line World System Teletex. The MV1815 has an on–chip data slicer circuit, dual page acquisition circuits, and direct memory addressing which allow a low cost Teletext decoder to be built with a minimum number of additional components.

FEATURES

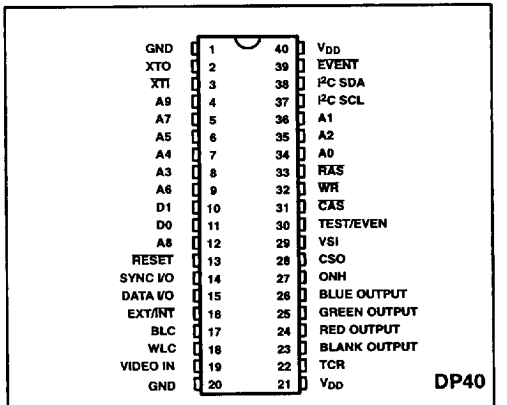
- On–Chip data slicing
- Up to 254 display pages stored, using low cost 150ns DRAMS
- Low external component count
- I²C Bus for low cost interfacing
- Multi–language capability for fourteen European languages
- Special parity inhibit for TOP 8–bit data
- Non–display packets stored for linked page operation, video programming, etc.
- high resolution characters typically 12 dots wide on a 15 by 10 matrix
- Accepts all non–display packets
- On–chip video switch
- Advanced CMOS technology gives low power disipation and high reliability

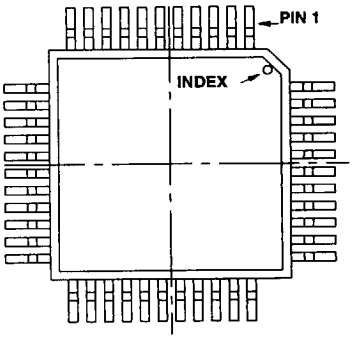
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	–0.3V to +7.0V
All inputs	–0.3V to V_{DD} + 0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	–65°C to + 150°C

ORDERING INFORMATION

MV1815–2 BA DP	West European version
MV1815–2 BA GP/GPTJ	West European version
MV1815–3 BA DP	West & East European version





PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	A1	16	D1	31	BLANK
2	SCL	17	D0	32	RED
3	SDA	18	A8	33	GREEN
4	N/C	19	N/C	34	BLUE
5	EVENT	20	RESET	35	ONH
6	V_{DD}	21	SYNC I/O	36	CSO
7	GND	22	DATA I/O	37	VSI
8	XTO	23	EXT/INT	38	N/C
9	XTI	24	BLC	39	TEST/EVEN
10	A9	25	WLC	40	CAS
11	A7	26	VIDEO	41	WR
12	A5	27	GND	42	RAS
13	A4	28	V_{DD}	43	A0
14	A3	29	TCR	44	A2
15	A6	30	N/C		

Fig. 1 Pin connections – top view

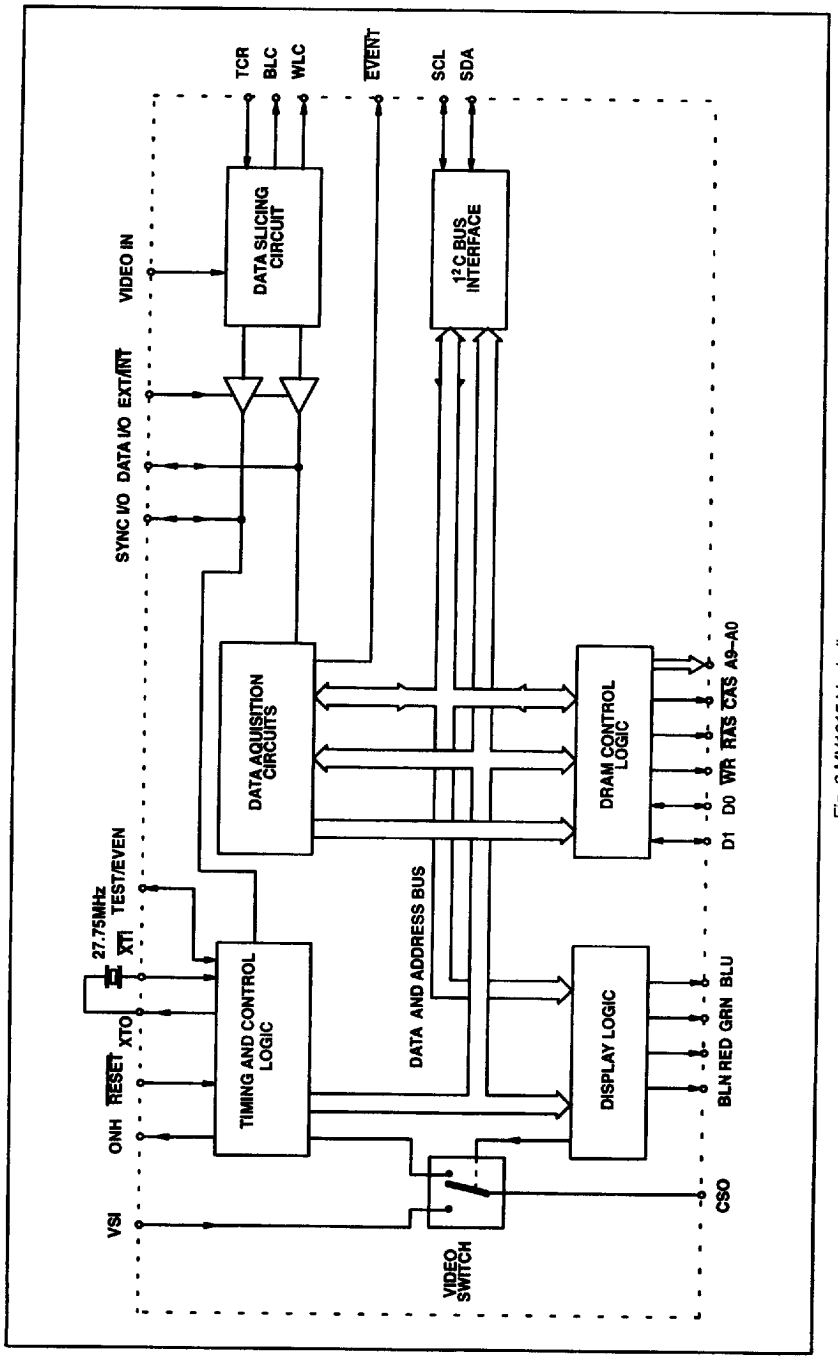


Fig. 2 MV1815 block diagram

Section	Specification
Data Acquisition Logic	
Line Standard	625 Lines 50 Fields/second
Teletext data rate	6.9375 Mbits/sec ±25ppm
Data line content	360 bits as 45 bytes of 8 bits each
TV lines used VBI	Lines 6 to 22 and 318 to 335
TV lines used full field	All TV Lines
Packets accepted	×/0 to ×/25, ×/26, ×/27, ×/28, ×/29, ×/30 (all formats), ×/31
Page numbers	000 to 7FF
Page subcodes	0000 to 3F7F
Display Logic	
Characters per row	40, occupying 43.24µs of the 52µs display time
Teletext rows displayed	0 to 23 with 24 and 25 software programmable
TV lines used	TV Lines: Rows Displayed / Start / Finish 24 / 48 / 287 25 or 26 / 38 / 297
Character definition	15 × 10 dot matrix
Character Sets	English, German, Swedish, Italian, French, Spanish,Czechoslovakian, Polish, Romanian, Hungarian, Turkish, Danish, Serbo–Croat, ASCII
Spacing control characters	Standard Level One Range
Data boxing into picture	Page Number – Row 0 characters 1 to 8 Page Header – Row 0 characters 9 to 32 Clock Time – Row 0 characters 33 to 40 Rows 24 and 25
Displayable page stores	Up to 254 pages, each of 1k bytes, depending on the size of the DRAM being used
Display options	Mix of text foreground and picture background Three part magnify – display rows 0 to 11 double height display rows 6 to 17 double height display rows 12 to 23 double height Boxing of Newsflash and Subtitles into picture Boxing of picture into text
Dynamic RAM Control Logic	
Memory Configuration	All sizes: Page or nibble mode types 254 pages – 2 off 1M × 1 or 1 off 1M × 4 62 pages – 2 off 256k × 1 or 1 off 256k × 4 14 pages – 2 off 64k × 1 or 1 off 64k × 4
Maximum access time (t_{RAC})	150ns
Refresh period for complete memory	2.048ms Refresh occurs during the line flyback period. Contents of any memory location may be accessed by the microprocessor via the I²C Bus Interface
I²C Bus Interface	Standard implementation of a slave transmitter/receiver Control of the MV1815 is via the I²C Bus Interface
I²C Bus Address	0010 001 R/$\overline{W}$

Table 1. MV1815 System specification

PIN DESCRIPTION		
Symbol	Pin No (DP 40)	Pin name and Description
GND	1, 20	Ground, both pins must be connected
XTO	2	Crystal out 27.75MHz fundamental crystal with an on–chip 1MΩ bias resistor to $\overline{XTI}$
$\overline{XTI}$	3	Crystal input
A9, A7, A5, A4, A3, A6, A8, A0, A2, A1	4 – 9 12, 34, 35, 36	DRAM address outputs
D1, D0	10, 11	DRAM data lines. Internal 100kΩ pull – up resistors are included.
$\overline{RESET}$	13	Active low reset input. Includes 100kΩ pull – up resistor.
SYNC I/O	14	Sliced sync input / output.
DATA I/O	15	Teletext data input / output
EXT/$\overline{INT}$	16	Control pin for SYNC and DATA I/O. Includes 100kΩ pull–down resistor. When low or not connected internal SYNC and DATA are used, pins 14 & 15 are outputs. When high supply SYNC and DATA from an external source, pins 14 & 15 are inputs.
BLC	17	Black level capacitor.
WLC	18	White level capacitor
VIDEO IN	19	Input for composite video signal with negative going SYNCS.
VDD	21, 40	+5V Supply. Both pins must be connected.
TCR	22	Time constant resistor controlling discharge rate of black and white level capacitor voltages.
BLANK	23	Blanking output, high power push–pull driver.
RED	24	Red output, high power push–pull tri–state driver.
GREEN	25	Green output, high power push–pull tri–state driver.
BLUE	26	Blue output, high power push–pull tri–state driver.
ONH	27	On hours indicator. When high CSO is locked to Video In. When low CSO is not locked.
CSO	28	Generated composite sync output during text, video input is switched through to CSO during modes that contain picture content. See Fig. 6.
VSI	29	Video switch input.
TEST	30	Used for factory testing. Even output is enabled by bits IOE and EOE in SYNCSW register. If EVEN output is not used, the pin should be left open–circuit. A 100kΩ pull–down resistor is included.
$\overline{CAS}$	31	DRAM column address strobe.
$\overline{WR}$	32	DRAM read/not write signal.
$\overline{RAS}$	33	DRAM row address strobe.
I^2C SCL	37	I^2C bus serial clock.
I^2C SDA	38	I^2C bus bi–directional data port.
$\overline{EVENT}$	39	Active low open drain output interrupt signal to microprocessor.

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 27.750000MHz. AT cut

Tolerance overall ±100ppm.
Nominal load capacitance 20pF
Equivalent series resistance <20Ω

A variable capacitor is provided internally on pin $\overline{XTI}$ and controlled by a phase locked loop to provide exact trimming of the frequency. This will provide compensation for temperature variation and crystal ageing.

BIT POSITION												
ADDRESS		REGISTER	7	6	5	4	3	2	1	0	R/W	RESET STATE
DEC	HEX											HEX
		RADD	A17	A16	IAI	RA4	RA3	RA2	RA1	RA0	W	00
0	0	ACONA	ACQ	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
1	1	STORA	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	W	02
2	2	PGS1A	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
3	3	PGS2A	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	20
4	4	PGS3A	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	00
5	5	ACONB	$\overline{HLD}$	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
6	6	STORB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	W	03
7	7	PGS1B	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
8	8	PGS2B	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBA0	W	00
9	9	PGS3B	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	88
10	A	RECON	WI0	WI24	WI25	PIN B	PIN A	FF	CDB	CDA	W	00
11	B	DISCON1	INV	RLH	DSB	CLS	CUR	BLC	LS3	UDI	W	00
12	C	DISCON2	LSO	LS1	LS2	MGS	IHD	SPH	BX1	BX0	W	00
13	D	DISCON3	TXT	MIX	INT	REV	UDK	SPOS	ST2	ST1	W	00
14	E	DISCON4	BXP	BXH	BXT	BXS	DHT	DHB	SG2	SG1	W	00
15	F	HADD	A15	A14	A13	A12	A11	A10	A9	A8	W	00
16	10	LADD	A7	A6	A5	A4	A3	A2	A1	A0	W	00
17	11	WDATA	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	W	00
19	13	SCROLL	WI29	MV	CRL	SRA4	SRA3	SRA2	SRA1	SRA0	W	00
20	14	SYNCSW	ESS	–	–	–	IOE	EOE	SEN	SVS	W	00
0	0	EVENTA	NPR	VHR	830A	X/29	X/28	X/27	X/26	C8	R	–
1	1	EVENTB	NPR	VHR	830B	X/29	X/28	X/27	X/26	C8	R	–
2	2	CBITSA	C14	C13	C12	C11	C10	C7	C6	C5	R	–
3	3	PGR1A	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
4	4	PGR2A	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
5	5	PGR3A	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
6	6	CBITB	C14	C13	C12	C11	C10	C7	C6	C5	R	–
7	7	PGR1B	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
8	8	PGR2B	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
9	9	PGR3B	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
10	A	HAMMC	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0	R	FF
17	11	RDATA	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	–

Table 2 MV1815 Register details

Note. Write register addresses 18, and 21–31 (12, and15–1F HEX) are reserved for future development and should not be used.

WRITE REGISTERS

RADD	(W)
A16 / A17	Memory quadrant select
IAI	Inhibit auto increment
RA$	Register address ($=0 to 4)

ACON A/B	(W 0 & 5)
ACQ	Aquisition on
MGC	Magazine compare
PAC	Page units compare
PBC	Page tens compare
SAC	Page subcode compare digit A
SBC	Page subcode compare digit B
SCC	Page subcode compare digit C
SDC	Page subcode compare digit D
HLD	Not hold display acquisition circuit

STOR A/B	(W 1 & 6)
STA$	Store number for aquisition A ($=0 to 7)
STB$	Store number for aquisition B ($=0 to 7)

PGS /1/2/3 A/B	(W 2,3 4 & 7,8,9)
SAS$	Sub–Code digit A ($=0 to 3) select
SBS$	Sub–Code digit B ($=0 to 2) select
SCS$	Sub–Code digit C ($=0 to 3) select
SDS$	Sub–Code digit D ($=0 or 1) select
PAS$	Page number (units) ($=0 to 3) select
PBS$	Page number (tens) ($=0 to 3) select
MS$	Magazine number ($=0 to 2) select

RECON	(W 10)
WI0	Write inhibit of packet 0
WI24	Write inhibit of packet 24
WI25	Write inhibit of packet 25
PIN B	Parity check inhibit acquisition circuit B
PIN A	Parity check inhibit acquisition circuit A
FF	Full field Teletext
CDB	Clear store disable acquisition circuit B
CDA	Clear store disable acquisition circuit A

DISCON1	(W 11)
INV	Invert display
RLH	Roll headers
DSB	Display acquisition circuit B (A if zero)
CLS	Clear current display store
CUR	Cursor enable
BLC	Block cursor
LS3	Language group select
UDI	Dispaly update indicator

DISCON2	(W 12)
LS$	Language select ($=0 to 2)
MGS	Magazine serial
IHD	Inhibit display, rows 2 to 26 disabled
SPH	Suppress header
BX$	Box control bits ($=0 or 1)

DISCON3	(W 13)
TXT	Text / not picture
MIX	Mix text and picture
INT	Display text in interlace mode (see Figure 6)
REV	Reveal hidden text
UDK	Update key, rows 1 to 26 disabled.
SPOS	Status line position
ST2	Display Status line 2 (row 26)
ST1	Display Status line 1 (row 25)

WRITE REGISTERS

DISCON4	(W 14)
BXP	Box page number
BXH	Box header
BXT	Box time
BXS	Box status rows
DHT	Double height top half
DHB	Double height bottom half
SG$	Seperate graphics control bits ($=0 or 1)

HADD and LADD	(W 15 & 14)
A$	Memory address ($=0 to 15)

WDATA	(W 17)
WD$	Data to be written to memory ($=0 to 7)

SCROLL	(W 19)
WI29	Write inhibit of packet 29
MV	Majority vote on framing code
CRL	Cursor lock at last HADD. LADD setting
SRA$	Scroll display row up ($=0 to 4)

SYNCSW	(W 20)
ESS	External sync source
IOE	Internal output enable
EOE	Even output enable
SEN	Select enable – SVS bit
SVS	Select VSI as sync source

READ REGISTER

EVENT A/B	(R 0 & 1)
NPR	New page received
VHR	Valid header received
830$	Packet 30 received aquisition $ ($=A or B)
X/29	Packet 29 received
X/28	Packet 28 received
X/27	Packet 27 received
X/26	Packet 26 received
C8	Update Indicator

CBITS A/B	(R 2 & 6)
C14	Language select bit
C13	Language select bit
C12	Language select bit
C11	Magazine serial
C10	Inhibit display
C7	Supress header
C6	Sub–title
C5	Newsflash

PGR/1/2/3/A/B	(R 3,4,5 & 7,8,9)
SAR$	Sub–code digit A ($=0 to 3) received
SBR$	Sub–code digit B ($=0 to 2) received
SCR$	Sub–code digit C ($=0 to 3) received
SDR$	Sub–code digit D ($=0 or 1) received
PAR$	Page number (units) ($=0 to 3) received
PBR$	Page number (tens) ($=0 to 3) received
MR$	Magazine number ($=0 to 2) received

HAMMC	(R 10)
HC$	Hamming counter ($=0 to 7)

RDATA	(R 17)
RD$	Data read from memory ($=0 to 7)

I²C BUS

Device Address **0010 001 R/W**

The circuit works as a slave transmitter with bit eight set high or as a slave receiver with bit eight low. In receive mode, the first data byte is written to the RADD register, where the least significant five bits from the sub–address for the next register to be written. The most significant three bits of RADD are data bits, see Table 2.

Automatic incrementing of registers allows successive data bytes to be written to or read from the registers. The automatic incrementing can be disabled by setting bit 5 of the sub–address register (RADD) to one.

If the sub–address is set to write or read from DRAM, the auto incrementing allows access to successive bytes of data. All DRAM addresses may be accessed via the I²C bus register. A stop condition resets the sub–address to zero.

Example of I²C Bus Messages

Write operation – MV1815 as a slave receiver

S	MV1815 ADD	W	A*	RADD (n)	A*	DATA (reg n)	A*	DATA (reg n + 1)	A*	P

Read operation – MV1815 as a slave transmitter

S	MV1815 ADD	R	A*	DATA * (reg 0)	A	DATA * (reg 1)	A	DATA * (reg 2)	A	P

S Start Conditions
P Stop Condition
A Acknowledge
W Write (=0)
R Read (=1)
* MV1815 output

Write/read operation – MV1815 as a slave transmitter sending data from register n etc.

S	MV1815 ADD	W	A*	RADD (reg n)	A*	S	MV1815 ADD	R	A*	DATA* (reg n)	A	DATA (reg n + 1)	A	P

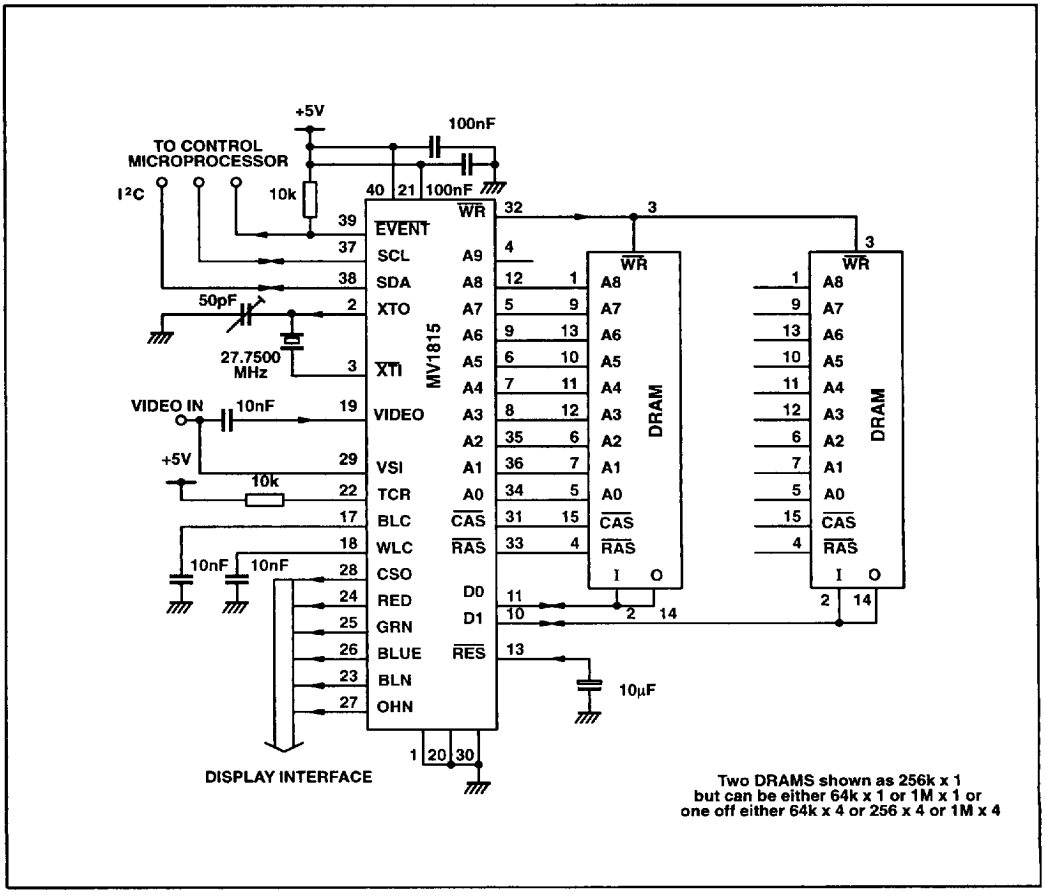


Fig. 3. MV1815 Typical application

DRAM Memory Organisation

The DRAM as viewed from the I²C Bus is organised in 1024 byte blocks. Each 1024 bytes (400 HEX) block is referred to as a store. Stores 0 and 1 are reserved for the non–display packets from acquisition A and B respectively. Stores 2 and above are used for display pages, one page per store

The display page number, first 8 bytes on row 0, are held in Store 0 bytes 0 to 7. The Time display, last 8 bytes on row 0 are also held in store 0 bytes 8 to F (HEX). See Figs. 4 and Figs. 5

To calculate the values of the start address in RADD, HADD and LADD for any store simply multiply the store number (HEX) by 400 (HEX)

e.g. Decimal store 160 = A0

A0 x 400 = 2 (RADD) 80 (HADD) 00 (HEX) (LADD)

To find the address of any particular location in the store add the value of the relative address from Fig. 4 or 5.

Table 3 gives examples of the start addresses of stores expressed as values of A17, A16 from RADD, A15–A8 from HADD and A7–A0 from LADD.

STORE NUMBER HEX	START ADDRESS IN HEX		
	RADD	HADD	LADD
00	0	00	00
01	0	04	00
02	0	08	00
03	0	0C	00
04	0	10	00
05	0	14	00
06	0	18	00
07	0	1C	00
08	0	20	00
:		:	
0F	0	3C	00
10	0	40	00
:		:	
40	1	00	00
41	1	04	00
:		:	
7F	1	FC	00
80	2	00	00
:		:	
F0	3	C0	00
:		:	
FF	3	FC	00

Table 3

Display Row	First byte Relative Address HEX		Last byte Relative Address HEX
0	000	NOTE 1 — PACKET 0 24 byte — NOTE 2	017
1	018	PACKET 1 40 bytes	03F
2	040		
3	068		
4	090		
5	0B8		
6	0E0		
7	108		
8	130		
9	158		
10	180		
11	1A8		
12	1D0	PACKETS 2 – 23	
13	1F8		
14	220		
15	248		
16	270		
17	298		
18	2C0		
19	2E8		
20	310		
21	338		
22	360		
23	388		
24	3B0	PACKET 24	
25	3D8	PACKET 25	3FF

Fig. 4 Organisation of Display Memory. Stores 2 to 256

NOTE 1. Display of page number here, 8 bytes which are located in store 0 with absolute addresses 000 to 007.
NOTE 2. Display of time here, 8 bytes which are located in store 0 with absolute addresses 008 to 00F

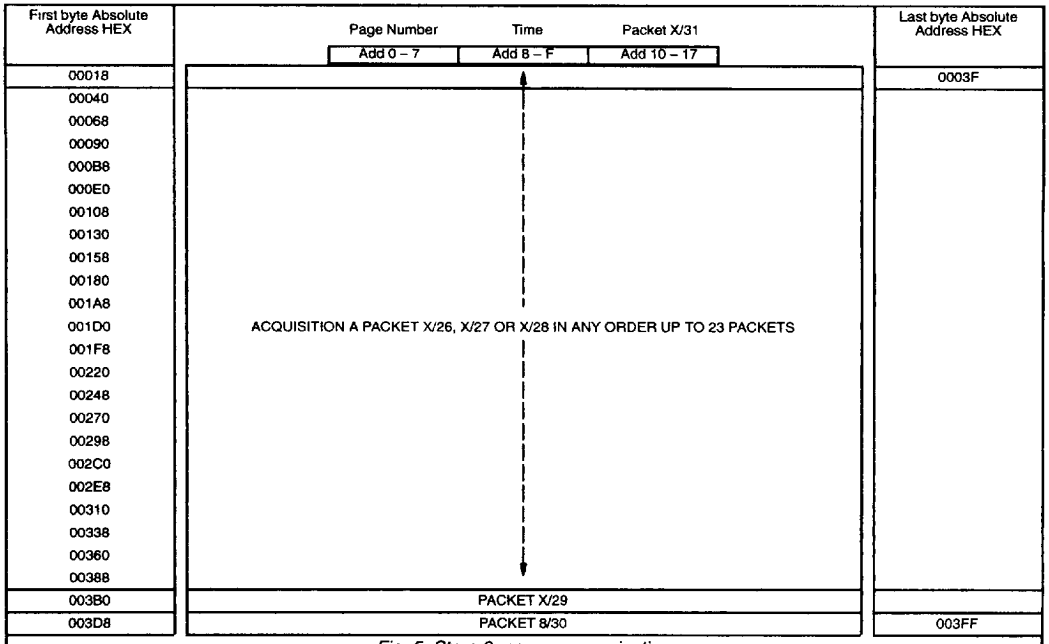


Fig. 5. Store 0 memory organisation

Packet 8/30 designation codes 0,1,4,5,8,9, C and D are written to store 0

NOTE: Store 1 is organised similarly except that it accepts aquisition circuit B packets X/26, etc The starting address is 00400 (HEX) and bytes 00400 to 00417 (HEX) are not used by the MV1815. All addresses shown in Fig 5 add 00400 (HEX)
Packet 8/30 designation codes 2,3,6,7, A,B,E and F are written to store 1.

	0	1
0	Alpha Black	Graphic Black
1	Alpha Red	Graphic Red
2	Alpha Green	Graphic Green
3	Alpha Yellow	Graphic Yelow
4	Alpha Blue	Graphic Blue
5	Alpha Magenta	Graphic Magenta
6	Alpha Cyan	Graphic Cyan
7	Alpha White[1]	Graphic White
8	Flash	Conceal Display [2]
9	Steady [1 2]	Contiguous Graphics [1 2]
A	End Box [1 2]	Separated Graphics [2]
B	Start Box [3]	No action
C	Normal Height [1 2]	Black Background [1 2]
D	Double Height	New Background [2]
E	No action	Hold Graphics
F	No action	Release Graphics [1]

Table 4 Control codes

Notes: 1. Presumed set at the start of each display row.

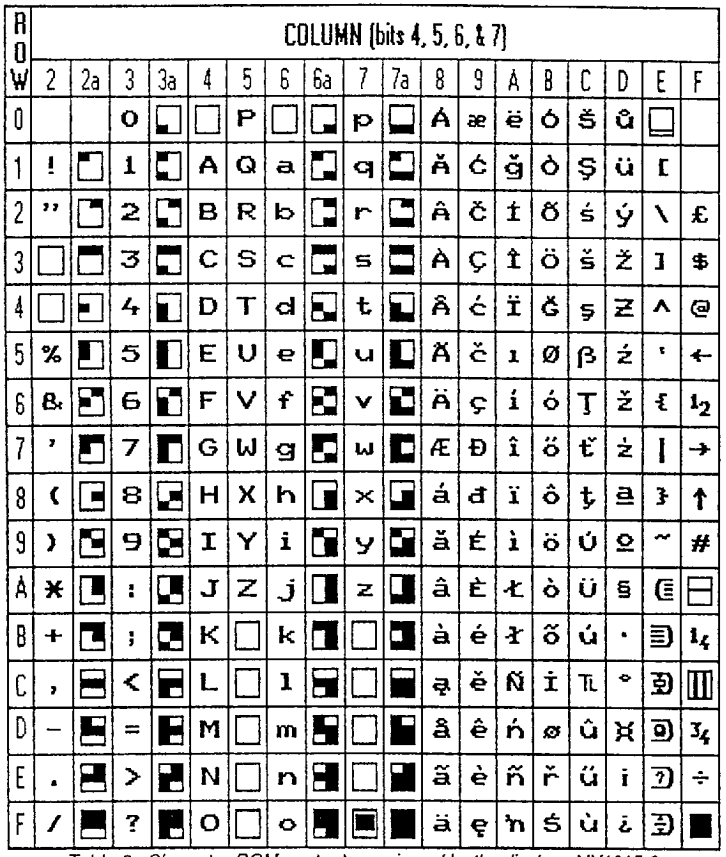
2 Action "set at the curent space", others are "set after the current space".

3. Two consecutive codes are transmitted, action takes place between them

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ENGLISH
2/3	£	#	#	£	é	ç	#	£
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	¡	č	@
5/B	←	Ä	Ä	°	ë	á	ť	←
5/C	½	Ö	Ö	ç	ê	é	ž	½
5/D	→	Ü	Å	→	ù	í	ý	→
5/E	↑	^	Ü	↑	î	ó	í	↑
5/F	#	_	_	#	#	ú	ř	#
6/0	▭	°	é	ù	è	¿	é	▭
7/B	¼	ä	ä	à	â	ü	á	¼
7/C	▮	ö	ö	ò	ô	ñ	ě	▮
7/D	¾	ü	å	è	û	è	ú	¾
7/E	÷	ß	ü	ì	ç	à	š	÷

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	POLISH	ROMANIAN	HUNGARIAN	TURKISH	DANISH	SERBO CROAT	ASCII	SOUTH AFRICAN
2/3	#	#	#	₺	£	#	#	£
2/4	ń	¤	ú	ğ	$	$	$	$
4/0	ą	Ţ	É	İ	@	Č	@	ħ
5/B	Ź	Â	í	Ş	Æ	Ć	[	ë
5/C	ś	Ş	Ö	Ö	Ø	Ž	\	ê
5/D	Ł	ă	Á	Ç	Å	Đ	]	ü
5/E	ć	î	ű	Ü	↑	š	^	é
5/F	ó	ı	ő	ğ	#	ë	_	ï
6/0	ę	ţ	é	ı	▭	č	'	š
7/B	ż	â	ó	ş	æ	ć	{	ä
7/C	ś	ş	ö	ö	ø	ž	▯	ô
7/D	ł	ă	á	ç	å	đ	}	û
7/E	ź	î	ü	ü	÷	š	~	ö

Table 5. Western European national optional variations - MV1815-2.



ROW	COLUMN (bits 4, 5, 6, & 7)																	
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0			0			P			p		Á	æ	ë	ó	š	û		
1	!		1		A	Q	a		q		ă	ć	ğ	ò	Ş	ü	[	
2	"		2		B	R	b		r		Â	č	ł	ő	ś	ý	\	£
3			3		C	S	c		s		À	Ç	î	ö	š	ž	]	$
4			4		D	T	d		t		Ã	ć	Ï	ğ	ş	Ź	^	@
5	%		5		E	U	e		u		Ä	č	ı	Ø	ß	ź	'	←
6	&		6		F	V	f		v		Ä	ç	í	ó	Ţ	ž	ł	½
7	'		7		G	W	g		w		Æ	Đ	î	ö	ť	ż	|	→
8	(		8		H	X	h		x		á	đ	ï	ô	ţ	ą	³	↑
9	)		9		I	Y	i		y		ă	É	ì	ö	Ú	ǫ	~	#
A	*		:		J	Z	j		z		â	È	ł	ò	Ü	ß		
B	+		;		K		k				à	é	ł	ő	ú	·		¼
C	,		<		L		l				ą	ě	Ń	ì	ű	°		
D	-		=		M		m				å	ê	ń	ø	û	ł		¾
E	.		>		N		n				ã	è	ń	ř	ü	ì		÷
F	/		?		O		o				ä	ę	ň	ś	ù	¿		

Table 6. Character ROM contents as viewed by the display - MV1815-2.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes. like the control columns 0 and 1 listed in table 4.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
☐ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 5. When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

LS(3210) TABLE POSITION	0000 ENGLISH	0001 GERMAN	0010 SWEDISH FINNISH	0011 ITALIAN	0100 FRENCH (BELGIAN)	0101 SPANISH	0110 CZECH	0111 ENGLISH
2/3	£	#	#	£	é	ç	#	£
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	i	č	@
5/B	←	Ä	Ä	°	ë	á	ť	←
5/C	½	Ö	Ö	ç	ê	é	ž	½
5/D	→	Ü	Å	→	ù	í	ý	→
5/E	↑	^	Ü	↑	î	ó	í	↑
5/F	#	_	_	#	#	ú	ř	#
6/0	¼	°	é	ù	è	¿	é	¼
7/B	¼	ä	ä	à	â	ü	á	¼
7/C	¾	ö	ö	ò	ô	ñ	ě	¾
7/D	¾	ü	å	è	û	è	ú	¾
7/E	÷	ß	ü	ì	ç	à	š	÷

LS(3210) TABLE POSITION	1000 ENGLISH	1001 GERMAN	1010 HUNGARIAN	1011 TURKISH	1100 DANISH	1101 SPANISH	1110 CZECH	1111 SOUTH AFRICAN
2/3	£	#	#	₺	£	ç	#	£
2/4	$	$	ú	ğ	$	$	ů	$
4/0	@	§	É	İ	@	i	č	ʼn
5/B	←	Ä	í	Ş	Æ	á	ť	ë
5/C	½	Ö	Ö	Ö	Ø	é	ž	ê
5/D	→	Ü	Á	Ç	Å	í	ý	ü
5/E	↑	^	ű	Ü	↑	ó	í	é
5/F	#	_	ő	Ğ	#	ú	ř	ï
6/0	¼	°	é	ı	¼	¿	é	š
7/B	¼	ä	ó	ş	æ	ü	á	ä
7/C	¾	ö	ö	ö	ø	ñ	ě	ô
7/D	¾	ü	á	ç	å	è	ú	û
7/E	÷	ß	ü	ü	÷	à	š	ö

Table 7. West and East European national optional variations MV1815-3.

ROW	COLUMN (bits 5, 6, 7 & 8)																
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0		□	0	▖	□	P	□	▖	p	▂	Á	č	ť	ň	ŕ	Ú	□	
1	!	▘	1	▘	A	Q	a	▘	q	▂	Â	ç	ť	h	ř	ů	₸	
2	"	▝	2	▝	B	R	b	▝	r	▂	Ä	Ď	ï	ó	ŕ	ú	¤	£
3	□	▀	3	▀	C	S	c	▀	s	▂	Ă	Đ	í	ò	ř	û	¡	$
4	□	▌	4	▌	D	T	d	▌	t	▂	Ă	ď	ı	ô	š	ü	¿	@
5	%	▌	5	▌	E	U	e	▌	u	▂	Ä	đ	í	ö	Ş	ű	·	←
6	&	▚	6	▚	F	V	f	▚	v	▂	Æ	É	î	ő	š	ô	^	½
7	'	▛	7	▛	G	W	g	▛	w	▂	á	È	ï	Ô	ş	ù	▯	→
8	(	▜	8	▜	H	X	h	▜	x	▂	â	Ě	ì	ø	ß	Ý	▲	↑
9	)	▞	9	▞	I	Y	i	▞	y	▂	à	é	Ĺ	ó	ţ	ý	▼	#
A	*	▙	:	▙	J	Z	j	▙	z	▂	å	ě	ľ	ò	ť	ž	⋵	⊟
B	+	▙	;	▙	K	□	k	▙	□	▂	ã	ê	ĺ	ő	Þ	ž	⋹	¼
C	,	▄	<	▄	L	□	l	▄	□	▂	ä	è	ľ	ö	þ	a	⋺	⫼
D	-	▄	=	▄	M	□	m	▄	□	▂	æ	ë	Ń	ő	Ú	º	⋻	¾
E	.	▄	>	▄	N	□	n	▄	□	▂	č	ğ	ń	ô	Ů	§	⋼	÷
F	/	▄	?	▄	O	□	o	▄	▄	▄	Ç	ğ	ń	ø	Ü	°	⋽	■

Table 8. Character ROM contents as viewed by the display MV1815-3.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes. like the control columns 0 and 1 listed in table 4.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
□ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 7. When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{CC}= +5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage	21 & 40	4.5	5.0	5.5	V	XTI=27.75MHz All outputs open
Supply Current	21 & 40		25		mA	circuit
	21 & 40		15		mA	XTI=0Hz All outputs open circuit
Video Input, VSI	19 & 29					
Voltage Amplitude		0.8		3.0	Vpp	Bottom of Sync to White (pk–pk)
Source Impedance				250	Ω	
TCR Input	22					
External Resistance		5	10	200	kΩ	Connected to V_{DD}
BLC and WLC	17 & 18					
Capacitor Value			10		nF	Connected to GND
Capacitor Tolerance		–10		+10		
Effective Series Resistance				5	Ω	1MHz
Sync I/O	14					100K (nom) pull up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input Current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input Current High		–30		+30	µA	V_{IN}=V_{DD}
Data I/O	15					No pull–up resistor
Output voltage High		2.4	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input Voltage High		V_{DD}–1.0		V_{DD}	V	
Input current	–30		+30		µA	V_{IN}=V_{DD} or V_{SS}
EXT/$\overline{INT}$ (Note 1)	16					100kΩ (nom) pull–down resistor
Input current Low		–10		+10	µA	V_{IN}=V_{SS}
Input current High		22	50	220	µA	V_{IN}=V_{DD}
$\overline{XTI}$ (Note 1)	3					1M (nom) resistor to XTO
Input current Low		–5.0	–5.0	–20	µA	–0.3 <V_{IN} <V_{IL} max
Input current High		0.5	5.0	20	µA	V_{IH} min <V_{IN} <(V_{DD}+0.3)
XTO output	2					See note 2
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Frequency			27.750		MHz	±100ppm

Notes.

1. Input voltage low and input voltage high for these are as specified for Data I/O
2. When $\overline{RESET}$ is held low, A9 (pin 4) will output F_{OSC}/2. If required, adjust capacitor on XTO for a frequency of 13.875MHz.

ELECTRICAL CHARACTERISTICS (continued)

T_{amb}= 0°C to +70°C, V_{CC}=+5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
ON HOUR INDICATOR ONH	27					
Output voltage V_{OH}		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage V_{OL}			0.2	0.4	V	I_{OL}=2.4mA
I²C bus SCL, SDA I/Ps	37, 38					100kΩ (nom) pull–up resistor
Input voltage Low		0		1.5	V	
Input voltage High		3.5		V_{DD}	V	
Output voltage Low		0	0 1	0.40	V	I_{OL}=3mA
SCL clock frequency	37		100	1000	kHz	
RED, GREEN, BLUE	24, 25, 26					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–12.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=24.0mA
Tri–state output leakage current		–60		60	µA	V_{OH}=V_{SS} or V_{DD}
EVENT	39					100kΩ (nom) pull–up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
BLANK	23					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–12.0mA
Output Voltage Low			0.2	0.4	V	I_{OL}=24.0mA
CSO	28					With typical load of 360Ω
Output voltage swing			0.5		Vpp	Text mode only, see note 3
Output voltage High		V_{DD}–0.5			V	Load of 4.3kΩ to V_{DD}
Output voltage Low				V_{DD}+0.5	V	
TEST/EVEN	30					100kΩ (nom) pull–down resistor
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–30		+30	µA	V_{IN}=V_{SS}
Input current High		22	50	220	µA	V_{IN}=V_{DD}

Note 3.

CSO output voltage when in picture or mix mode will depend on size of Video signal applied to VSI pin 29, together with attenuation due to internal transmission switch (60Ω nom) and external load on pin 28. In these states the video signal at pin 29 is switched straight through to pin 28.

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{CC}=+5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
MEMORY INTERFACE						100kΩ (nom) pull–up resistor
DATA D0,D1	11,10					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input current High		–30		+30	µA	V_{IN}=V_{DD}
ADDRESS A0–A9 $\overline{RAS}$, $\overline{CAS}$, $\overline{WR}$	See Fig. 1					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
$\overline{RESET}$ (Schmitt input)	13					100kΩ (nom) pull–up resistor
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input current High		–10		+10	µA	V_{IN}=V_{DD}
Hysteresis voltage			0.8		V	(Rising threshold) – (falling threshold) voltages

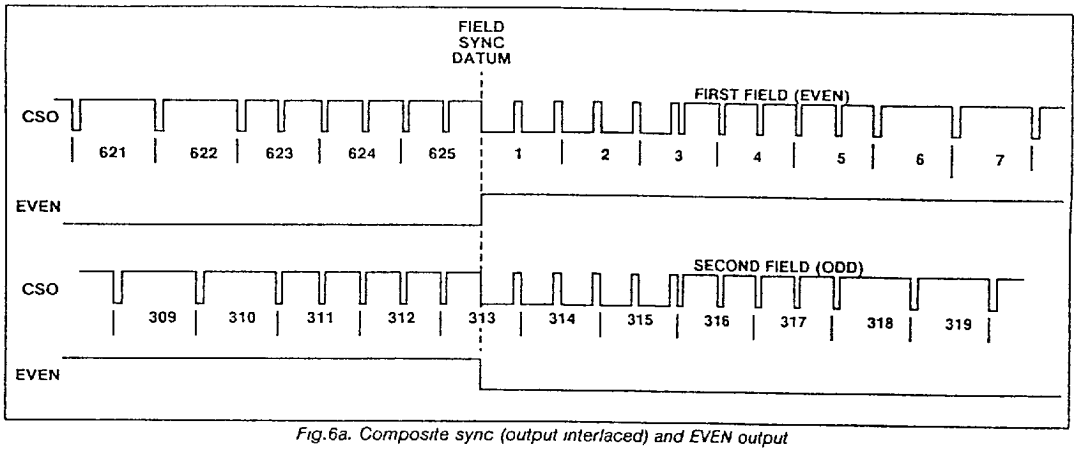


Fig.6a. Composite sync (output interlaced) and EVEN output

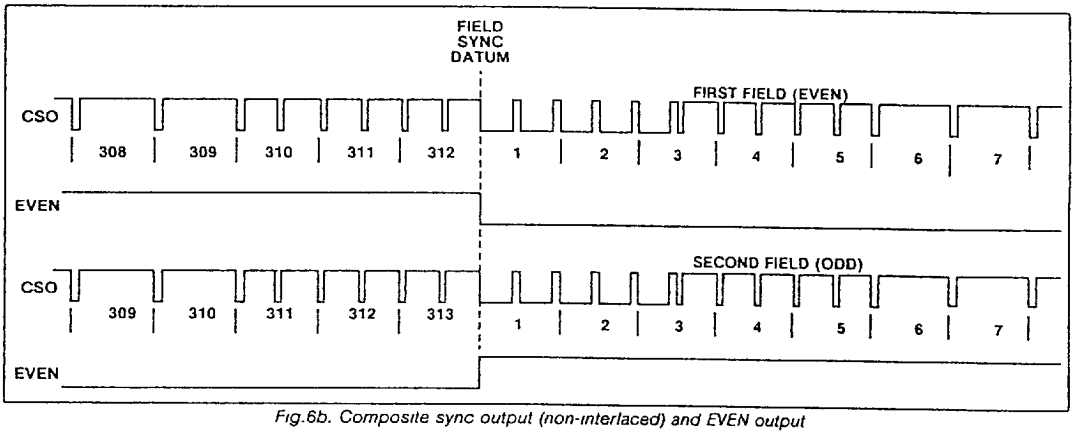


Fig.6b. Composite sync output (non-interlaced) and EVEN output

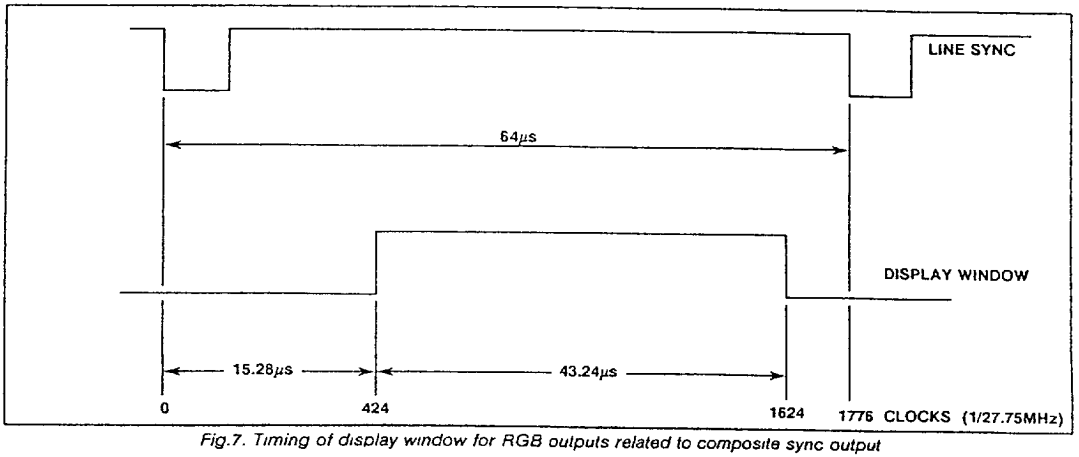


Fig.7. Timing of display window for RGB outputs related to composite sync output