NCV7310

Single Wire LIN Transceiver with Regulator Control

NCV7310 provides the physical interface for LIN (Local Interconnect Network). The device works in cooperation with a microprocessor providing serial data to a single wire network, and receiving data over the same network. System design requires a master/slave operation. The device is backward compatible with ISO9141 while meeting the newer LIN objectives, including slew rate control. Applications can be found in the industrial market as well as the automotive market. This device includes an inhibit (INH) function used to control an external voltage regulator.

Features

- Single–Wire Transceiver Compatible with the LIN Protocol
- Also Compatible with ISO 9141
- 20 kbit/s Operation
- Low Current Sleep Mode
- Short Circuit Protection
- Thermal Shutdown
- ESD to 4.0 kV All Pins
- Loss of Ground Does Not Affect Bus Activity
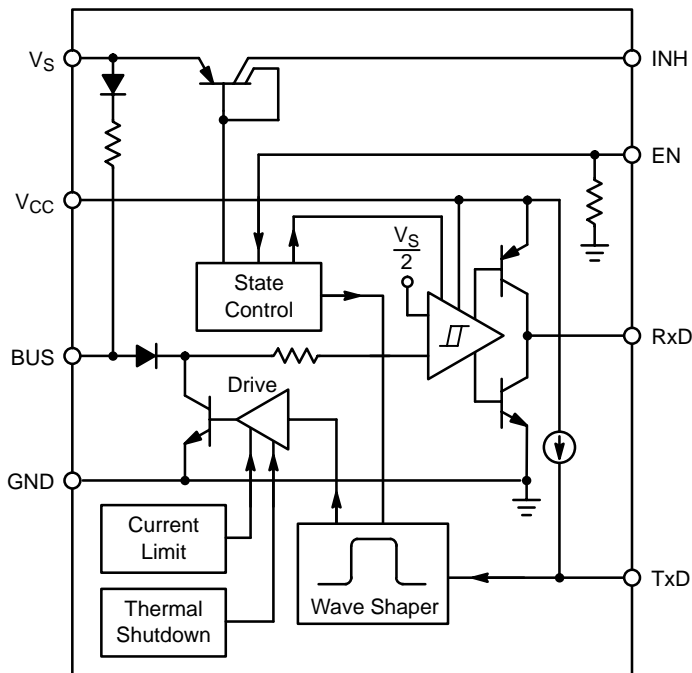- Unpowered Node Does Not Affect Bus Activity
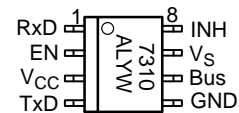

Figure 1. Block Diagram

ON Semiconductor™

http://onsemi.com

SO–8
D SUFFIX
CASE 751

PIN CONNECTION AND MARKING DIAGRAM

A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
NCV7310D	SO–8	95 Units/Rail
NCV7310DR2	SO–8	2500 Tape & Reel

NCV7310
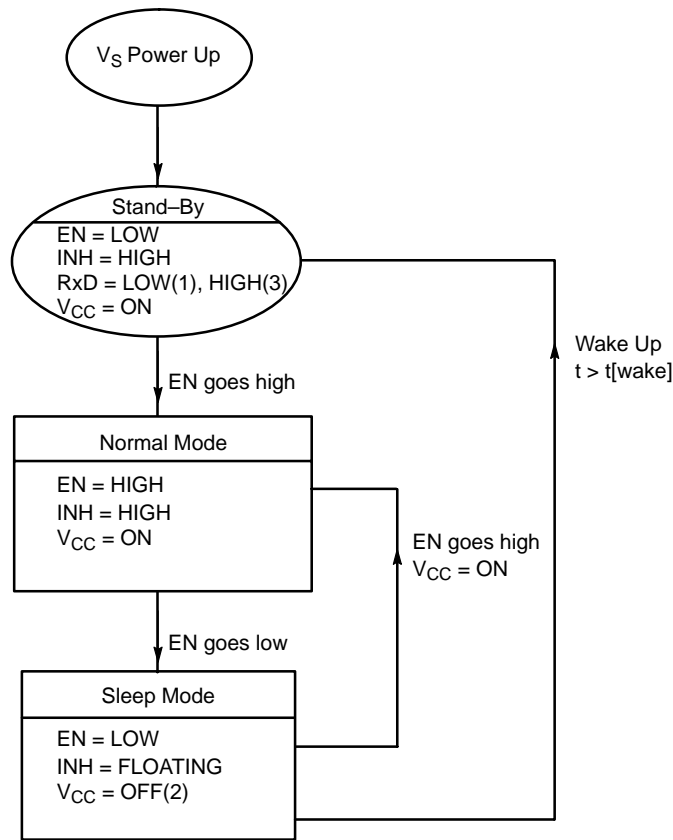
1. After wake–up via bus.
2. ON when INH not used to control external voltage regulator.
3. After V_S power up.

Figure 2. State Diagram

MAXIMUM RATINGS*

Symbol	Rating	Value	Unit
V_{CC}	Logic Power Supply Voltage	−0.3 to 6.0	V
V_S	Battery Supply Voltage	−0.3 to 40	V
Bus	Bus Input Voltage	−20 to 28	Vdc
Bus	Bus Input Voltage (t < 1.0 ms)	40	V
EN, TxD, RxD	Logic Input Voltage	−0.3 to V_{CC} + 0.3	V
INH	INHIBIT	−0.3 to V_S + 0.3	V
ESD	ESD Discharge Susceptibility (Human Body Model)	4.0	kV
T_J	Operating Junction Temperature	−40 to 150	°C
Tstg	Storage Temperature Range	−55 to 150	°C

$R_{\theta JC}$
$R_{\theta JA}$
	Package Thermal Resistance
	    Junction–to–Case
	    Junction–to–Ambient
		45
		165
			°C/W
			°C/W

*The maximum package power dissipation must be observed.

NCV7310

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_{CC} ≤ 5.5 V, 6.0 V ≤ V_S ≤ 20 V, R_T = 1.0 kΩ, EN = V_{CC},
−40°C ≤ T_J ≤ 125°C; unless otherwise specified. Note 1. See Figures 4 and 5.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
I_{CC} Quiescent Current Recessive State	TxD = V_{CC}, Note 2.	–	2.0	4.0	mA
I_{CC} Quiescent Current Dominant State	TxD = 0 V, Note 2.	–	2.0	4.0	mA
I_S Quiescent Current Recessive State	TxD = V_{CC}	–	1.0	2.0	mA
I_S Quiescent Current Dominant State	TxD = 0 V	–	6.0	8.0	mA
Quiescent Current Sleep Mode	V_S ≤ 12 V. Note 3.	–	35	50	μA
RxD High Level Output Voltage	I_{RxD} = −400 μA	$0.8 \times V_{CC}$	–	V_{CC}	V
RxD Low Level Output Voltage	I_{RxD} = 400 μA	0	–	$0.2 \times V_{CC}$	V
Receiver Threshold Voltage, recessive to dominant edge	–	$0.4 \times V_S$	$0.46 \times V_S$	–	V
Receiver Threshold Voltage, dominant to recessive edge	–	–	$0.54 \times V_S$	$0.6 \times V_S$	V
Receiver Hysteresis	–	–	$0.08 \times V_S$	–	V
TxD High Level Threshold Voltage	–	–	$0.5 \times V_{CC}$ +0.4 V	$0.7 \times V_{CC}$	V
TxD Low Level Threshold Voltage	–	$0.3 \times V_{CC}$	$0.5 \times V_{CC}$ −0.4 V	–	–
TxD Hysteresis	–	–	800	–	mV
TxD Pull Up Current	TxD = 0 V	−150	−100	−80	μA
Bus Recessive Output Voltage	TxD = V_{CC}	$0.8 \times V_S$	V_S	–	V
Bus Dominant Output Voltage	TxD = 0 V	0	–	$0.2 \times V_S$	V
Bus Short Circuit Current	Bus = 13.5 V	40	70	110	mA
Bus Leakage Current	V_{CC} = 0 V, V_S = 0 V, Bus = −12 V V_{CC} = 0 V, V_S = 0 V, Bus = 20 V	−750 –	−350 0	– 5.0	μA
Bus Pull Up Resistance	–	20	30	47	kΩ
Bus Wake–up Threshold Voltage	–	$0.4 \times V_S$	–	$0.7 \times V_S$	V
EN High Level Threshold Voltage	–	–	$0.5 \times V_{CC}$ +0.4 V	$0.7 \times V_{CC}$	V
EN Low Level Threshold Voltage	–	$0.3 \times V_{CC}$	$0.5 \times V_{CC}$ −0.4 V	–	V
EN Pull Down Resistance	–	15	30	60	kΩ
INH High Level Drop Voltage, ΔINH = V_S − INH	I_{INH} = −0.15 mA	–	0.05	0.5	V
INH Leakage Current	Sleep Mode, INH = 0 V	−5.0	0	5.0	μA

1. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be 100% parametrically tested in production.
2. Sum of current into V_{CC} and EN pins.
3. Sum of current into Bus and V_S pins. V_S = V_{BUS} ≤ 12 V, I_Q = I_S + I_{BUS}.

NCV7310

SWITCHING CHARACTERISTICS ($4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$, $6.0 \text{ V} \leq V_S \leq 20 \text{ V}$, $R_T = 1.0 \text{ k}\Omega$, $EN = V_{CC}$, $-40°C \leq T_J \leq 125°C$; unless otherwise specified. Note 4. See Figures 4 and 5.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Bus Falling Edge Slew Rate	80% to 20%, $C_{Bus} = 3.3$ nF, $V_{CC} = 5.0$ V, $V_S = 13.5$ V	−3.0	−2.0	−1.0	V/μs
Bus Rising Edge Slew Rate	20% to 80%, $C_{Bus} = 3.3$ nF, $V_{CC} = 5.0$ V, $V_S = 13.5$ V	1.0	1.5	3.0	V/μs
Propagation Delay, TxD Low to RxD Low, $t_{d(L)TR}$ (Recessive to Dominant)	$C_{Bus} = 3.3$ nF, $C_{RxD} = 20$ pF, $V_{CC} = 5.0$ V, $V_S = 13.5$ V	2.0	5.0	10	μs
Propagation Delay, TxD High to RxD High, $t_{d(H)TR}$ (Dominant to Recessive)	$C_{Bus} = 3.3$ nF, $C_{RxD} = 20$ pF, $V_{CC} = 5.0$ V, $V_S = 13.5$ V	2.0	5.0	10	μs
Propagation Delay, TxD Low to Bus Low, $t_{d(L)T}$	$C_{Bus} = 3.3$ nF, $V_{CC} = 5.0$ V	–	1.0	4.0	μs
Propagation Delay, TxD High to Bus High, $t_{d(H)T}$	$C_{Bus} = 3.3$ nF, $V_{CC} = 5.0$ V	–	1.0	4.0	μs
Propagation Delay, Bus Dominant (Low) to RxD Low, $t_{d(L)R}$	$C_{Bus} = 3.3$ nF, $C_{RxD} = 20$ pF, $V_{CC} = 5.0$ V	–	1.0	4.0	μs
Propagation Delay, Bus Recessive (High) to RxD High, $t_{d(H)R}$	$C_{Bus} = 3.3$ nF, $C_{RxD} = 20$ pF, $V_{CC} = 5.0$ V	–	1.0	4.0	μs
Receiver Delay Symmetry	–	−2.0	–	2.0	μs
Transmitter Delay Symmetry	–	−2.0	–	2.0	μs
Wake–up Delay Time	–	30	70	110	μs

4. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be 100% parametrically tested in production.

PIN FUNCTION DESCRIPTION

| PACKAGE PIN # 8 Lead SOIC	PIN SYMBOL	FUNCTION
1	RxD	Receive data output. Transmit data also loops back on this pin.
2	EN	Enable input. Internal 30 kΩ pull down resistor. Transceiver in normal mode when high.
3	V_{CC}	5.0 V supply input.
4	TxD	Transmit data input. Internal pull up current source (100μA).
5	GND	Ground.
6	Bus	Bus Input/Output. Internal pull up resistor (30 kΩ) through a diode (protection when V_S is low).
7	V_S	Battery supply input.
8	INH	Inhibit Output. For use with external regulator. Goes high with wakeup signal on Bus.

NCV7310
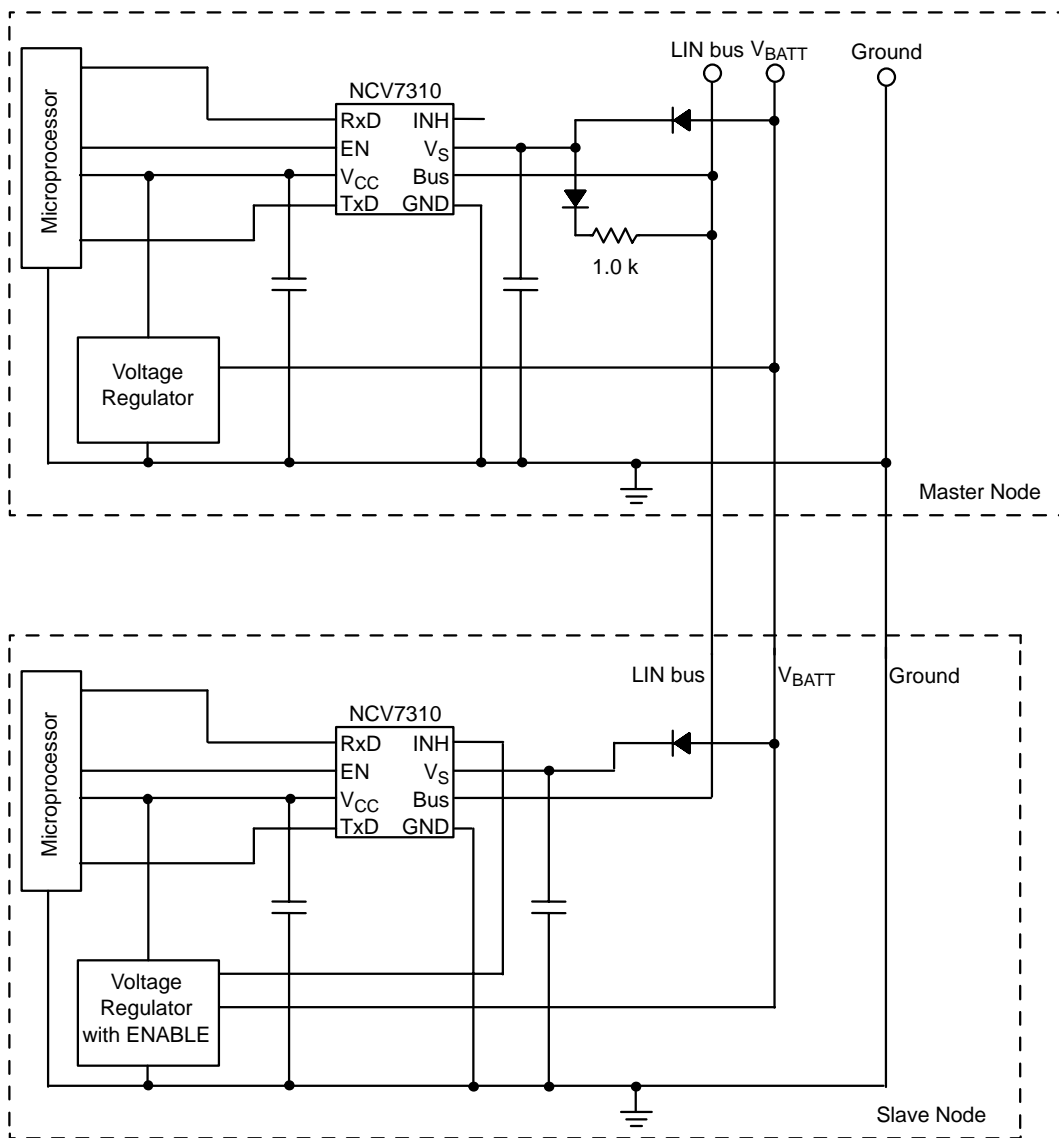
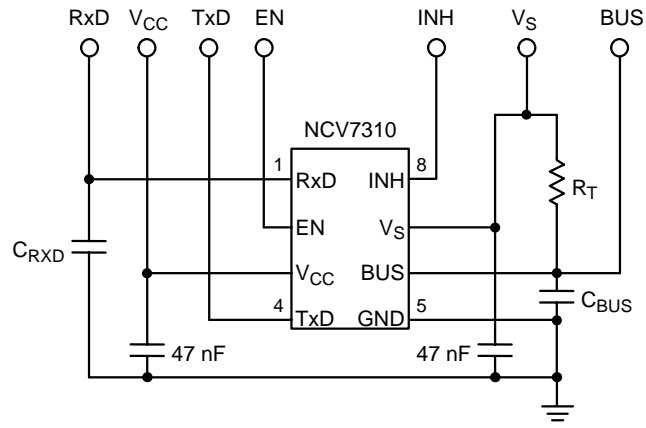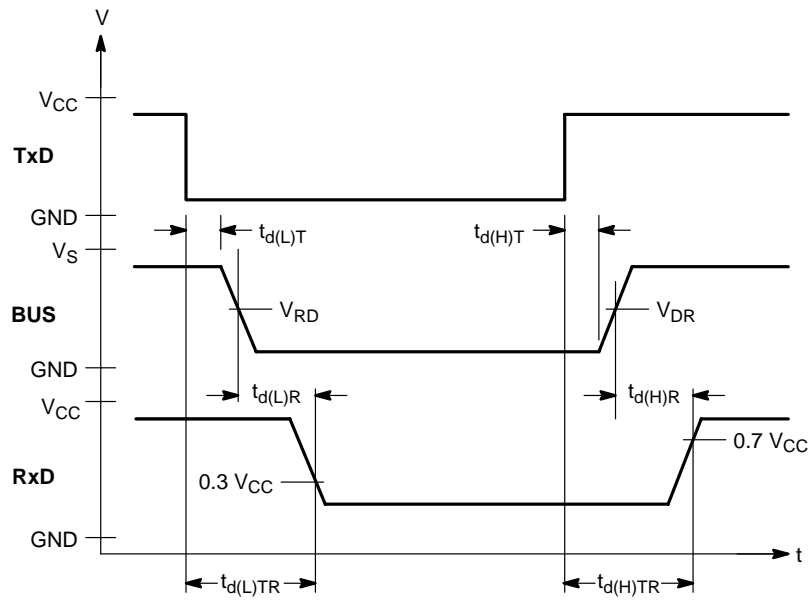**Figure 3. Application Diagram**

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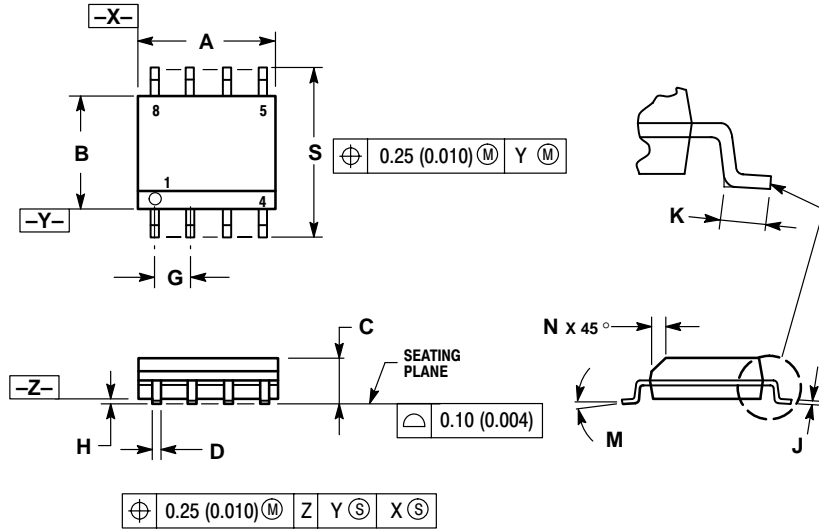

Figure 4. Test Circuit

Figure 5. Switching Characteristics Timing Diagram

PACKAGE DIMENSIONS

SO–8
D SUFFIX
CASE 751–07
ISSUE V

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ | 0.25 (0.010) Ⓜ | Y Ⓜ

⊕ | 0.25 (0.010) Ⓜ | Z | Y Ⓢ | X Ⓢ

SEATING PLANE

◁ | 0.10 (0.004)

N X 45°

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

NCV7310

PUBLICATION ORDERING INFORMATION