# PNC28C256

## CMOS/SNOS EEPROM
## HIGH PERFORMANCE 32K×8 ELECTRICALLY ERASABLE PROM

The PNC28C256 is a high performance EEPROM fabricated with Plessey Semiconductors' proprietary CMOS/SNOS technology. This full-featured device follows the JEDEC-approved pinout and 5V-only operation standard for 32K×8 EEPROMs.

The PNC28C256 features single and multi-byte page write cycles. Internal latches allow a byte load cycle time as fast as the read cycle time. Writing of latched data into the non-volatile cells is self-timed, resulting in an effective write time of 160$\mu$s/byte. Other features include software data protection, $\overline{\text{DATA}}$ polling and toggle bit early end-of-write detection, as well as chip erase and chip program mode.

All devices are margin mode tested to a standard of 10 years data retention after $10^5$ write cycles. Margin mode testing may be performed by the user to predict data retention.

### FEATURES

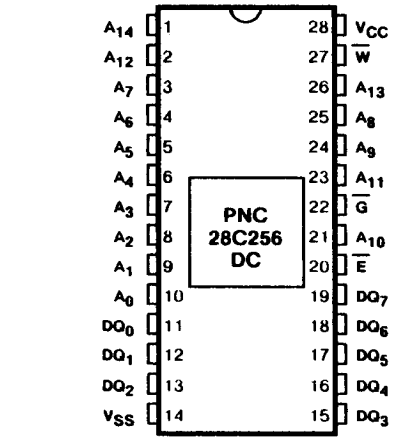
- 70ns (PNC28C256-70), 90ns (PNC28C256-90) and 120ns (PNC28C256-12) Access Times
- Self-Timed Page Write
- Single 5V ±10% Operation
- 160$\mu$s/Byte Effective Write Time
- 80mA Active Current
- 150$\mu$A Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling
- Toggle Bit
- 10 Year Retention at $10^5$ Write Cycles
- 10ms Chip Erase and Chip Program
- Margin Mode
- JEDEC Standard Pinout and Operation

### ABSOLUTE MAXIMUM RATINGS

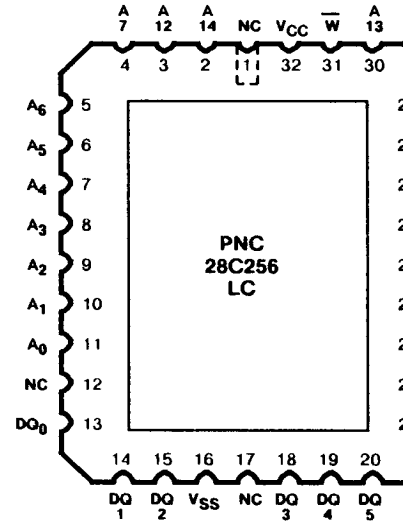
| | |
|---|---|
| Voltage on typical input relative to $V_{SS}$ | -0.6V to 7.0V |
| Voltage on $DQ_{0-7}$ and $\overline{W}$ | -0.5V to ($V_{CC}$ + 0.5V) |
| Temperature under bias | -55°C to + 125°C |
| Storage temperature | -65°C to + 150°C |
| Power dissipation | 1W |
| DC output current | 15mA |
| (one output at a time, one second duration) | |

**Note**

Stresses greater than those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at any other conditions than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.




DC28




LC32

| Pin Name | Function |
|---|---|
| $A_0$-$A_{14}$ | Address inputs |
| $\overline{W}$ | Write enable |
| $DQ_0$-$DQ_7$ | Data in/out |
| $\overline{E}$ | Chip enable |
| $\overline{G}$ | Output enable |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |

*Fig.1 Pin connections (not to scale) - top views*

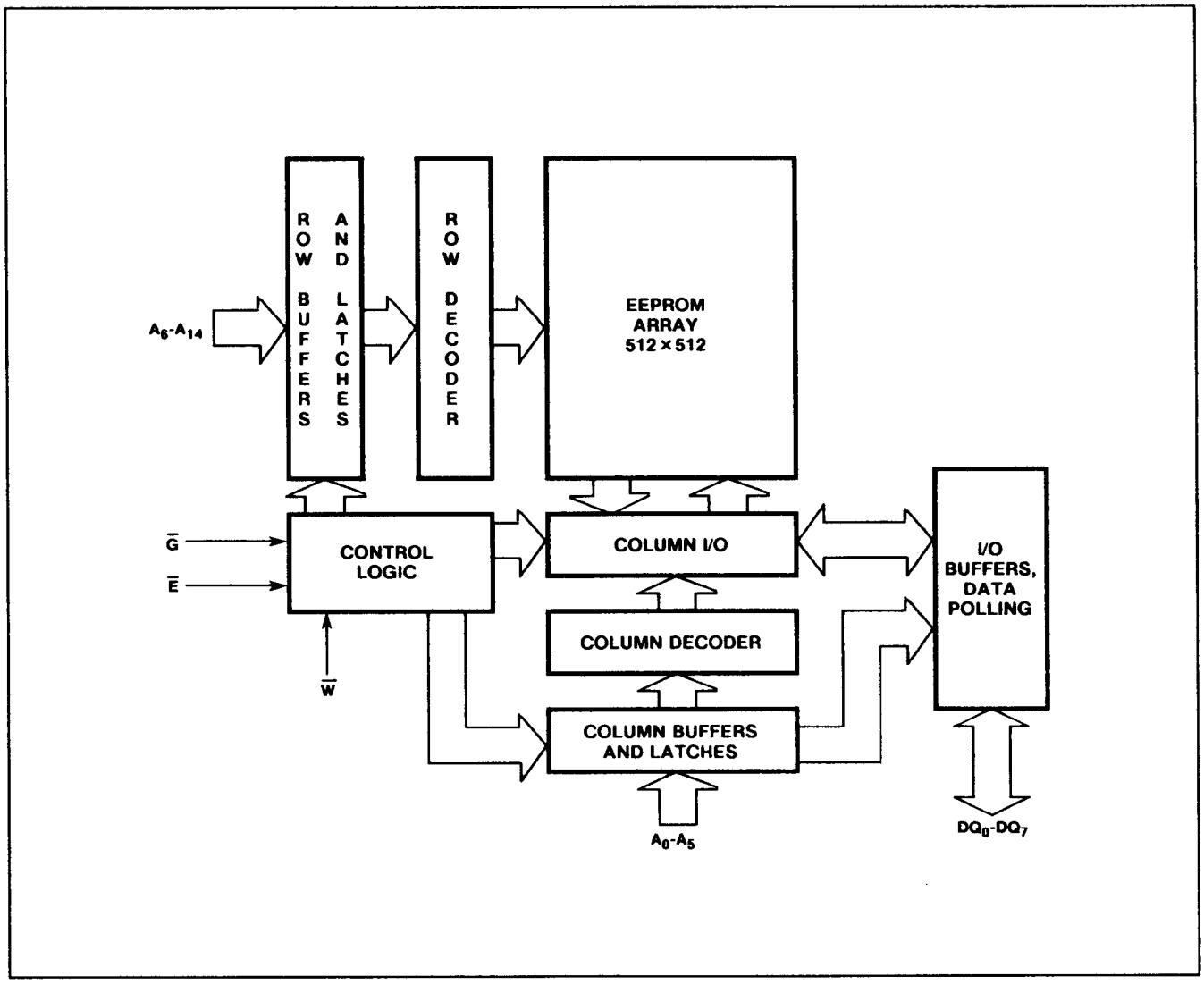



*Fig.2 Logic block diagram*

## DC OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | $V_{CC}$ to $V_{SS}$ |
| Input logic '1' voltage | $V_{IH}$ | 2.0 | | $V_{CC}+0.5$ | V | All Inputs |
| Input logic '0' voltage | $V_{IL}$ | -0.5 | | 0.8 | V | All Inputs |
| Ambient operating teperature | $T_{AMB}$ | 0 | | 70 | °C | |

## DC ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 0°C to +70°C, $V_{CC}$ = +5V ± 10%

| Characteristic | Symbol | Value | | Units | Conditions | |
|---|---|---|---|---|---|---|
| | | Min. | Max. | | | |
| $V_{CC}$ power supply current (Active, cycling TTL input levels) | $I_{CC}$ | | 80 | mA | $t_{AVAX}$ = 70ns | $\overline{E} = \overline{G} = V_{IL}$ |
| | | | 70 | mA | $t_{AVAX}$ = 90ns | $\overline{W} = V_{IH}$ |
| | | | 60 | mA | $t_{AVAX}$ = 120ns | $DQ_{0-7}$ open |
| $V_{CC}$ power supply current (standby, cycling TTL input levels) | $I_{SB1}$ | | 1.5 | mA | $\overline{E} = V_{IH}$ | |
| $V_{CC}$ power supply current (standby,stable CMOS input levels) | $I_{SB2}$ | | 150 | μA | $\overline{E} \geq (V_{CC}-0.2V)$ $V_{IN} \leq 0.2V$ or $\geq (V_{CC}-0.2V)$ | |
| Input leakage current | $I_{ILK}$ | | ±5 | μA | $V_{IN}$ = 0V to $V_{CC}$ | |
| Output leakage current | $I_{OLK}$ | | ±10 | μA | $\overline{E} = V_{IH}$, $V_{IN}$ = 0V to $V_{CC}$ | |
| Output logic '1' voltage | $V_{OH}$ | 2.4 | | V | $I_{OH}$ = -2mA | |
| Output logic '0' voltage | $V_{OL}$ | | 0.4 | V | $I_{OL}$ = 4mA | |
| Write inhibit supply voltage | $V_{WI}$ | 3.2 | 3.8 | V | | |
| Supervoltage | $V_H$ | 12 | 14 | V | | |

## MODE SELECTION (See notes 1 and 2)

| Mode | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | $DQ_{0-7}$ | Power |
|---|---|---|---|---|---|
| Standby | H | X | X | High Z | Standby |
| Read | L | L | H | $D_{OUT}$ | Active |
| Byte or page write | L | H | L | $D_{IN}$ | Active |
| Write inhibit | X | X | H | High Z or $D_{OUT}$ | Active |
| Write inhibit | X | L | X | High Z or $D_{OUT}$ | Active |
| Chip erase | L | $V_H$ | L | $D_{IN} = V_{IL}$ | Active |
| Chip program | L | $V_H$ | L | $D_{IN} = V_{IH}$ | Active |

NOTES
1. H = high TTL level; L = low TTL level; X = H or L
2. For information on Margin Mode, contact Plessey Semiconductors

## TYPICAL POWER-UP TIMING (See notes 3 and 4)

| Symbol | Parameter | Typ. | Units |
|---|---|---|---|
| $t_{PUR}$ | Power-up to read operation | 100 | μs |
| $t_{PUW}$ | Power-up to write operation | 5 | ms |

NOTES
3. $T_A$ = 25°C and $V_{CC}$ = 5.0V
4. These parameters are periodically characterised but not 100% tested

## CAPACITANCE $T_{amb}$ = 25°C, f = 1.0MHz (See note 4)

| Parameter | Symbol | Max. | Units | Conditions |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | 6 | pF | ΔV = 0 to 3V |
| Output capacitance | $C_{OUT}$ | 12 | pF | ΔV = 0 to 3V |

## AC TEST CONDITIONS

| | |
|---|---|
| Input pulse levels | 0V to 3V |
| Input rise and fall times | ≤5ns |
| Input and output timing reference levels | 1.5V |
| Output load | See Fig.3 |

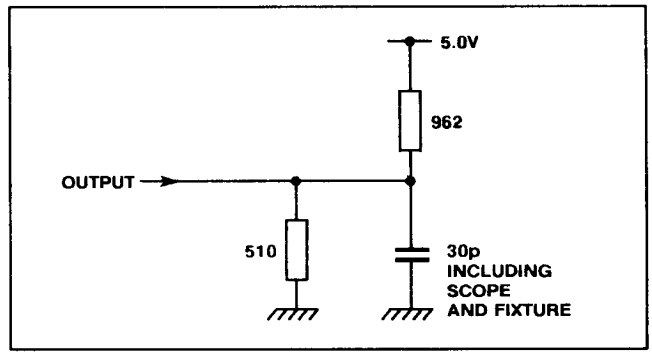



*Fig.3 AC Output loading*

## AC CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = 0°C to +70°C, $V_{CC}$ = +5V ± 10%.

**READ CYCLE** (See note 8)

| Symbol | | Parameter | PNC28C256-70 | | PNC28C256-90 | | PNC28C256-12 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Standard | Alternative | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{AVAX}$ | $t_{RC}$ | Read cycle time | 70 | | 90 | | 120 | | ns | |
| $t_{ELQV}$ | $t_{CE}$ | Chip enable access time | | 70 | | 90 | | 120 | ns | |
| $t_{AVQV}$ | $t_{AA}$ | Address access time | | 70 | | 90 | | 120 | ns | |
| $t_{GLQV}$ | $t_{OE}$ | Output enable access time | | 35 | | 40 | | 50 | ns | |
| $t_{ELQX}$ | $t_{LZ}$ | $\overline{E}$ low to active output | 0 | | 0 | | 0 | | ns | 5 |
| $t_{GLQX}$ | $t_{OLZ}$ | $\overline{G}$ low to active output | 0 | | 0 | | 0 | | ns | |
| $t_{EHQZ}$ | $t_{HZ}$ | $\overline{E}$ high to high-Z output | | 35 | | 40 | | 50 | ns | 6 |
| $t_{GHQZ}$ | $t_{OHZ}$ | $\overline{G}$ high to high-Z output | | 35 | | 40 | | 50 | ns | 6 |
| $t_{AXQX}$ | $t_{OH}$ | Address invalid to data out invalid | 0 | | 0 | | 0 | | ns | |
| $t_{WHQVC}$ | | $\overline{DATA}$ polling access time | | 70 | | 90 | | 120 | ns | 7 |

NOTES

5. $\overline{G}$ is low before $\overline{E}$ goes low
6. Measured ±200mV from steady state output voltage. Load capacitance is 5pF
7. Refer to Fig.10
8. $\overline{E}$,$\overline{G}$ and $\overline{W}$ must make the transition between $V_{IH}$(min) to $V_{IL}$(max), or $V_{IL}$(max) to $V_{IH}$(min) in a monotonic fashion

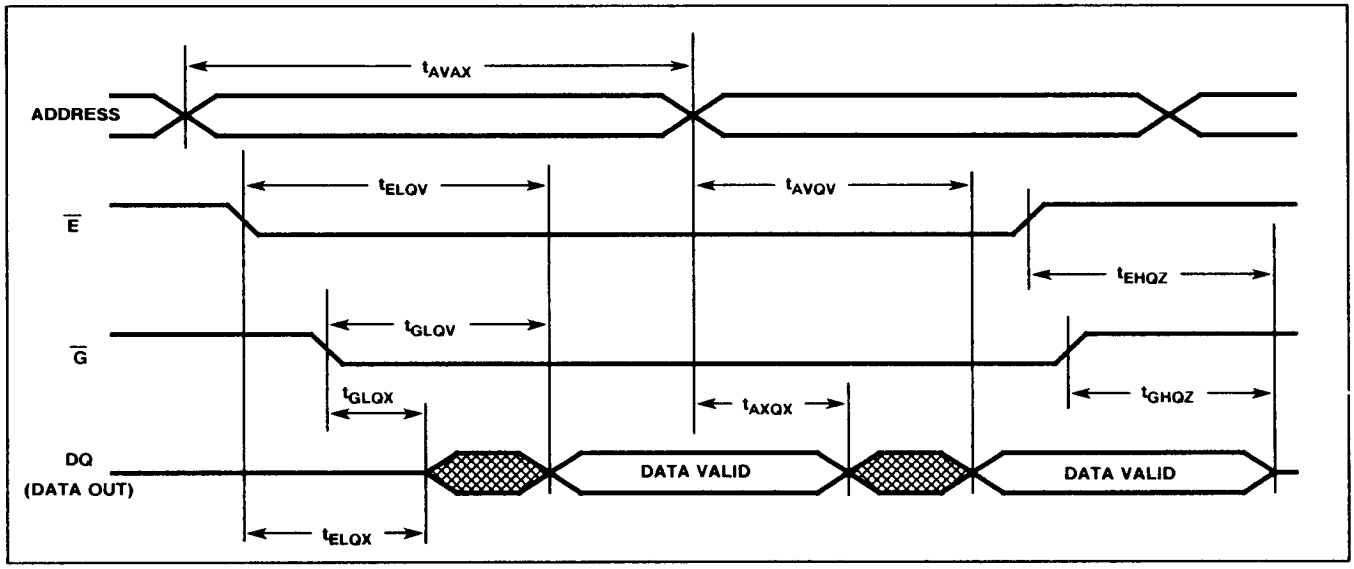



*Fig.4 READ cycle timing diagram (see notes 5, 6 and 8)*

**BYTE/PAGE WRITE CYCLE 1: $\overline{W}$ CONTROLLED** (See note 8)

| Symbol | | Parameter | PNC28C256-70 | | PNC28C256-90 | | PNC28C256-12 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Standard | Alternative | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{WLWLB}$ | $t_{WC}$ | Write cycle time | | 10 | | 10 | | 10 | ms | |
| $t_{WVWLP}$ | $t_{BLC}$ | Byte load cycle time | 70 | | 90 | | 120 | | ns | 10 |
| | | | | 200 | | 200 | | 200 | $\mu$s | 10 |
| $t_{AVWL}$ | $t_{AS}$ | Address set-up time | 0 | | 0 | | 0 | | ns | |
| $t_{WLAX}$ | $t_{AH}$ | Address hold time | 35 | | 45 | | 60 | | ns | |
| $t_{GHWL}$ | $t_{OES}$ | $\overline{G}$ high to $\overline{W}$ low time | 10 | | 10 | | 10 | | ns | |
| $t_{WHGL}$ | $t_{OEH}$ | $\overline{G}$ high hold time from $\overline{W}$ high | 10 | | 10 | | 10 | | ns | |
| $t_{WLWH}$ | $t_{WP}$ | Write pulse duration | 45 | | 60 | | 80 | | ns | 9,12 |
| $t_{GLWL}$ | | $\overline{G}$ low write inhibit setup time | 10 | | 10 | | 10 | | ns | |
| $t_{DVWH}$ | $t_{DS}$ | Data set-up time | 45 | | 45 | | 45 | | ns | |
| $t_{WHDX}$ | $t_{DH}$ | Data hold time | 0 | | 0 | | 0 | | ns | |
| $t_{ELWL}$ | $t_{CS}$ | $\overline{E}$ set-up time to $\overline{W}$ low | 0 | | 0 | | 0 | | ns | |
| $t_{WHEH}$ | $t_{CH}$ | $\overline{E}$ hold time from $\overline{W}$ high | 0 | | 0 | | 0 | | ns | |
| $t_{WHWL}$ | $t_{WPH}$ | $\overline{W}$ high to $\overline{W}$ low time | 25 | | 30 | | 40 | | ns | 10,12 |
| $t_{WHWLT}$ | | $\overline{W}$ high timeout | 100 | | 100 | | 100 | | $\mu$s | 11 |

NOTES
9. $\overline{W}$ and $\overline{E}$ are noise protected. A write pulse of less than 7ns (typical) will not activate a write cycle
10. Refer to Fig. 7
11. This is the minimum time the internal timer waits before initiating the erase/program portion of the write cycle
12. During a page write cycle, the maximum pulse duration allowed is 100$\mu$s

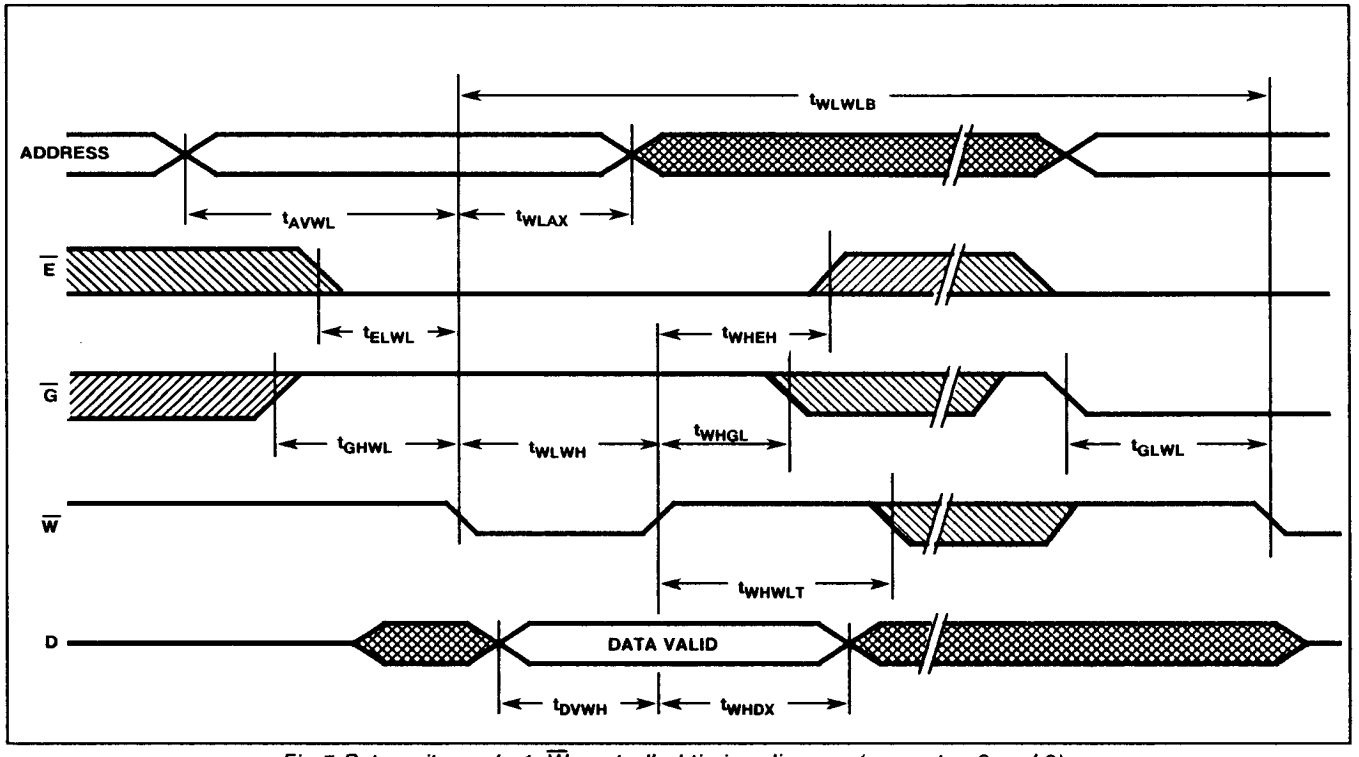



*Fig.5 Byte write cycle 1: $\overline{W}$ controlled timing diagram (see notes 8 and 9)*

**BYTE/PAGE WRITE CYCLE 2: $\overline{E}$ CONTROLLED** (See note 8)

| Symbol | | Parameter | PNC28C256-70 | | PNC28C256-90 | | PNC28C256-12 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Standard | Alternative | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{ELELB}$ | $t_{WC}$ | Write cycle time | 10 | | 10 | | 10 | | ns | |
| $t_{ELELP}$ | $t_{BLC}$ | Byte load cycle time | 70 | 200 | 90 | 200 | 120 | 200 | ns<br>$\mu$s | 13<br>13 |
| $t_{AVEL}$ | $t_{AS}$ | Address set-up time | 0 | | 0 | | 0 | | ns | |
| $t_{ELAX}$ | $t_{AH}$ | Address hold time | 35 | | 45 | | 60 | | ns | |
| $t_{GHEL}$ | $t_{OES}$ | $\overline{G}$ high to $\overline{E}$ low time | 10 | | 10 | | 10 | | ns | |
| $t_{EHGL}$ | $t_{OEH}$ | $\overline{G}$ high hold time from $\overline{E}$ high | 10 | | 10 | | 10 | | ns | |
| $t_{ELEH}$ | $t_{WP}$ | Write pulse duration | 45 | | 60 | | 80 | | ns | 9,12 |
| $t_{GLEL}$ | | $\overline{G}$ low write inhibit setup time | 10 | | 10 | | 10 | | ns | |
| $t_{DVEH}$ | $t_{DS}$ | Data set-up time | 45 | | 45 | | 45 | | ns | |
| $t_{EHDX}$ | $t_{DH}$ | Data hold time | 0 | | 0 | | 0 | | ns | |
| $t_{WLEL}$ | $t_{CS}$ | $\overline{W}$ set-up time to $\overline{E}$ low | 0 | | 0 | | 0 | | ns | |
| $t_{EHWH}$ | $t_{CH}$ | $\overline{W}$ hold time from $\overline{E}$ high | 0 | | 0 | | 0 | | ns | |
| $t_{EHEL}$ | $t_{WPH}$ | $\overline{E}$ high to $\overline{E}$ low time | 25 | | 30 | | 40 | | ns | 12,13 |
| $t_{EHELT}$ | | $\overline{E}$ high timeout | 100 | | 100 | | 100 | | $\mu$s | 11 |

NOTE
13. Refer to Fig. 8

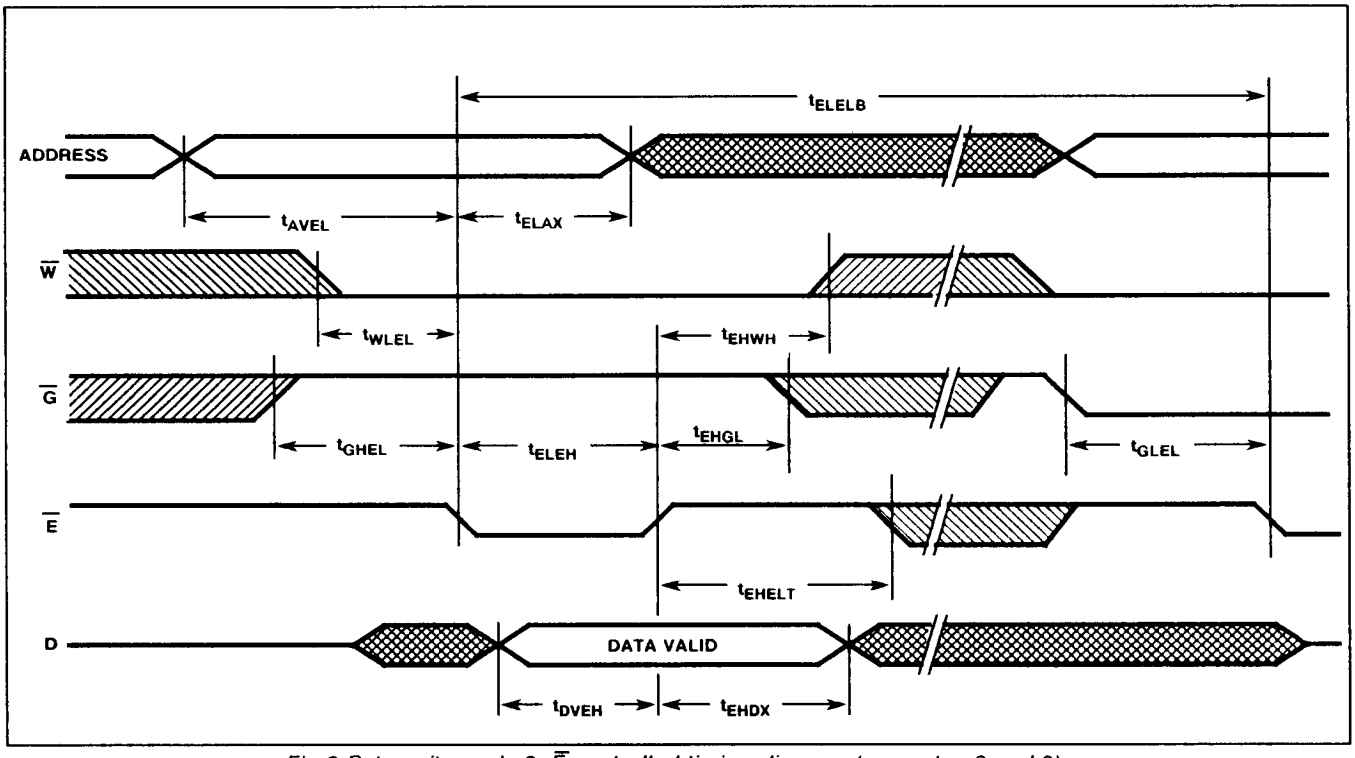



*Fig.6 Byte write cycle 2: $\overline{E}$ controlled timing diagram (see notes 8 and 9)*

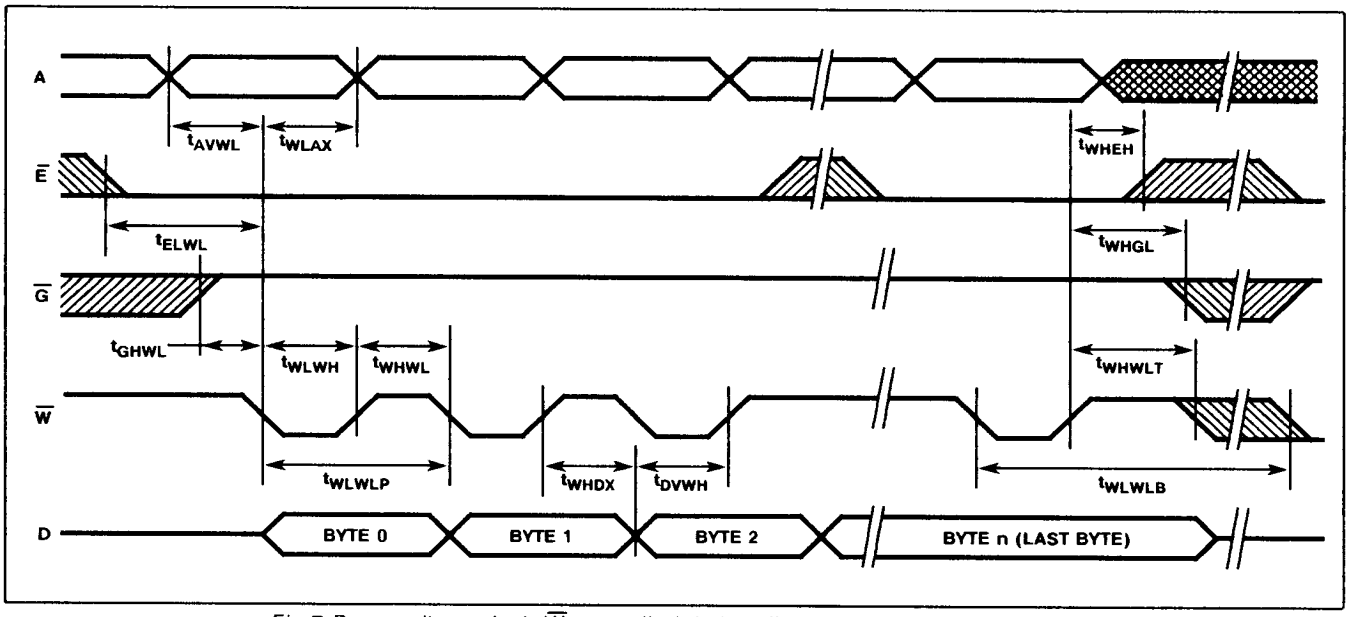



*Fig.7 Page write cycle 1: $\overline{W}$ controlled timing diagram (see notes 8 and 9)*

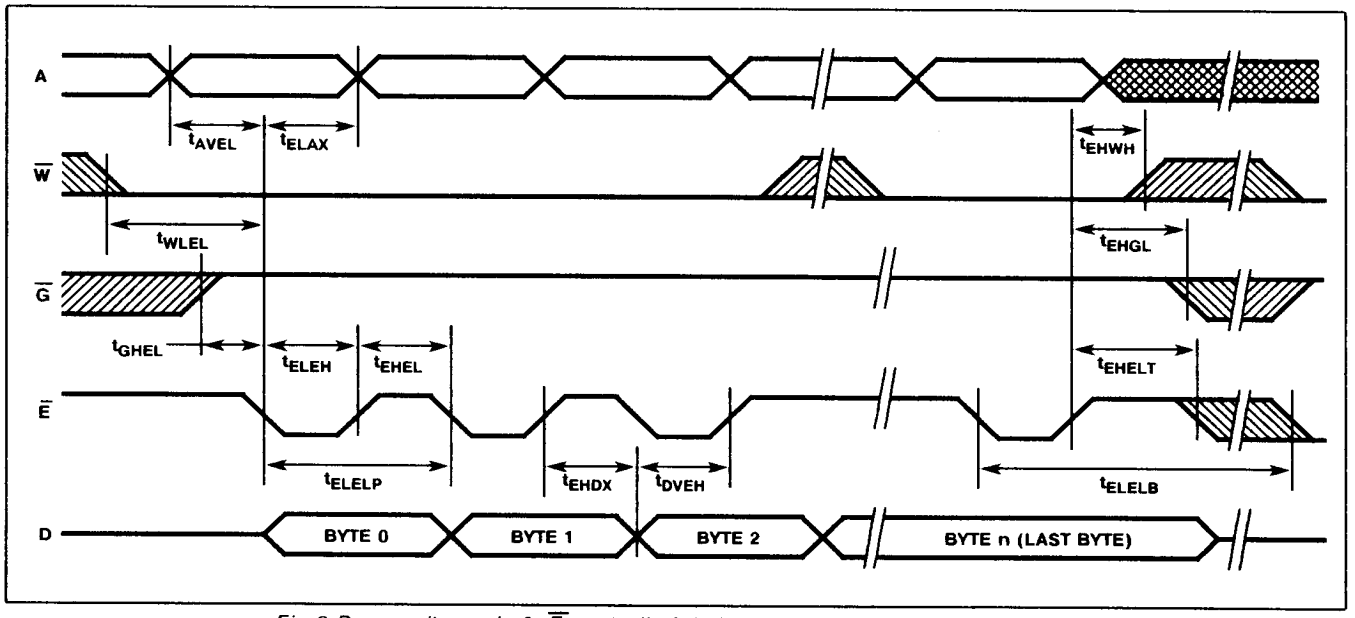



*Fig.8 Page write cycle 2: $\overline{E}$ controlled timing diagram (see notes 8 and 9)*

**CHIP ERASE/PROGRAM CYCLE** (See note 14)

| Symbol | Parameter | PNC28C256-70 | | PNC28C256-90 | | PNC28C256-12 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{BELGH}$ | Chip enable set-up to $\overline{G}$ at $V_H$ | 0 | | 0 | | 0 | | ns | |
| $t_{BGHDX}$ | Data hold after $\overline{G}$ at $V_H$ | 100 | | 100 | | 100 | | µs | |
| $t_{BWLWH}$ | $\overline{W}$ pulse width | 10 | | 10 | | 10 | | ms | |
| $t_{BWHGL}$ | $\overline{W}$ recovery | 20 | | 20 | | 20 | | µs | |
| $t_{BDVGH}$ | Data set-up to $\overline{G}$ at $V_H$ | 0 | | 0 | | 0 | | ns | 14 |
| $t_{BGHWL}$ | $\overline{G}$ at $V_H$ to $\overline{W}$ low | 5 | | 5 | | 5 | | µs | |

NOTE

14. When $DQ_{0-7}$ are high, all memory cells are written to a '1' state; when $DQ_{0-7}$ are low, all memory cells are written to a '0' state.

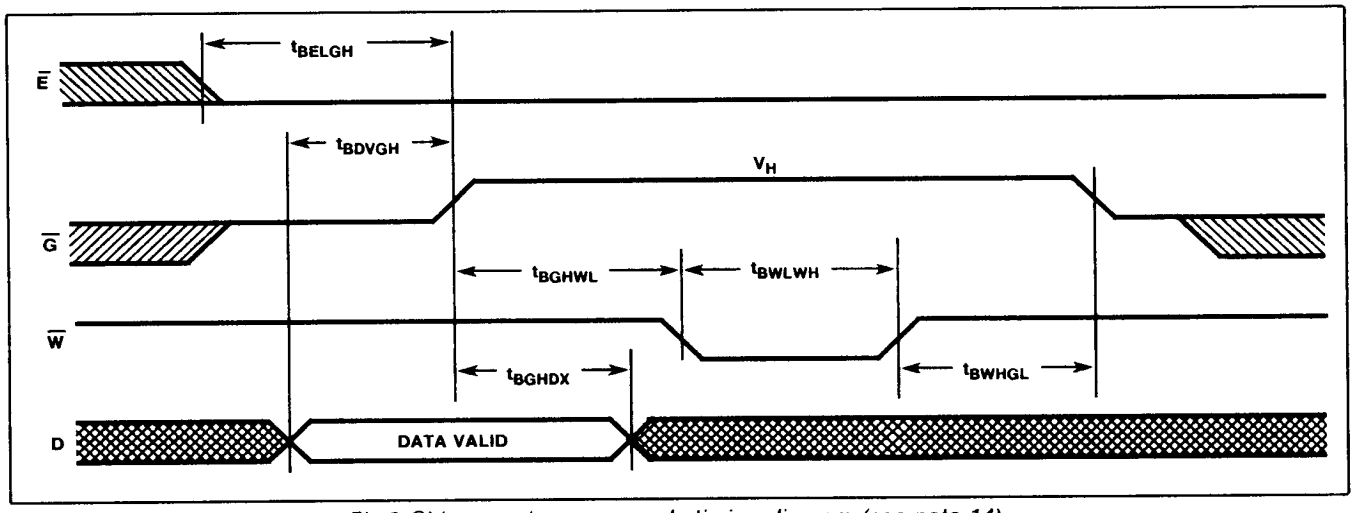



*Fig.9 Chip erase/program cycle timing diagram (see note 14)*

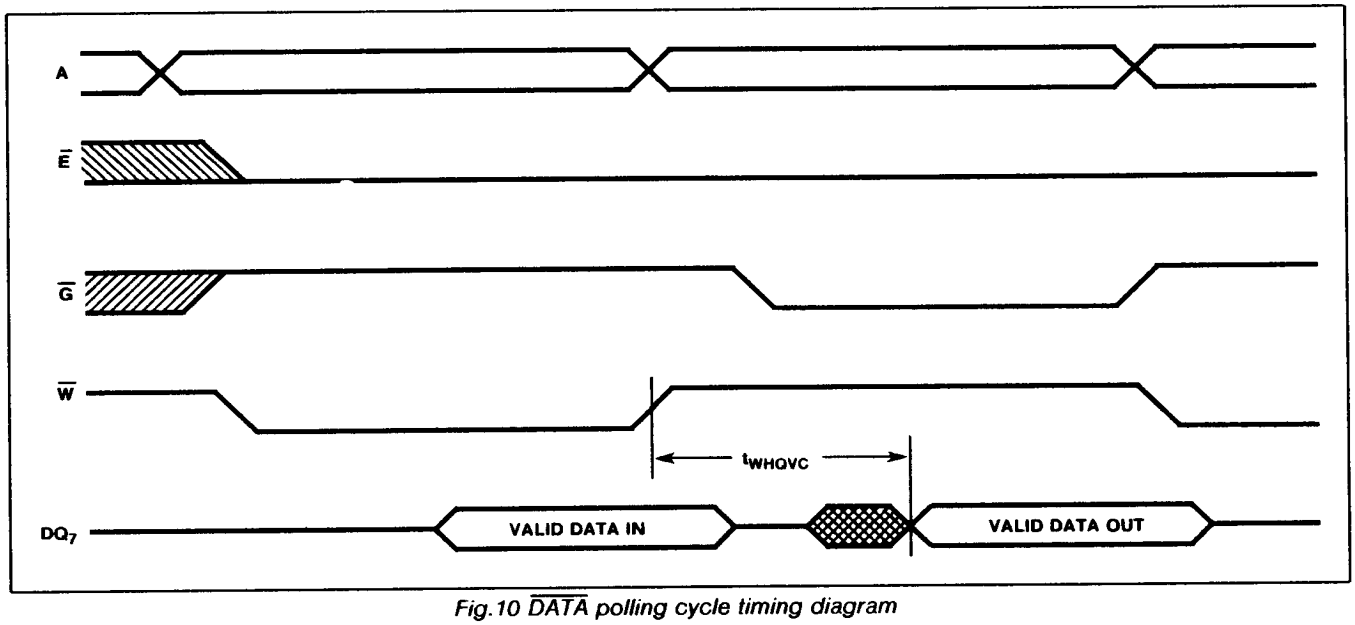



*Fig.10 $\overline{DATA}$ polling cycle timing diagram*

## DEVICE OPERATION

### READ

The read operation is identical to a static RAM. When $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ is HIGH, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are in a high impedance state whenever $\overline{E}$ or $\overline{G}$ is HIGH.

### BYTE and PAGE WRITE

A low pulse on $\overline{W}$ ($\overline{E}$ LOW), or $\overline{E}$ ($\overline{W}$ LOW), while G is HIGH initiates a write cycle. The address is latched on the falling edge of $\overline{W}$ or $\overline{E}$, whichever occurs last. The data is latched on the rising edge of $\overline{W}$ or $\overline{E}$, whichever occurs first. At that same transition, an internal timer is started. This timer restarts upon any $\overline{W}$ or $\overline{E}$ transition occurring before the end of the time-out period. If no additional write cycles are detected and the internal timer reaches the end of the time-out period, then the erase/program portion of the write cycle begins. After this time further write attempts are ignored.

There are 64 bytes in one page. The address of the pages are specified with pins $A_{6-14}$. These addresses are latched at the beginning of the page cycle in order to prevent inadvertent page changes. The remaining addresses ($A_{0-5}$) are used to specify bytes within each page.

### Hardware Protection

The PNC28C256 offers three hardware protection features:

1. $V_{CC}$ sense - writing is inhibited below a specified $V_{CC}$ power supply level $V_{WI}$
2. Noise filter - when the $\overline{W}$ or $\overline{E}$ pulse is shorter than 7ns, the write cycle is successfully aborted, and the data remains unchanged
3. Write inhibit - Holding $\overline{G}$ low, $\overline{E}$ high or $\overline{W}$ high inhibits writing.

### Software Protection

Software protection is enabled by performing a 3-byte write operation to specific addresses with specific data. After protection is enabled, the same three write commands must begin each write cycle in order for writing to occur. These commands must obey the page write timing specifications. Once enabled, the software protection feature remains active until a specific 6-byte write operation is performed to disable protection. Power transitions will not disable protection. The software protection circuitry is immune to power disruptions. To enable software protection, the following page load sequence must be executed (data format $DQ_{0-7}$; address format $A_{0-14}$):

1. Load data AA(hex) to address 5555(hex)
2. Load data 55(hex) to address 2AAA(hex)
3. Load data A0(hex) to address 5555(hex)
4. Load data XX(hex) to any Y-address (optional)

The software data protection state is entered at the end of the write period. To disable software protection mode:

1. Load data AA(hex) to address 5555(hex)
2. Load data 55(hex) to address 2AAA(hex)
3. Load data 80(hex) to address 5555(hex)
4. Load data AA(hex) to address 5555(hex)
5. Load data 55(hex) to address 2AAA(hex)
6. Load data 20(hex) to address 5555(hex)
7. Load data XX(hex) to any Y-address (optional)

The software data protection state is exited at the end of the write period. Note that the software protection enable and disable sequences constitute an illegal page write in that the page address is changed within a page write operation. When the PNC28C256 detects one of these sequences, all load commands that are parts of the code information will be ignored and the page address (X-address) following the last code instruction will be latched. A valid page cycle begins at this point.

### $\overline{\text{DATA}}$ Polling

A write cycle may complete in less time than the specified maximum write time. $\overline{\text{DATA}}$ polling may be used to detect early end-of-write. The total time spent writing the array may thereby be minimised. During a byte or page write cycle, attempting to read the last byte written will result in the complement of the written data on $DQ_7$. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the write cycle. If the PNC28C256 is in the software protected state and an illegal write operation is attempted, $\overline{\text{DATA}}$ polling will not show complemented data, indicating a write cycle is NOT in progress.

### Toggle Bit ($DQ_6$)

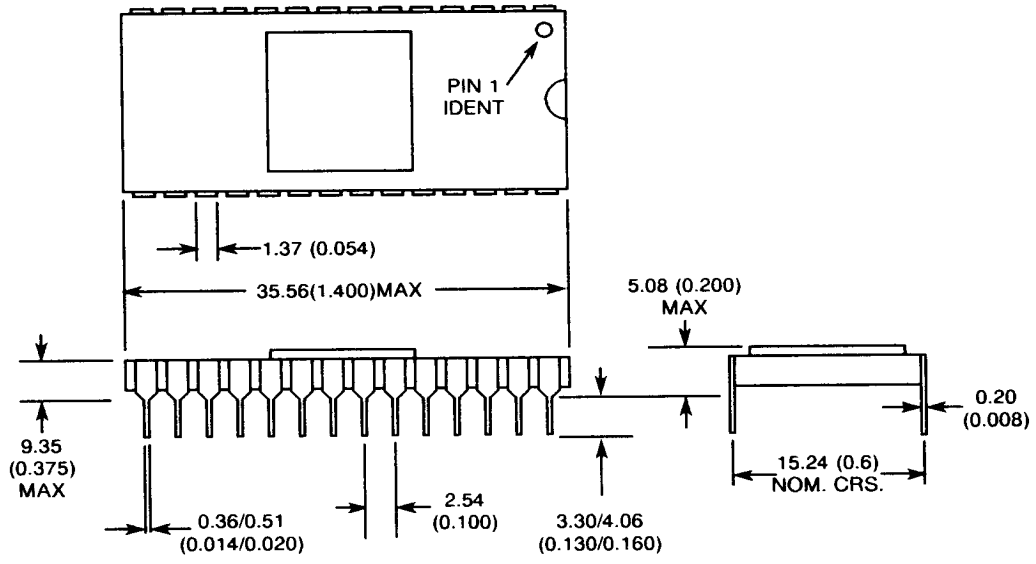
The PNC28C256 provides an additional method for determining when the internal write (erase/program) cycle is complete. During the internal write cycle, $DQ_6$ will toggle from one to a logic zero, and then from a logic zero to a logic one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations. If the PNC28C256 is in the software protected state and an illegal write operation is attempted, toggle bit $DQ_6$ will not toggle, indicating a write cycle is NOT in progress.

### CHIP ERASE and CHIP PROGRAM

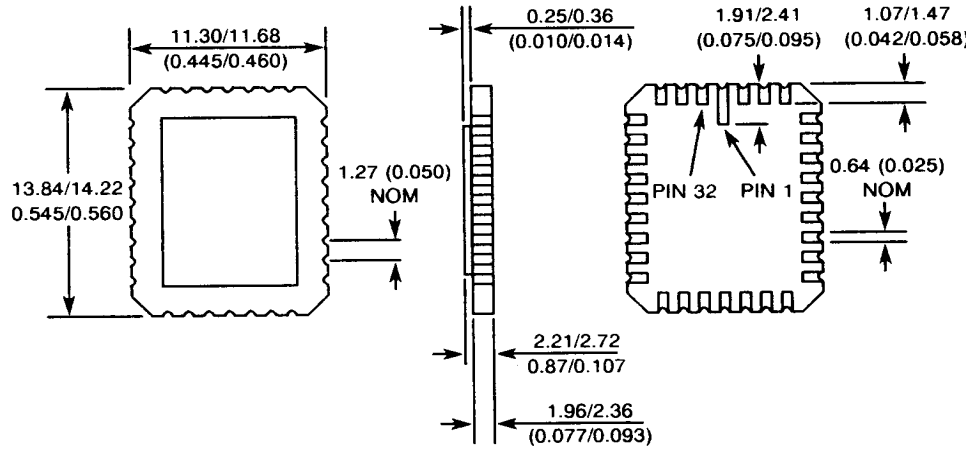
The entire memory may be set to a LOW state by the use of the chip erase operation. By setting $\overline{E}$ LOW, $DQ_{0-7}$ LOW, and $\overline{G}$ to the supervoltage $V_H$, the chip is erased (all cells written LOW) when a 10ms low pulse is applied to the $\overline{W}$ pin. If $DQ_{0-7}$ are set HIGH, all cells are programmed (written HIGH).

## PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information please contact your local Customer Service Centre.




**28-LEAD SIDEBRAZED CERAMIC DIL (0.6in) - DC28**




**32-PIN LEADLESS CHIP CARRIER - LC32**

## ORDERING INFORMATION

**PNC28C256-70 DC** (Commercial - Sidebrazed Ceramic DIL package)
**PNC28C256-90 DC** (Commercial - Sidebrazed Ceramic DIL package)
**PNC28C256-12 DC** (Commercial - Sidebrazed Ceramic DIL package)
**PNC28C256-70 LC** (Commercial - Ceramic LCC package)
**PNC28C256-90 LC** (Commercial - Ceramic LCC package)
**PNC28C256-12 LC** (Commercial - Ceramic LCC package)

PLESSEY
SEMICONDUCTORS

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