



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	3.0 Ω	1.5A	VN0606L

www.DataSheet4U.com

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 30V$
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

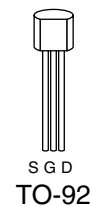
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



Note: See Package Outline section for dimensions.

11/12/01

Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: <http://www.supertex.com>. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-92	0.33A	1.6A	1W	125	170	0.33A	1.6A

* I_D (continuous) is limited by max rated T_J .

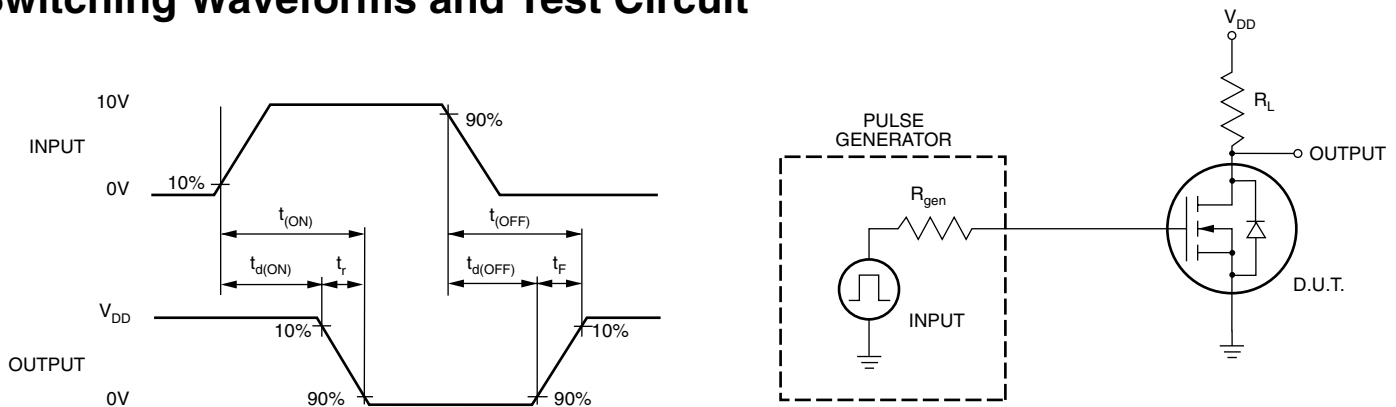
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0V, I_D = 10\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 30V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0V, V_{DS} = 50V$
				500		$V_{GS} = 0V, V_{DS} = 50V,$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	1.5			A	$V_{GS} = 10V, V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	Ω	$V_{GS} = 10V, I_D = 1A$
G_{FS}	Forward Transconductance	170			$\text{m}\Omega$	$V_{DS} = 10V, I_D = 0.5A$
C_{ISS}	Input Capacitance			50	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1\text{ MHz}$
C_{OSS}	Common Source Output Capacitance			25		
C_{RSS}	Reverse Transfer Capacitance			5		
$t_{(ON)}$	Turn-ON Time			10	ns	$V_{DD} = 25V, I_D = 0.6A,$ $R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-OFF Time			10		
V_{SD}	Diode Forward Voltage Drop		0.85		V	$V_{GS} = 0V, I_{SD} = 0.47A$

Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



11/12/01