

54AC/74AC161 • 54ACT/74ACT161 54AC/74AC163 • 54ACT/74ACT163

T-45-23-05

Synchronous Presettable Binary Counter

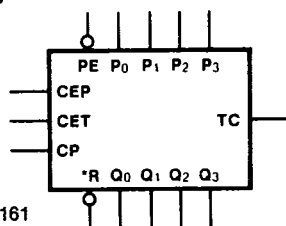
Description

The 'AC/'ACT161 and 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'AC/'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- 'ACT161 and 'ACT163 have TTL-Compatible Inputs

Ordering Code: See Section 6

Logic Symbol

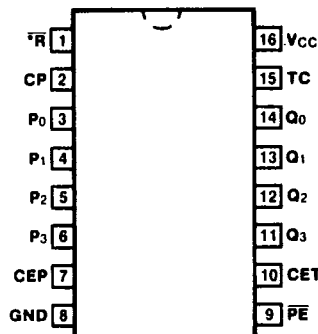


- MR for '161
- SR for '163

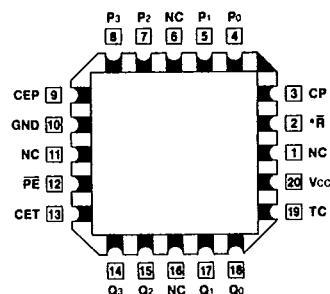
Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
MR ('161)	Asynchronous Master Reset Input
SR ('163)	Synchronous Reset Input
P0 - P3	Parallel Data Inputs
PE	Parallel Enable Input
Q0 - Q3	Flip-Flop Outputs
TC	Terminal Count Output

Connection Diagrams



Pin Assignment
for DIP, Flatpak and SOIC



Pin Assignment
for LCC

- MR for '161
- SR for '163

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Functional Description

The 'AC/ACT161 and 'AC/ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('161), synchronous reset ('163), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, '161), Synchronous Reset ($\overline{SR}$, '163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('161) or $\overline{SR}$ ('163)

HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/ACT161 and 'AC/ACT163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$
 $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$

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Mode Select Table

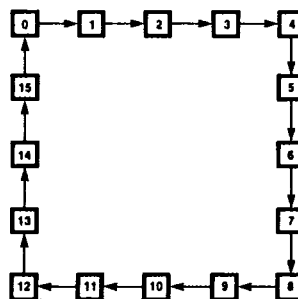
* $\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ($\uparrow$)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '163 only

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

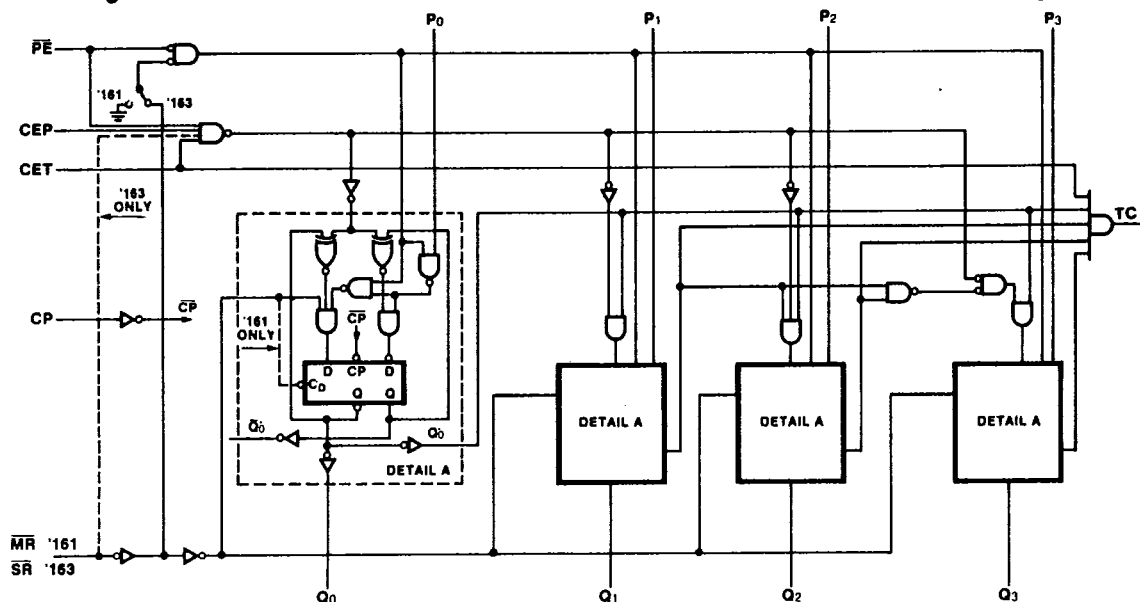
State Diagram

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Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$, $T_A = 25^\circ C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT161/163)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$ $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$

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AC Characteristics

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Symbol	Parameter	Vcc* (V)	74AC161			54AC161		74AC161		Units	Fig. No.
			TA = + 25°C CL = 50 pF			TA = - 55°C to + 125°C CL = 50 pF		TA = - 40°C to + 85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Maximum Count Frequency	3.3 5.0	87 118							MHz	3-3
tPLH	Propagation Delay CP to Qn (PE Input HIGH or LOW)	3.3 5.0	7.5 5.5							ns	3-6
tPHL	Propagation Delay CP to Qn (PE Input HIGH or LOW)	3.3 5.0	8.5 6.0							ns	3-6
tPLH	Propagation Delay CP to TC	3.3 5.0	9.5 7.0							ns	3-6
tPHL	Propagation Delay CP to TC	3.3 5.0	11.0 8.0							ns	3-6
tPLH	Propagation Delay CET to TC	3.3 5.0	7.5 5.5							ns	3-6
tPHL	Propagation Delay CET to TC	3.3 5.0	8.5 6.0							ns	3-6
tPLH	Propagation Delay MR to Qn	3.3 5.0	8.5 6.0							ns	3-6
tPHL	Propagation Delay MR to TC	3.3 5.0	11.0 8.0							ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74AC161		54AC161	74AC161	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Pn to CP	3.3 5.0	5.5 4.0				ns	3-9
th	Hold Time, HIGH or LOW Pn to CP	3.3 5.0	-7.0 -5.0				ns	3-9
ts	Setup Time, HIGH or LOW SR to CP	3.3 5.0	5.5 4.0				ns	3-9
th	Hold Time, HIGH or LOW SR to CP	3.3 5.0	-7.5 -5.5				ns	3-9
ts	Setup Time, HIGH or LOW PE to CP	3.3 5.0	5.5 4.0				ns	3-9
th	Hold Time, HIGH or LOW PE to CP	3.3 5.0	-7.5 -5.5				ns	3-9
ts	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5				ns	3-9
th	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	-4.5 -3.0				ns	3-9
tw	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
tw	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
tw	MR Pulse Width, LOW	3.3 5.0	4.5 3.0				ns	3-6
trec	Recovery Time MR to CP	3.3 5.0	0 0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

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Symbol	Parameter	V _{CC} * (V)	74ACT161			54ACT161		74ACT161		Units	Fig. No.
			T _A = + 25°C C _L = 50 pF			T _A = - 55°C to + 125°C C _L = 50 pF		T _A = - 40°C to + 85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	115	125				100		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	5.5	9.5			1.0	10.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	6.0	10.5			1.0	11.5	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.0			1.0	12.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	12.5			1.0	13.5	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	8.5			1.0	10.0	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	9.5			1.0	10.5	ns	3-6
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.0	6.0	10.0			1.0	11.0	ns	3-6
t _{PHL}	Propagation Delay MR to TC	5.0	1.0	8.0	13.5			1.0	14.5	ns	3-6

*Voltage Range 5.0 Is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74ACT161		54ACT161	74ACT161	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Pn to CP	5.0	4.0	9.5		11.5	ns	3-9
th	Hold Time, HIGH or LOW Pn to CP	5.0	-5.0	0		0	ns	3-9
ts	Setup Time, HIGH or LOW MR to CP	5.0	4.0	8.5		9.5	ns	3-9
th	Hold Time, HIGH or LOW MR to CP	5.0	-5.5	-0.5		-0.5	ns	3-9
ts	Setup Time HIGH or LOW PE to CP	5.0	4.0	8.5		9.5	ns	3-9
th	Hold Time, HIGH or LOW PE to CP	5.0	-5.5	-0.5		-0.5	ns	3-9
ts	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	3-9
th	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0		0	ns	3-9
tw	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0		3.5	ns	3-6
tw	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0		3.5	ns	3-6
tw	MR Pulse Width, LOW	5.0	3.0	3.0		7.5	ns	3-6
trec	Recovery Time MR to CP	5.0	0	0		0.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance	45.0	pF	Vcc = 5.5 V

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AC Characteristics

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Symbol	Parameter	V _{CC} * (V)	74AC163			54AC163		74AC163		Units	Fig. No.
			T _A = + 25°C C _L = 50 pF			T _A = - 55°C to + 125°C C _L = 50 pF		T _A = - 40°C to + 85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0	70 110	87 118				60 95		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0			1.0 1.0	13.5 9.5	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	12.0 9.5			1.0 1.0	13.0 10.0	ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	9.5 7.0	15.0 10.5			1.0 1.0	16.5 11.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	11.0 8.0	14.0 11.0			1.0 1.0	15.5 11.5	ns	3-6
t _{PLH}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	7.5 5.5	9.5 6.5			1.0 1.0	11.0 7.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	8.5 6.0	11.0 8.5			1.0 1.0	12.5 9.5	ns	3-6

*Voltage Range 3.3 Is 3.0 V ± 0.3 V
Voltage Range 5.0 Is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74AC163		54AC163	74AC163	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Pn to CP	3.3 5.0	5.5 4.0	13.5 8.5		16.0 10.5	ns	3-9
th	Hold Time, HIGH or LOW Pn to CP	3.3 5.0	-7.0 -5.0	-1.0 0		-0.5 0	ns	3-9
ts	Setup Time, HIGH or LOW SR to CP	3.3 5.0	5.5 4.0	14.0 9.5		16.5 11.0	ns	3-9
th	Hold Time, HIGH or LOW SR to CP	3.3 5.0	-7.5 -5.5	-1.0 -0.5		-0.5 0	ns	3-9
ts	Setup Time, HIGH or LOW PE to CP	3.3 5.0	5.5 4.0	11.5 7.5		14.0 8.5	ns	3-9
th	Hold Time, HIGH or LOW PE to CP	3.3 5.0	-7.5 -5.0	-1.0 -0.5		-0.5 0	ns	3-9
ts	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5		7.0 5.0	ns	3-9
th	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	-4.5 -3.0	0 0		0 0.5	ns	3-9
tw	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5		4.0 3.0	ns	3-6
tw	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0		4.5 3.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

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Symbol	Parameter	V _{CC} * (V)	74ACT163			54ACT163		74ACT163		Units	Fig. No.
			T _A = + 25°C C _L = 50 pF			T _A = - 55°C to + 125°C C _L = 50 pF		T _A = - 40°C to + 85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Count Frequency	5.0	120	128				105		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	5.5	10.0			1.0	11.0	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n (PE Input HIGH or LOW)	5.0	1.0	6.0	11.0			1.0	12.0	ns	3-6
t _{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.5			1.0	13.5	ns	3-6
t _{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	13.5			1.0	15.0	ns	3-6
t _{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	9.0			1.0	10.5	ns	3-6
t _{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	10.0			1.0	11.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74ACT163		54ACT163	74ACT163	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Pn to CP	5.0	4.0	10.0		12.0	ns	3-9
th	Hold Time, HIGH or LOW Pn to CP	5.0	-5.0	0.5		0.5	ns	3-9
ts	Setup Time, HIGH or LOW SR to CP	5.0	4.0	10.0		11.5	ns	3-9
th	Hold Time, HIGH or LOW SR to CP	5.0	-5.5	-0.5		-0.5	ns	3-9
ts	Setup Time HIGH or LOW PE to CP	5.0	4.0	8.5		10.5	ns	3-9
th	Hold Time, HIGH or LOW PE to CP	5.0	-5.5	-0.5		0	ns	3-9
ts	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	3-9
th	Hold Time, HIGH or LOW CEP or CET to CP	5.0	-3.0	0		0.5	ns	3-9
tw	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5		3.5	ns	3-6
tw	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5		3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance	45.0	pF	Vcc = 5.5 V