REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Change drawing CAGE number to 67268 and add a vendor CAGE no. 66958. Editorial changes throughout.	6 NOV 87	R R Evans

CURRENT CAGE CODE 67268

REV STATUS OF PAGES																							
REV STATUS	REV	A	A	A		A	A	A	A	A									A	A	A	A	A
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Defense Electronics Supply Center Dayton, Ohio	PREPARED BY [illegible]	**MILITARY DRAWING** This drawing is available for use by all Departments and Agencies of the Department of Defense
Original date of drawing: 16 July 1986	CHECKED BY [illegible]	TITLE: MICROCIRCUIT, MONOLITHIC, N-CHANNEL, SILICON GATE, SERIAL COMMUNICATIONS CONTROLLER
	APPROVED BY [illegible]	
	SIZE A / CODE IDENT. NO. 14933	DWG NO. 5962-85518
AMSC N/A	REV A	PAGE 1 OF 22

5962-E604

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-85518	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit
01	Z8030A	6.0 MHz	Serial communications controller
02	Z8030	4.0 MHz	Serial communications controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2"), dual-in-line package
Y	C-5 (44-terminal, .650" x .650"), square chip carrier package

1.3 Absolute maximum ratings.

V_{CC} supply voltage range (referenced to ground)	-0.3 V dc to +7.0 V dc
Voltage on any pin (referenced to ground)	-0.3 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation:	
At -55°C	2.0 W
Lead temperature (soldering, 10 seconds)	+270°C
Maximum junction temperature (T_J):	
At T_C = +125°C	+161°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Q and Y	(See MIL-M-38510, appendix C)

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.2 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Frequency of operation:	
Device type 01	0.5 MHz to 6.0 MHz
Device type 02	0.5 MHz to 4.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C
Clock rise and fall times:	
Device type 01	15 ns maximum rise, 10 ns maximum fall
Device type 02	20 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Timing diagram. The timing diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
High input voltage	V_{IH}		1, 2, 3	ALL	2.2	V_{CC} +0.3 1/	V
Low input voltage	V_{IL}		1, 2, 3	ALL	-0.3 1/	+0.8	V
Low output voltage	V_{OL}	$I_{OL} = 2.0$ mA	1, 2, 3	ALL		+0.4 1/	V
High output voltage	V_{OH}	$I_{OH} = -250\ \mu A$	1, 2, 3	ALL	+2.4 1/		V
Power supply current	I_{CC}	Outputs open, $T_C = -55°C$ $V_{CC} = 5.5$ V	1, 2, 3	ALL		350	mA
Output leakage current low	I_{LOL}	$V_{IN} = 0.4$ V	1, 2, 3	ALL	-10	+10	µA
Output leakage current high	I_{LOH}	$V_{IN} = 2.4$ V	1, 2, 3	ALL	-10	+10	µA
Input low current	I_{IL}	$V_{IN} = 0.4$ V	1, 2, 3	ALL	-10	+10	µA
Input high current	I_{IH}	$V_{IN} = 2.4$ V	1, 2, 3	ALL	-10	+10	µA
Maximum frequency 1/	f_{MAX}		9, 10, 11	01	6.0		MHz
				02	4.0		MHz
Input capacitance	C_{IN}		4	ALL		10 1/	pF
Output capacitance	C_{OUT}		4	ALL		15 1/	pF
Bidirectional capacitance	$C_{I/O}$		4	ALL		20 1/	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$, $C_L = 50\ pF \pm 10\%$ unless otherwise specified	Group A subgroups	Reference	Device type 01 Min	01 Max	02 Min	02 Max	Unit
$\overline{AS}$ low width	TwAS	See figure 3	9, 10, 11	1	50		70		ns
$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay 1/	TdDS(AS)	unless otherwise specified	9, 10, 11	2	25		50		ns
$\overline{CS_0}$ to $\overline{AS}$ ↑ setup time 1/ 2/	TsCS0(AS)		9, 10, 11	3	0		0		ns
$\overline{CS_0}$ to $\overline{AS}$ ↑ hold time 2/	ThCS0(AS)		9, 10, 11	4	40		60		ns
CS_1 to $\overline{DS}$ ↓ setup time 2/	TsCS1(DS)		9, 10, 11	5	80		100 1/		ns
CS_1 to $\overline{DS}$ ↑ hold time 2/	ThCS1(DS)		9, 10, 11	6	40 1/		55		ns
$\overline{INTACK}$ to $\overline{AS}$ ↑ setup time 1/	TsIA(AS)		9, 10, 11	7	0		0		ns
$\overline{INTACK}$ to $\overline{AS}$ ↑ hold time 1/	ThIA(AS)		9, 10, 11	8	250		250		ns
R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ setup time	TsRWR(DS)		9, 10, 11	9	80		100		ns
R/$\overline{W}$ to $\overline{DS}$ ↑ hold time 1/	ThRW(DS)		9, 10, 11	10	40		55		ns
R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ setup time 1/	TsRWW(DS)		9, 10, 11	11	0		0		ns
$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay 1/	TdAS(DS)		9, 10, 11	12	50		85		ns
$\overline{DS}$ low width 1/	TwDS		9, 10, 11	13	250		390		ns
Valid access recovery time 1/ 3/	TrC		9, 10, 11	14	6TcPC +130		6TcPC +200		ns
Address to $\overline{AS}$ ↑ setup time 2/	TsA(AS)		9, 10, 11	15	10		30		ns
Address to $\overline{AS}$ ↑ hold time 2/	ThA(AS)		9, 10, 11	16	30		50		ns
Write data to $\overline{DS}$ ↓ setup time	TsDW(DS)		9, 10, 11	17	20		30		ns
Write data to $\overline{DS}$ ↑ hold time 1/	ThDW(DS)		9, 10, 11	18	20		30		ns
$\overline{DS}$ ↓ to data active delay 1/	TdDS(DA)		9, 10, 11	19	0		0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Reference	Device type 01 Min	Device type 01 Max	Device type 02 Min	Device type 02 Max	Unit
$\overline{DS}$ ↑ to read data not valid delay	TdDSr(DR)	See figure 3, C_L = 50 pF ±10% unless otherwise specified	9, 10, 11	20	0		1/ 0		ns
$\overline{DS}$ ↓ to read data valid delay 1/	TdDSf(DR)		9, 10, 11	21		180		250	ns
$\overline{AS}$ ↑ to read data valid delay 1/	TdAS(DR)		9, 10, 11	22		335		520	ns
$\overline{DS}$ ↑ to read data float delay 1/ 4/	TdDS(DRZ)		9, 10, 11	23		45		70	ns
Address required valid to read data valid delay	TdA(DR)		9, 10, 11	24		420		570 1/	ns
$\overline{DS}$ ↓ to wait valid delay 1/ 5/	TdDS(W)		9, 10, 11	25		200		240	ns
$\overline{DS}$ ↓ to $\overline{W/REQ}$ not valid delay 1/	TdDSf(REQ)		9, 10, 11	26		200		240	ns
$\overline{DS}$ ↑ to $\overline{DTR/REQ}$ not valid delay 1/	TdDSr(REQ)		9, 10, 11	27		5TcPC +500		5TcPC +300	ns
$\overline{AS}$ ↑ to $\overline{INT}$ valid delay 1/ 5/	TdAS(INT)		9, 10, 11	28		500		500	ns
$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (acknowledge) delay 1/ 6/	TdAS(DSA)		9, 10, 11	29	250		250		ns
$\overline{DS}$ (acknowledge) low width 1/	TwDSA		9, 10, 11	30	250		390		ns
$\overline{DS}$ ↓ (acknowledge) to read data valid delay 1/	TdDSA(DR)		9, 10, 11	31		180		250	ns
IEI to $\overline{DS}$ ↓ (acknowledge) setup time 1/	TsIEI(DSA)		9, 10, 11	32	100		120		ns
IEI to $\overline{DS}$ ↑ (acknowledge) hold time 1/	ThIEI(DSA)		9, 10, 11	33	0		0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Reference	Device type 01 Min	Device type 01 Max	Device type 02 Min	Device type 02 Max	Unit
IEI to IEO delay 1/	TdIEI(IEO)	See figure 3, C_L = 50 pF ±10% unless otherwise specified	9, 10, 11	34		100		120	ns
$\overline{AS}$ ↑ to IEO delay 1/ 7/	TdAS(IEO)		9, 10, 11	35		250		250	ns
$\overline{DS}$ ↓ (acknowledge) 1/ 5/ to $\overline{INT}$ inactive delay	TdDSA(INT)		9, 10, 11	36		500		500	ns
$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay 1/ for no reset	TdDS(ASQ)		9, 10, 11	37	15		30		ns
$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay 1/ 2/ for no reset	TdASQ(DS)		9, 10, 11	38	30		30		ns
$\overline{AS}$ and $\overline{DS}$ coincident low for reset 1/ 8/	TwRES		9, 10, 11	39	250		250		ns
PCLK low width	TwPCl		9, 10, 11	40	70	1000 1/	105 1/	2000 1/	ns
PCLK high width	TwPCh		9, 10, 11	41	70	1000 1/	105 1/	2000 1/	ns
PCLK cycle time	TcPC		9, 10, 11	42	165	2000 1/	250	4000 1/	ns
PCLK rise time 1/	TrPC		9, 10, 11	43		15		20	ns
PCLK fall time	TfPC		9, 10, 11	44		10		1/ 20	ns
PCLK ↓ to $\overline{W/REQ}$ valid 1/	TdPC(REQ)		9, 10, 11	1		250		250	ns
PCLK ↓ to wait 1/ inactive delay	TdPC(W)		9, 10, 11	2		350		350	ns
$\overline{RxC}$ ↑ to PCLK ↑ setup time 9/ 12/ (PCLK 4 case only)	TsRXC(PC)		9, 10, 11	3	70	TwPCL 1/	80	TwPCL 1/	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Reference	Device type 01 Min	Device type 01 Max	Device type 02 Min	Device type 02 Max	Unit
RxD to $\overline{RxC}$ ↑ 1/ 9/ setup time ($\overline{X1}$ mode)	TsRXD(RXCr)	See figure 3; C_L = 50 pF ±10% unless otherwise specified	9, 10, 11	4	0		0		ns
RxD to $\overline{RxC}$ ↑ hold time (X1 mode) 9/	ThRXD(RXCr)		9, 10, 11	5	150		1/ T50		ns
RxD to $\overline{RxC}$ ↓ 1/ 9/ 13/ setup time (X1 mode)	TsRXD(RXCf)		9, 10, 11	6	0		0		ns
RxD to $\overline{RxC}$ ↓ 9/ 13/ hold time (X1 mode)	ThRXD(RXCf)		9, 10, 11	7	150		1/ T50		ns
$\overline{SYNC}$ to $\overline{RxC}$ ↑ setup time 1/ 9/	TsSY(RXC)		9, 10, 11	8	-200		-200		ns
$\overline{SYNC}$ to $\overline{RxC}$ ↑ 1/ 9/ hold time	ThSY(RXC)		9, 10, 11	9	3TcPC +200		3TcPC +200		ns
$\overline{TxC}$ ↓ to PCLK ↑ 10/ 12/ setup time	TsTXC(PC)		9, 10, 11	10	0		0		ns
$\overline{TxC}$ ↓ to TxD delay 10/ (X1 mode)	TdTXCf(TXD)		9, 10, 11	11		230		300	ns
$\overline{TxC}$ ↑ to TxD delay 10/ 13/ (X1 mode)	TdTXCr(TXD)		9, 10, 11	12		230		300	ns
TxD to TRxC delay 1/ (send clock echo)	TdTXD(TRX)		9, 10, 11	13		200		200	ns
$\overline{RTxC}$ high width 1/ 14/	TwRTXh		9, 10, 11	14	180		180		ns
$\overline{RTxC}$ low width 1/ 14/	TwRTXl		9, 10, 11	15	180		180		ns
$\overline{RTxC}$ cycle time 1/ 14/	TcRTX		9, 10, 11	16	400		400		ns
Crystal oscillator period 1/ 11/	TcRTXX		9, 10, 11	17	250	1000	250	1000	ns
$\overline{TRxC}$ high width 1/ 14/	TwTRXh		9, 10, 11	18	180		180		ns
$\overline{TRxC}$ low width 1/ 14/	TwTRXl		9, 10, 11	19	180		180		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Reference	Device type 01 Min	Device type 01 Max	Device type 02 Min	Device type 02 Max	Unit
$\overline{TRxC}$ cycle time 1/ 14/	TcTRX	See figure 3, C_L = 50 pF ±10% unless otherwise specified	9, 10, 11	20	400		400		ns
$\overline{DCD}$ or $\overline{CTS}$ pulse width 1/	TwEXT		9, 10, 11	21	200		200		ns
$\overline{SYNC}$ pulse width 1/	TwSY		9, 10, 11	22	200		200		ns
$\overline{RxC}$ ↑ to $\overline{W/REQ}$ valid delay 1/ 16/ 18/	TdRXC(REQ)		9, 10, 11	1	8	12	8	12	ns
$\overline{RxC}$ ↑ to wait inactive delay 1/ 15/ 16/ 18/	TdRXC(W)		9, 10, 11	2	8	12	8	12	ns
$\overline{RxC}$ ↑ to $\overline{SYNC}$ valid delay 1/ 16/ 18/	TdRXC(SY)		9, 10, 11	3	4	7	4	7	ns
$\overline{RxC}$ ↑ $\overline{INT}$ valid delay 1/ 15/ 16/ 18/ 19/	TdRXC(INT)		9, 10, 11	4	8 +2	12 +3	8 +2	12 +3	ns
$\overline{TxC}$ ↓ to $\overline{W/REQ}$ valid delay 1/ 17/ 18/	TdTXC(REQ)		9, 10, 11	5	5	8	5	8	ns
$\overline{TxC}$ ↓ to wait inactive delay 1/ 15/ 17/ 18/	TdTXC(W)		9, 10, 11	6	5	8	5	8	ns
$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ valid delay 1/ 17/ 18/	TdTXC(DRQ)		9, 10, 11	7	4	7	4	7	ns
$\overline{TxC}$ ↓ to $\overline{INT}$ valid delay 2/ 1/15/17/18/19/	TdTXC(INT)		9, 10, 11	8	4 +2	6 +3	4 +2	6 +3	ns
$\overline{SYNC}$ transition to $\overline{INT}$ valid delay 1/15/19/	TdSY(INT)		9, 10, 11	9	2	3	2	3	ns
$\overline{DCD}$ or $\overline{CTS}$ transition to $\overline{INT}$ valid delay 1/ 15/ 19/	TdEXT(INT)		9, 10, 11	10	2	3	2	3	ns

See footnotes at end of table.

1/ If not tested, shall be guaranteed to the specified limits.

2/ Parameter does not apply to interrupt acknowledge transactions.

3/ Parameter applies only between transactions involving the SCC.

4/ Float delay is defined as the time required for a ±0.5 V change in the output with a maximum DC load and minimum AC load.

5/ Open-drain output, measured with open-drain test load.

6/ Parameter is system dependent. For any Z-SCC in the daisy chain TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain. TsIEI(DSA) for the Z-SCC and TdIEIf(IEO) for each device separating them in the daisy chain.

7/ Parameter applies only to a Z-SCC pulling $\overline{INT}$ low at the beginning of the interrupt acknowledge transactions.

8/ Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z-SCC.

9/ $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.

10/ $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

11/ Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30 pF capacitors to the ground connected to them.

12/ Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{RxC}$ and PCLK or $\overline{TxC}$ and PCLK is required.

13/ Parameter applies only to FM encoding/decoding.

14/ Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.

15/ Open-drain output, measured with open-drain test load.

16/ $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.

17/ $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

18/ Units equal to TcPC.

19/ Units equal to $\overline{AS}$.

Device types 01 and 02

Case Q

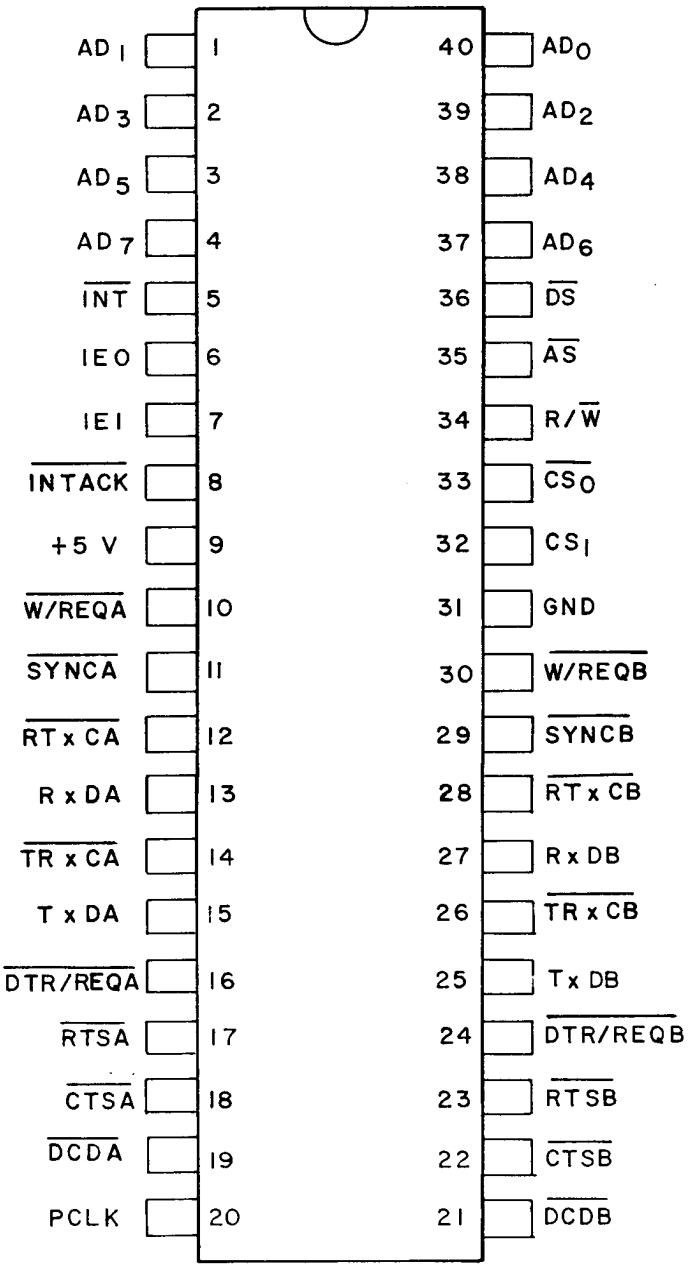


FIGURE 1. Terminal connections.

Device types 01 and 02

Case Y

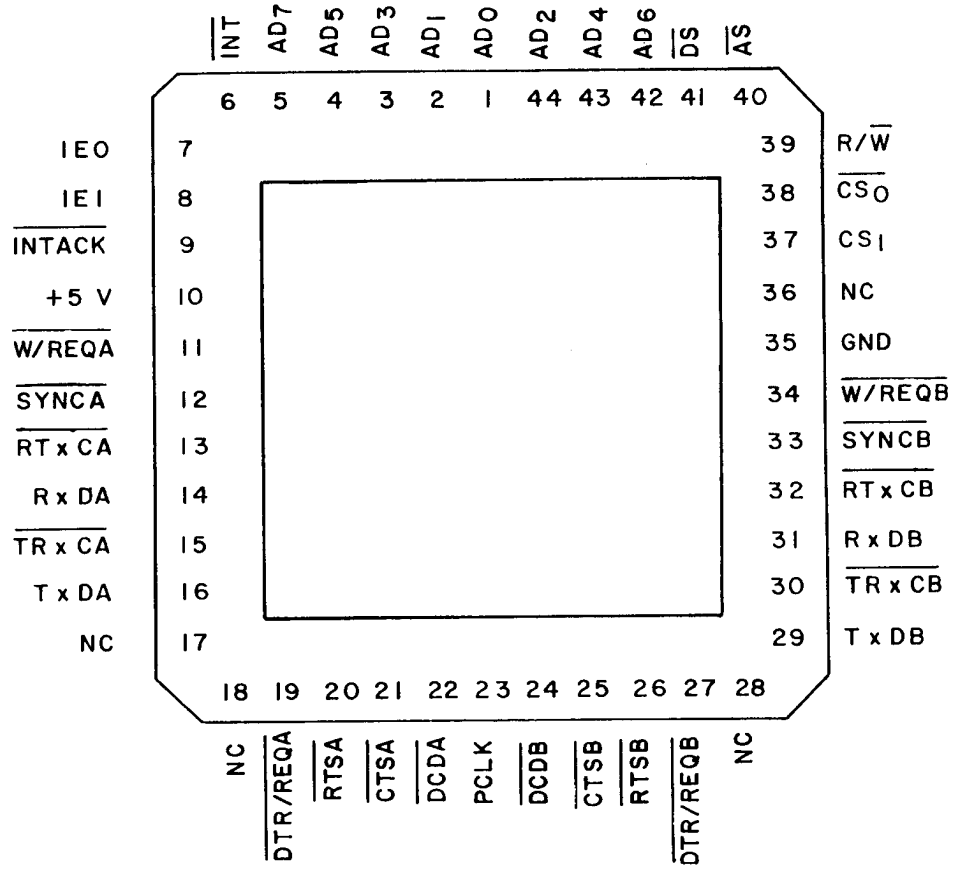
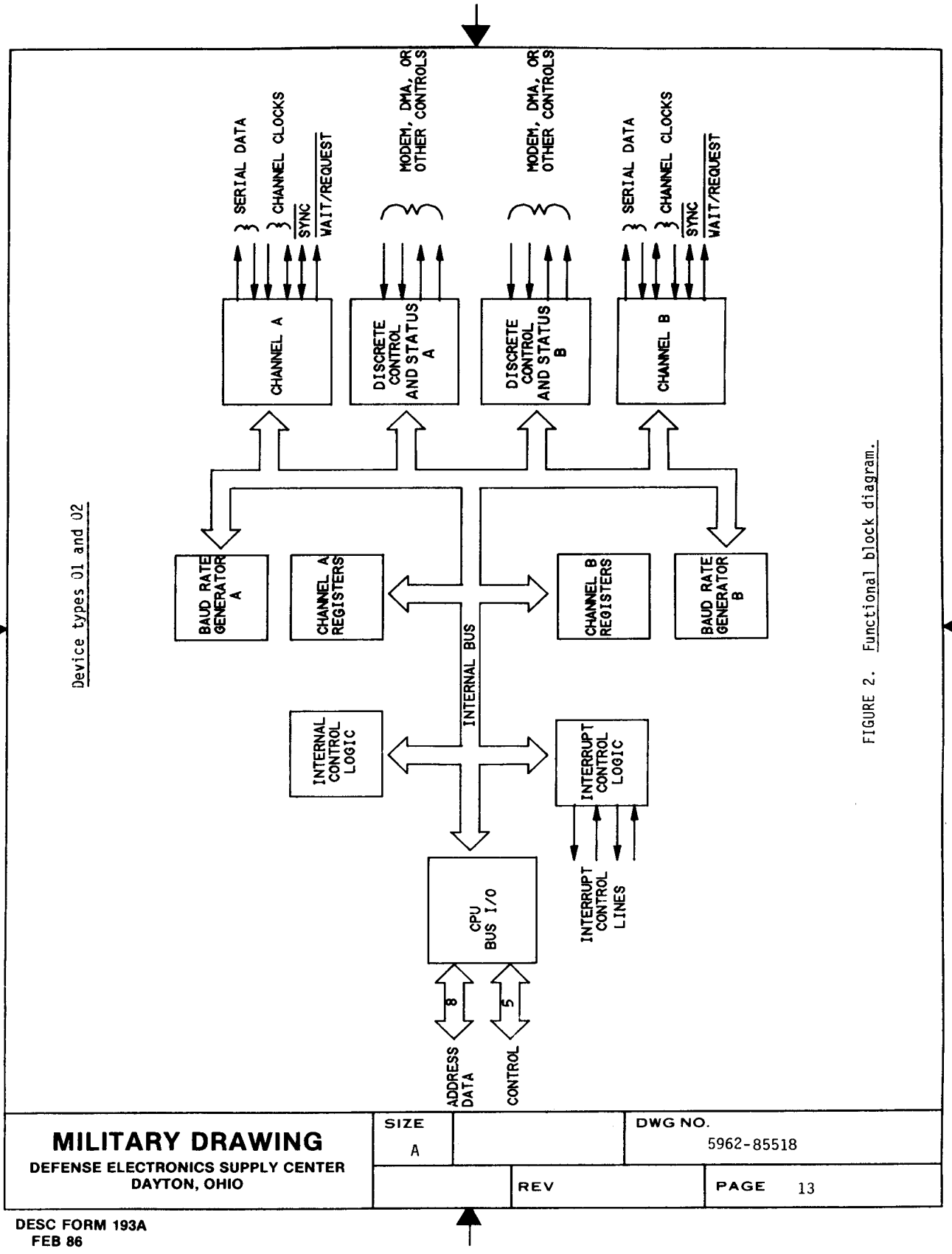


FIGURE 1. Terminal connections - Continued.



Device types 01 and 02

FIGURE 2. Functional block diagram.

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Device types 01 and 02

READ AND WRITE TIMING

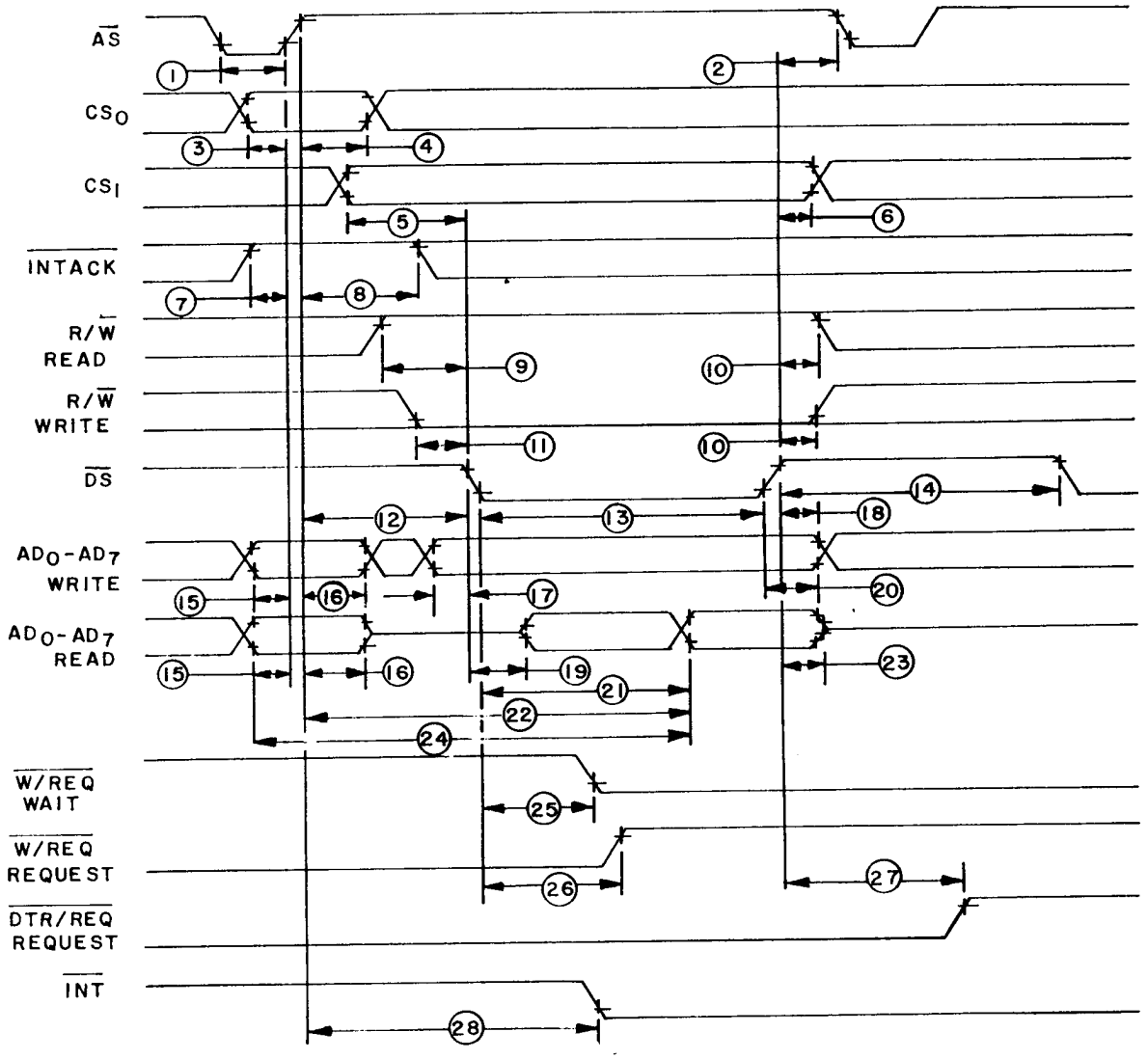

FIGURE 3. Timing diagram.

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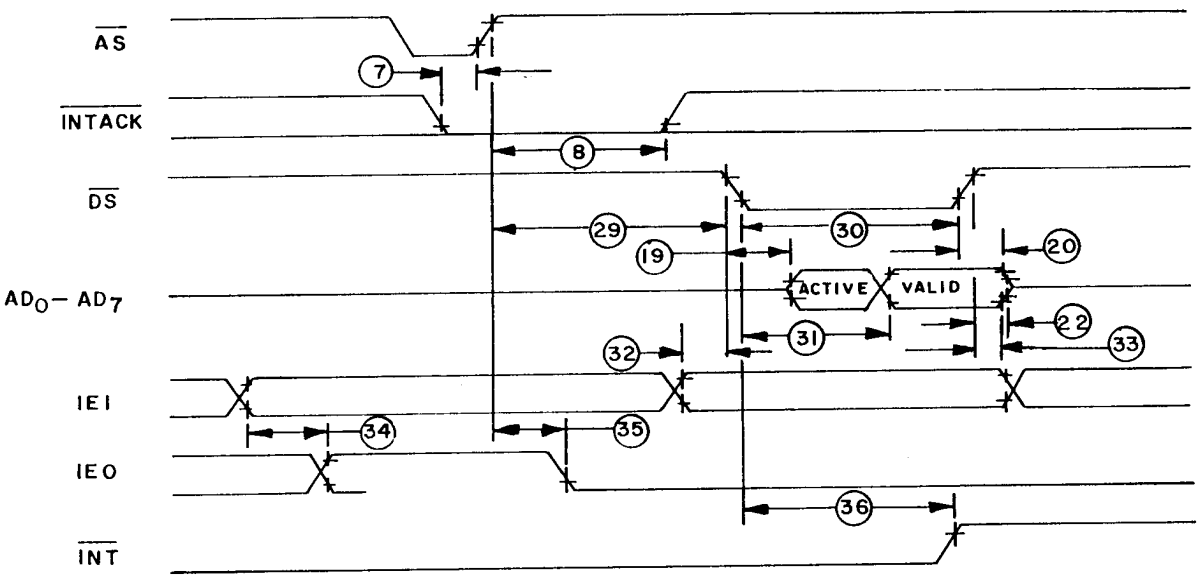
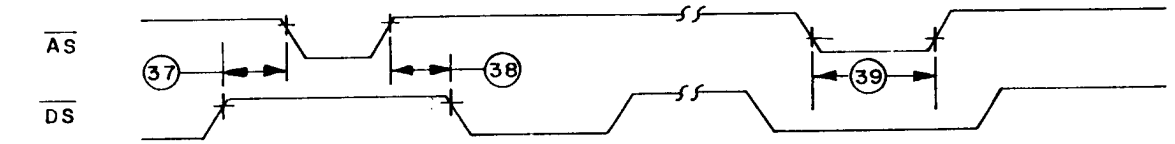
Device types 01 and 02

INTERRUPT ACKNOWLEDGE TIMING



RESET TIMING



CYCLE TIMING

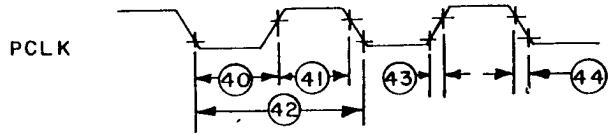


FIGURE 3. Timing diagram - Continued.

Device types 01 and 02

GENERAL TIMING

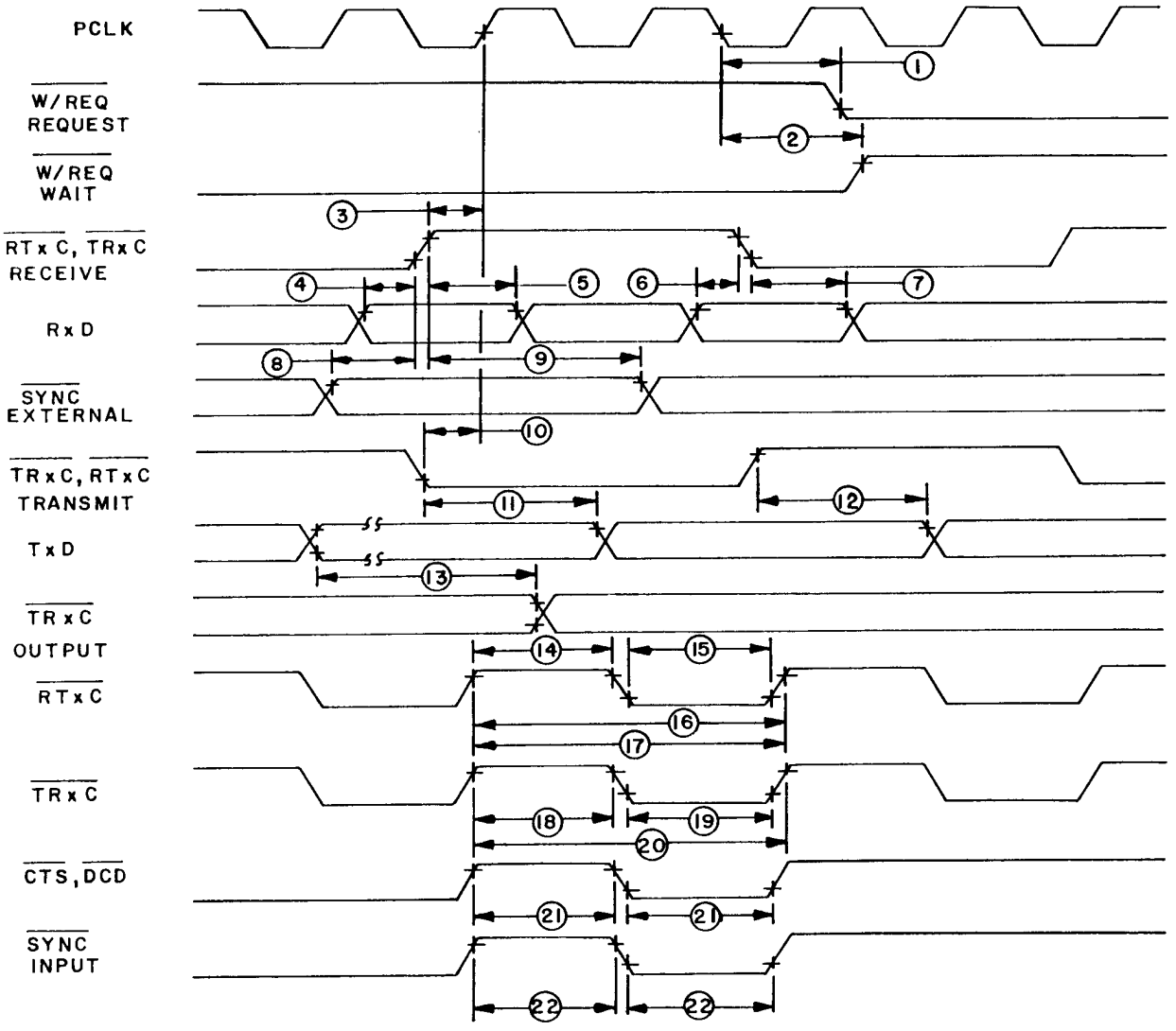


FIGURE 3. Timing diagram - Continued.

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Device types 01 and 02

SYSTEM TIMING

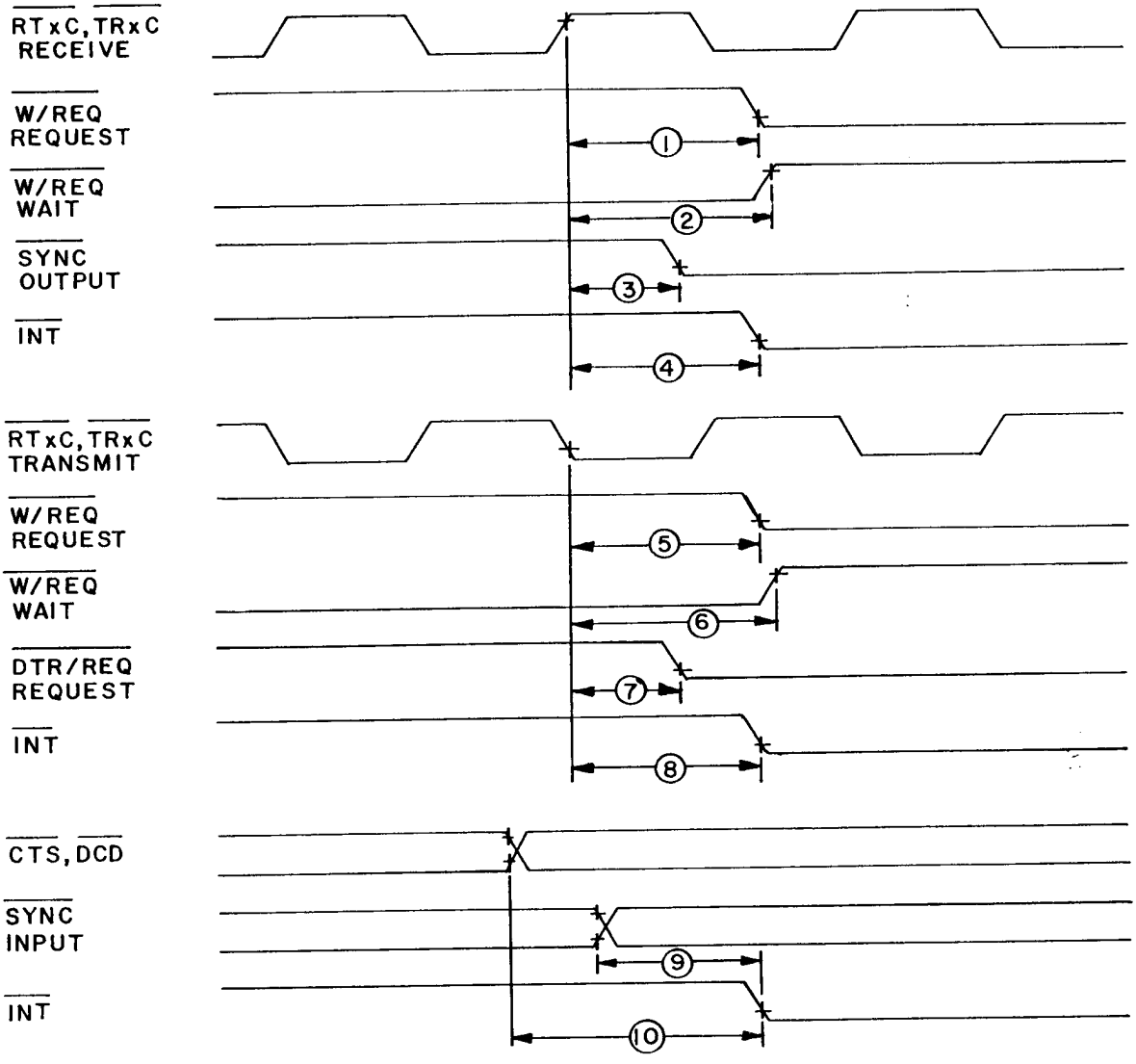

FIGURE 3. Timing diagram - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 tests shall include verification of the instruction set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional descriptions for these devices shall be as follows:

(The following section describes the pin functions of the Z-SCC. Figures 1 and 2 detail the respective pin functions and pin assignments.)

AD_0-AD_7. Address/data bus (bidirectional, active high, 3-state). These multiplexed lines carry register addresses to the Z-SCC as well as data or control information to and from the Z-SCC.

$\overline{AS}$. Address strobe (input, active low). Addresses on AD_0-AD_7 are latched by the rising edge of this signal.

$\overline{CS_0}$. Chip select 0 (input, active low). This signal is latched concurrently with the addresses on AD_0-AD_7 and must be active for the intended bus transaction to occur.

CS_1. Chip select 1 (input, active high). This second select signal must also be active before the intended bus transaction can occur. CS_1 must remain active throughout the transaction.

$\overline{CTSA}$, $\overline{CTSB}$. Clear to send (inputs, active low). If these pins are programmed as auto enables, a low on the inputs enables their respective transmitters. If not programmed as auto enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The device detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

$\overline{DCDA}$, $\overline{DCDB}$. Data carrier detect (inputs active low). These pins function as receiver enables if they are programmed for auto enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The Z-SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

$\overline{DS}$. Data strobe (input, active low). This signal provides timing for the transfer of data into and out of the Z-SCC. If $\overline{AS}$ and $\overline{DS}$ coincide, this is interpreted as a reset.

$\overline{DTR/REQA}$, $\overline{DTR/REQB}$. Data terminal ready/request (outputs, active low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as request lines for a DMA controller.

IEI. Interrupt enable in (input, active high). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. Interrupt enable out (output, active high). IEO is high only if IEI is high and the CPU is not servicing a Z-SCC interrupt or the Z-SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$. Interrupt request (output, open-drain, active low). This signal is activated when the Z-SCC requests an interrupt.

$\overline{INTACK}$. Interrupt acknowledge (input, active low). This signal indicates an active interrupt acknowldege cycle. During this cycle, the Z-SCC interrupt daisy chain settles. When $\overline{DS}$ becomes active, the Z-SCC places an interrupt vector on the data bus (if IEI is high). $\overline{INTACK}$ is latched by the rising edge of $\overline{AS}$.

PCLK. Clock (input). This is the master Z-SCC clock used to synchronize internal signals. PCLK is not required to have any phase relationship with the master system clock, although the frequency of this clock must be as least 90 percent of the CPU clock frequency for a Z8000. PCLK is a TTL level signal.

RxDA, RxDB. Receive data (inputs, active high). These input signals receive serial data at standard TTL levels.

6.4 Symbols, definitions, and functional descriptions - Continued.

$\overline{RTxCA}$, $\overline{RTxCB}$. Receive/transmit clock (inputs, active low). These pins can be programmed in several different modes of operation. In each channel, $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock of the digital phase-locked loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

$\overline{RTSA}$, $\overline{RTSB}$. Request to send (outputs, active low). When the request to send (RTS) bit in write register 5 is set, the $\overline{RTS}$ signal goes low. When the RTS bit is reset in the asynchronous mode and auto enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in asynchronous mode with auto enable off, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

R/$\overline{W}$. Read/write (input). This signal specifies whether the operation to be performed is a read or a write.

$\overline{SYNCA}$, $\overline{SYNCB}$. Synchronization (inputs or outputs, active low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit.

In the asynchronous receive mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the synchronous/hunt status bits in read register 0 but have no other function.

In external synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$.

In the internal synchronization mode (Monosync and bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.

TxDA, TxDB. Transmit data (outputs, active high). These output signals transmit serial data at standard TTL levels.

$\overline{TRxCA}$, $\overline{TRxCB}$. Transmit/receive clocks (inputs or outputs, active low). These pins can be programmed in several different modes of operation. $\overline{TRxC}$ may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

$\overline{W/REQA}$, $\overline{W/REQB}$. Wait/request (outputs, open-drain when programmed for a wait function, driven high or low when programmed for a request function). These dual-purpose outputs may be programmed as request lines for a DMA controller or as wait lines to synchronize the CPU to the Z-SCC data rate. The reset state is wait.

6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8551801QX	56708 66958	Z8030ACMB Z8030AD2/883
5962-8551801YX	56708 66958	Z8030ALMB Z8030AK2/883
5962-8551802QX	56708 66958	Z8030CMB Z8030D2/883
5962-8551802YX	56708 66958	Z8030LMB Z8030K2/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
56708	Zilog, Incorporated 1315 Dell Avenue Campbell, CA 95008
66958	SGS Semiconductor Corporation 1000 Bell Road Phoenix, AZ 85022