REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 04713 to case outline J(DIP PACKAGE). Editorial changes throughout.	1987 JUN 1	M. A. Frye
B	Add vendor CAGE 04713 for the "L" package. Changed drawing CAGE code to 67268. Deleted vendor CAGE 18714. Editorial changes throughout.	1990 NOV 26	M. A. Frye

CURRENT CAGE CODE 67268

REV																								
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REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B						
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Marcia B Kelleher

CHECKED BY: Thomas J. Riccuiti

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 15 JANUARY 1987

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, HIGH-SPEED CMOS, OCTAL THREE-STATE TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-86885

SHEET 1 OF 17

DESC FORM 193-1
SEP 87

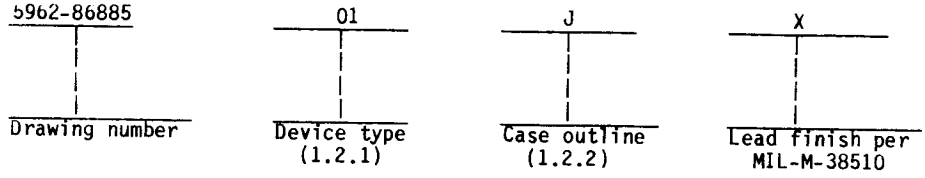
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1756

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC646	Octal noninverting three-state bus transceiver/register

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current	±20 mA
DC output current (per pin)	±35 mA
DC V_{CC} or GND current (per pin)	±70 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW 2/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}
Case operating temperature (T_C)	-55°C to +125°C
Input rise or fall time (t_r, t_f):	
V_{CC} = 2.0 V	0 to 1,000 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 6.0 V	0 to 400 ns
Minimum setup time (t_s):	
T_C = +25°C:	
V_{CC} = 2.0 V	100 ns
V_{CC} = 4.5 V	20 ns
V_{CC} = 6.0 V	17 ns
T_C = -55°C, +125°C:	
V_{CC} = 2.0 V	150 ns
V_{CC} = 4.5 V	30 ns
V_{CC} = 6.0 V	26 ns
Minimum hold time (t_h):	
T_C = -55°C, +125°C:	
V_{CC} = 2.0 V	55 ns
V_{CC} = 4.5 V	11 ns
V_{CC} = 6.0 V	9 ns
Minimum clock pulse width (t_w):	
T_C = +25°C:	
V_{CC} = 2.0 V	90 ns
V_{CC} = 4.5 V	18 ns
V_{CC} = 6.0 V	15 ns
T_C = -55°C, +125°C:	
V_{CC} = 2.0 V	135 ns
V_{CC} = 4.5 V	27 ns
V_{CC} = 6.0 V	23 ns
Maximum operating frequency (f_{MAX}):	
T_C = +25°C:	
V_{CC} = 2.0 V	5 MHz
V_{CC} = 4.5 V	27 MHz
V_{CC} = 6.0 V	31 MHz
T_C = -55°C, +125°C:	
V_{CC} = 2.0 V	3 MHz
V_{CC} = 4.5 V	18 MHz
V_{CC} = 6.0 V	20 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C < T_C < +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\|I_{OL}\| = 20\ \mu A$	$V_{CC} = 2.0$ V	1,2,3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\|I_{OL}\| = 6.0$ mA	$V_{CC} = 4.5$ V		3.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\|I_{OL}\| = 7.8$ mA	$V_{CC} = 6.0$ V		5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\|I_{OL}\| = 20\ \mu A$	$V_{CC} = 2.0$ V	1,2,3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\|I_{OL}\| = 6.0$ mA	$V_{CC} = 4.5$ V			0.4	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\|I_{OL}\| = 7.8$ mA	$V_{CC} = 6.0$ V			0.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
High level input voltage 2/	V_{IH}		V_{CC} = 2.0 V	1,2,3	1.5		V
			V_{CC} = 4.5 V		3.15		
			V_{CC} = 6.0 V		4.2		
Low level input voltage 2/	V_{IL}		V_{CC} = 2.0 V	1,2,3		0.3	V
			V_{CC} = 4.5 V			0.9	
			V_{CC} = 6.0 V			1.2	
Input capacitance	C_{IN}	V_{CC} = GND, T_C = +25°C, see 4.3.1c		4		10	pF
Quiescent current	I_{CC}	V_{CC} = 6.0 V, V_{IN} = V_{CC} or GND		1,2,3		160	µA
Input leakage current	I_{IN}	V_{CC} = 6.0 V, V_{IN} = V_{CC} or GND		1,2,3		±1	µA
Off-state output current	I_{OZ}	V_O = V_{CC} or GND, V_I = V_{IH}		1,2,3		±10	µA
Functional tests		See 4.3.1d		7,8			
Propagation delay, A or B input to A or B output 3/	t_{PHL1}, t_{PLH1}	C_L = 50 pF, T_C = +25°C, see figure 4	V_{CC} = 2.0 V	9		180	ns
			V_{CC} = 4.5 V			34	
			V_{CC} = 6.0 V			29	
		C_L = 50 pF, T_C = -55°C, +125°C, see figure 4	V_{CC} = 2.0 V	10,11		253	ns
			V_{CC} = 6.0 V			51	
			V_{CC} = 6.0 V			43	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay, clock B to A or clock A to B input to A or B output 3/	t_{PHL2}, t_{PLH2}	C_L = 50 pF, T_C = +25°C, see figure 4	V_{CC} = 2.0 V	9		220	ns
			V_{CC} = 4.5 V			44	
			V_{CC} = 6.0 V			38	
		C_L = 50 pF, T_C = -55°C, +125°C, see figure 4	V_{CC} = 2.0 V	10,11		330	ns
			V_{CC} = 4.5 V			66	
			V_{CC} = 6.0 V			57	
Propagation delay, source B to A or source A to B input to A or B output 3/	t_{PHL3}, t_{PLH3}	C_L = 50 pF, T_C = +25°C, see figure 4	V_{CC} = 2.0 V	9		290	ns
			V_{CC} = 4.5 V			58	
			V_{CC} = 6.0 V			50	
		C_L = 50 pF, T_C = -55°C, +125°C, see figure 4	V_{CC} = 2.0 V	10,11		435	ns
			V_{CC} = 4.5 V			87	
			V_{CC} = 6.0 V			75	
Propagation delay, output enable, $\overline{G}$ input or DIR to A or B output 3/	t_{PZH}, t_{PZL}	C_L = 50 pF, T_C = +25°C, see figure 4	V_{CC} = 2.0 V	9		175	ns
			V_{CC} = 4.5 V			35	
			V_{CC} = 6.0 V			30	
		C_L = 50 pF, T_C = -55°C, +125°C, see figure 4	V_{CC} = 2.0 V	10,11		265	ns
			V_{CC} = 4.5 V			53	
			V_{CC} = 6.0 V			45	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C < T_C < +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay, output disable, $\overline{G}$ input to A or B output 3/	t_{PHZ}, t_{PLZ}	C_L = 50 pF, T_C = +25°C, see figure 4	V_{CC} = 2.0 V	9		175	ns
			V_{CC} = 4.5 V			35	
			V_{CC} = 6.0 V			30	
		C_L = 50 pF, T_C = -55°C, +125°C, see figure 4	V_{CC} = 2.0 V	10,11		265	ns
			V_{CC} = 4.5 V			53	
			V_{CC} = 6.0 V			45	
Transition time, high to low, low to high 4/	t_{THL}, t_{TLH}	C_L = 50 pF, T_C = +25°C, see figure 4	V_{CC} = 2.0 V	9		60	ns
			V_{CC} = 4.5 V			12	
			V_{CC} = 6.0 V			10	
		C_L = 50 pF, T_C = -55°C, +125°C, see figure 4	V_{CC} = 2.0 V	10,11		90	ns
			V_{CC} = 4.5 V			18	
			V_{CC} = 6.0 V			15	
Three-state output capacitance 5/	C_{OUT}	Output enable = V_{CC} = 6.0 V, see 4.3.1c		4		20	pF

1/ For a power supply of 5.0 V ±10 percent the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case V_{IN} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 80 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

2/ V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} or V_{OL} tests.

3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified limits in table I.

4/ Transition times (t_{THL} and t_{TLH}), if not tested, shall be guaranteed to the specified limits in table I.

5/ Set the output enable control pins to V_{CC} or GND, as applicable, to disable the outputs of the device.

Device type	01	
Case outlines	J and L	3
Terminal number	Terminal symbol	
1	CAB	NC
2	SAB	CAB
3	DIR	SAB
4	A1	DIR
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	A8	A6
12	GND	A7
13	B8	A8
14	B7	GND
15	B6	NC
16	B5	B8
17	B4	B7
18	B3	B6
19	B2	B5
20	B1	B4
21	$\overline{G}$	B3
22	SBA	NC
23	CBA	B2
24	V_{CC}	B1
25	---	$\overline{G}$
26	---	SBA
27	---	CBA
28	---	V_{CC}

FIGURE 1. Terminal connections.

Device type 01

Inputs						Data I/O †		Operation
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 through A8	B1 through B8	
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H			Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X			Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled (data at the bus pins will be stored on every low to high transition on the clock inputs).

FIGURE 2. Truth table.

Device type 01

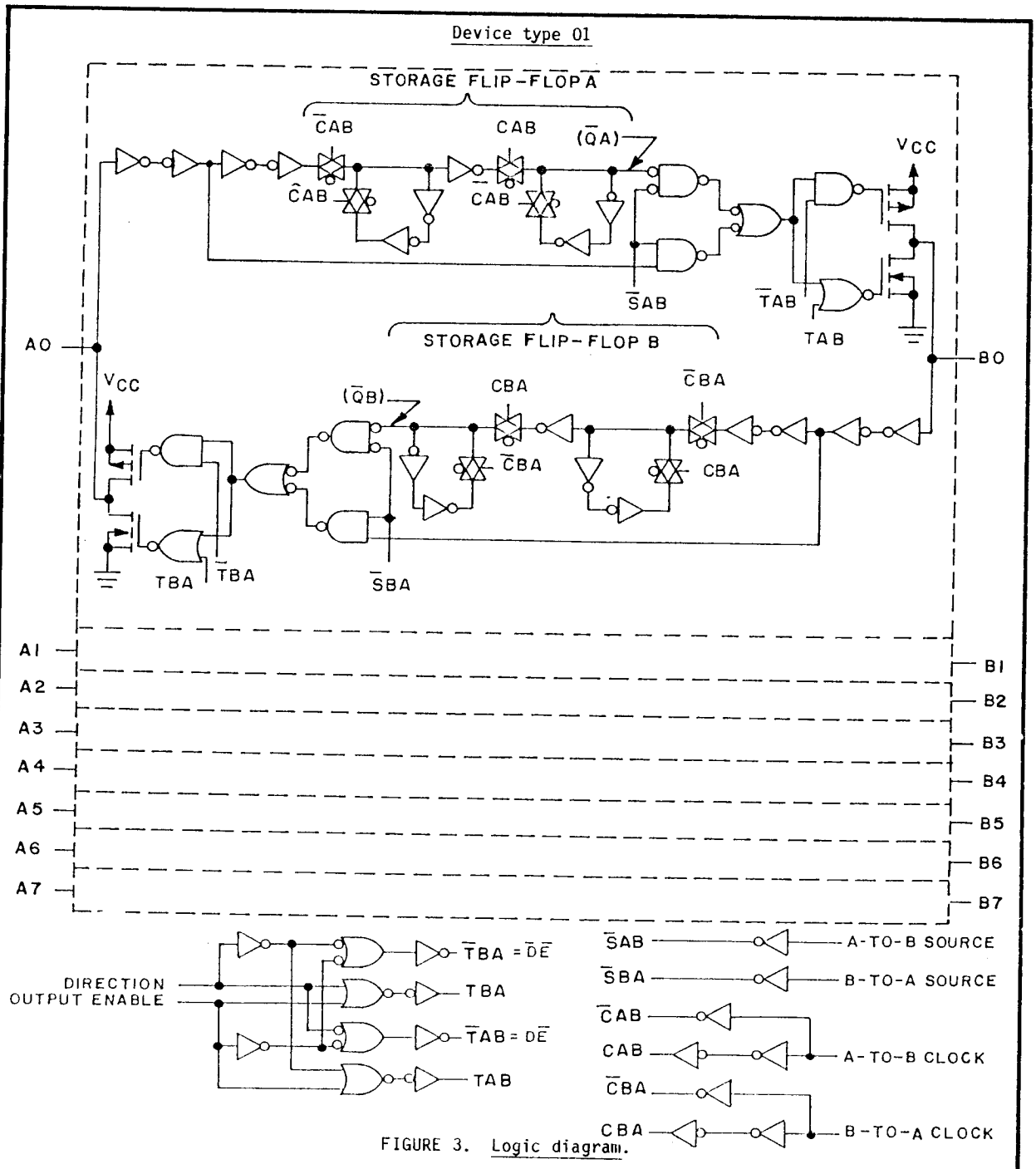


FIGURE 3. Logic diagram.

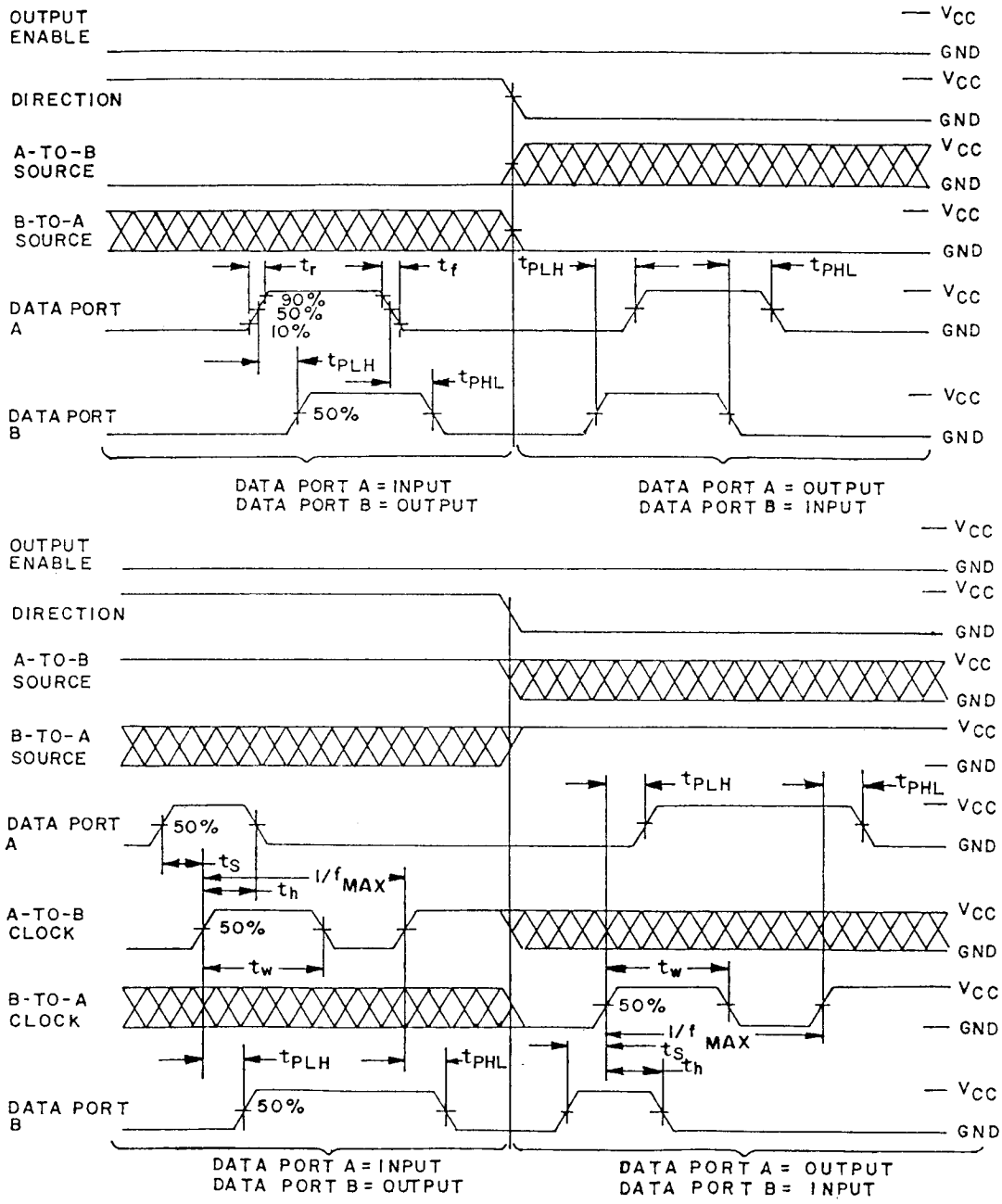
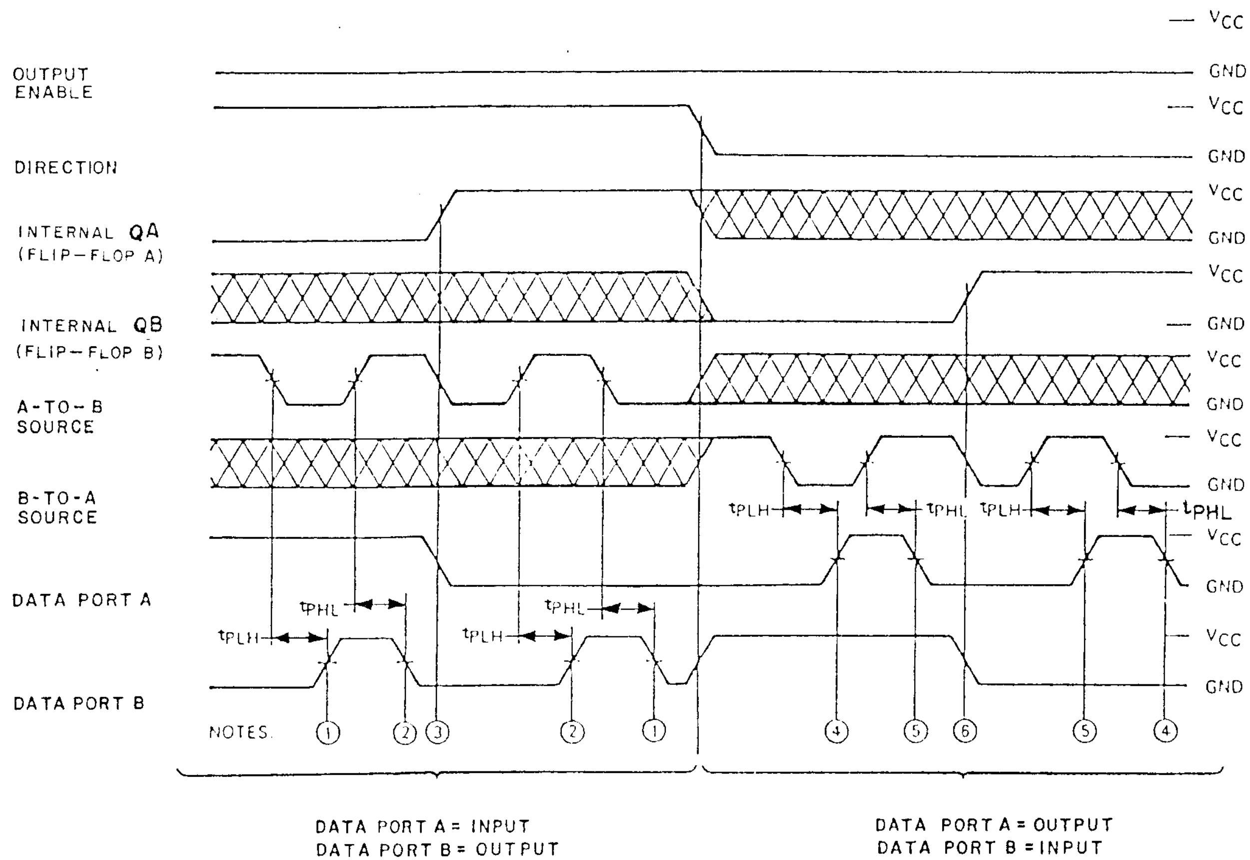
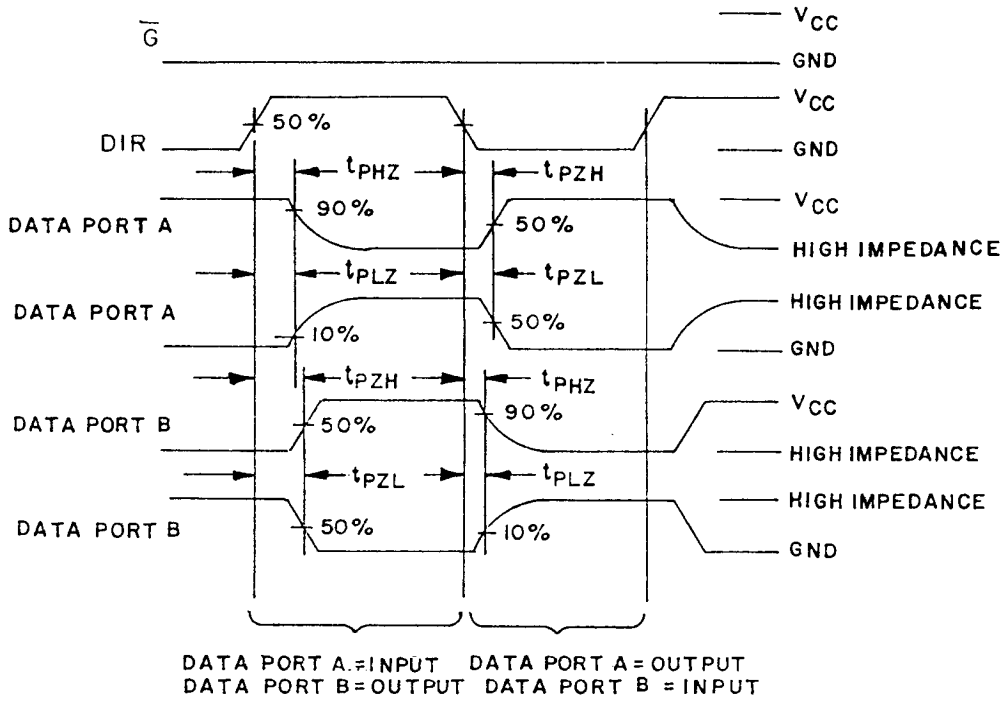


FIGURE 4. Switching time waveforms.



NOTES:
1. Output B changes from the level of the storage flip-flop, QA, to the level of input A.
2. Output B changes from the level of input A to the level of the storage flip-flop QA.
3. The A storage flip-flop, A-to-B source, and input A have simultaneously changed state for the purpose of this example. Output B is now displaying the voltage level of input A.
4. Output A changes from the level of the storage flip-flop, QB, to the level of input B.
5. Output A changes from the level of input B to the level of the storage flip-flop, QB.
6. The B storage flip-flop, B-to-A source, and input B have simultaneously changed state for the purpose of this example. Output A is now displaying the voltage level of input B.

FIGURE 4. Switching time waveforms - Continued.



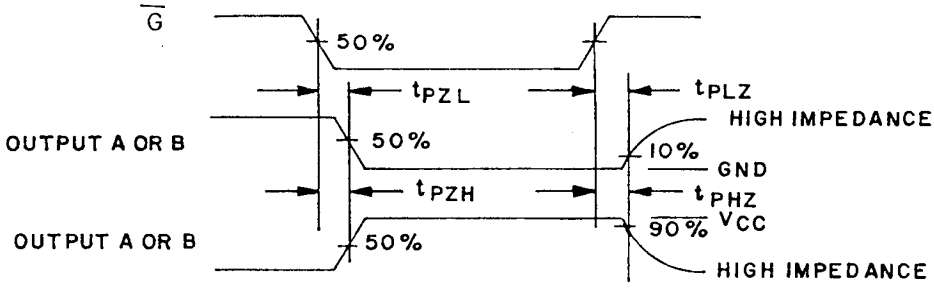


FIGURE 4. Switching time waveforms - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8,9,10**,11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. The coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone 513-296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 26 NOV 1990

Approved sources of supply for SMD 5962-86885 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification PIN
5962-8688501JX	04713	54HC646/BJAJC	M38510/65508BJX
5962-8688501LX	27014 04713	MM54HC646J/883 54HC646/BLAJC	M38510/65508BLX
5962-86885013X	27014	MM54HC646E/883	M38510/65508B3X

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
04713	Motorola, Incorporated 7402 South Price Road Tempe, AZ 85283
27014	National Semiconductor 2900 Semiconductor Dr. P.O. Box 58090 Santa Clara, CA 95052-8090 Point of contact: 333 Western Avenue South Portland, ME 04106

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.