REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
94-09-07

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-94641
A	67268	

SHEET 1 OF 22

DESC FORM 193
JUL 94

5962-E253-94

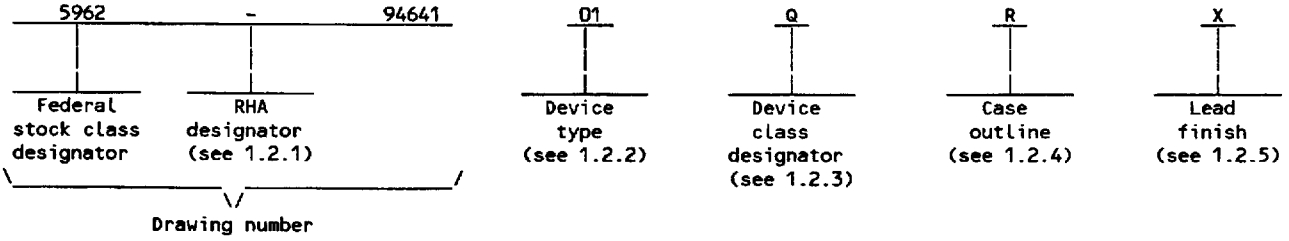
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0008879 638

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	145146-2	4-bit data bus input phase locked loop frequency sythesizer

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-0.5 V dc to +10.0 V dc
Input or output voltage, dc or transient (V_{IN}, V_{OUT})	-0.5 V dc to V_{DD} +0.5 V dc
Input or output current, dc or transient (I_{IN}, I_{OUT})	±10 mA
Supply current (I_{DD}, I_{SS})	±30 mA
Power dissipation (P_D)	500 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 8 seconds)	+260°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA})	+50°C/W

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{DD})	3.0 V dc to 9.0 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values referenced to V_{SS}

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Power supply voltage range	V_{DD}		---	1,2,3	3	9	V
Dynamic supply 4/ 5/ current	I_{SS}	$f_{IN} = OSC_{IN} = 10$ MHz, 1 V_{PP} ac coupled sine wave R = 128, A = 32, N = 128	3.0	4,5		-3	mA
				6		-3.7	
			5.0	4,5		-8	
				6		-10	
			9.0	4,5		-24	
				6		-30	
Quiescent supply 5/ current (not including pull-up current component)	I_{SS}	$V_{IN} = (f_{IN}/OSC_{IN}) = V_{DD}$ or V_{SS}, $I_{OUT} = 0$ µA R = 128, A = 32, N = 128, R, N counter = location 0, ϕR, ϕV and LD = high	3.0	1,3		-800	µA
				2		-1600	
			5.0	1,3		-1200	
				2		-2400	
			9.0	1,3		-1600	
				2		-3200	
Input voltage 4/ 5/ (f_{IN}, OSC_{IN})	V_{IN}	Input ac coupled sine wave	---	4,5,6	500		mV_{PP}
Low level input 5/ 6/ voltage (f_{IN}, OSC_{IN})	V_{IL}	$V_{OUT} \ge 2.1$ V	3.0	4,5,6		0	V
		$V_{OUT} \ge 3.5$ V	5.0			0	
		$V_{OUT} \ge 6.3$ V	9.0			0.25	
High level input 5/ 6/ voltage (f_{IN}, OSC_{IN})	V_{IH}	$V_{OUT} \le 0.9$ V	3.0	4,5,6	3.0		V
		$V_{OUT} \le 1.5$ V	5.0		5.0		
		$V_{OUT} \le 2.7$ V	9.0		8.75		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Low level input voltage 5/ (all other inputs)	V_{IL}	$V_{OUT} \le 0.5$ V or $V_{OUT} \ge V_{DD} - 0.5$ V	3.0	4,5,6		0.9	V
			5.0			1.5	
			9.0			2.7	
High level input 5/ voltage (all other inputs)	V_{IH}	$V_{OUT} \le 0.5$ V or $V_{OUT} \ge V_{DD} - 0.5$ V	3.0	4,5,6	2.1		V
			5.0		3.5		
			9.0		6.3		
Input leakage current 5/ (all inputs except f_{IN}, OSC_{IN})	I_{IH}	$V_{IN} = V_{DD}$	9.0	1		0.1	µA
				2		1.0	
				3		0.3	
Input current 5/ (f_{IN}, OSC_{IN})	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS}	9.0	1	±1	±25	µA
				2	±1	±22	
				3	±1	±50	
Input leakage current 5/ (all inputs except f_{IN}, OSC_{IN})	I_{IL}	$V_{IN} = V_{SS}$	9.0	1		-0.1	µA
				2		-1.0	
				3		-0.3	
Low level output 5/ voltage, OSC_{OUT}	V_{OL}	$I_{OUT} = 0$ µA, $V_{IN} = V_{DD}$	3.0	1,2,3		0.9	V
			5.0			1.5	
			9.0			2.7	
High level output 5/ voltage, OSC_{OUT}	V_{OH}	$I_{OUT} = 0$ µA, $V_{IN} = V_{SS}$	3.0	1,2,3	2.1		V
			5.0		3.5		
			9.0		6.3		
Low level output 5/ voltage, all other outputs	V_{OL}	$I_{OUT} = 0$ µA, $V_{IN} = 0$ V or V_{DD}	3.0	1,2,3		0.05	V
			5.0			0.05	
			9.0			0.05	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
High level output 5/ voltage, all other outputs	V_{OH}	I_{OUT} = 0 µA	3.0	1,2,3	2.95		V
			5.0		4.95		
			9.0		8.95		
Low level sinking current, modulus control	I_{OL}	V_{OUT} = 0.3 V	3.0	1	1.10		mA
				2	0.66		
				3	1.30		
Low level sinking current, modulus control	I_{OL}	V_{OUT} = 0.4 V	5.0	1	1.70		mA
				2	1.08		
				3	1.90		
		V_{OUT} = 0.5 V	9.0	1	3.30		
				2	2.10		
				3	3.80		
High level sourcing current, modulus control	I_{OH}	V_{OUT} = 2.7 V	3.0	1	-0.50		mA
				2	-0.30		
				3	-0.60		
		V_{OUT} = 4.6 V	5.0	1	-0.75		
				2	-0.50		
				3	-0.90		
		V_{OUT} = 8.5 V	9.0	1	-1.25		
				2	-0.80		
				3	-1.50		
Low level sinking current, lock detect	I_{OL}	V_{OUT} = 0.3 V	3.0	1	0.20		mA
				2	0.15		
				3	0.25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Low level sinking current, lock detect	I_{OL}	V_{OUT} = 0.4 V	5.0	1	0.51		mA
				2	0.36		
				3	0.64		
		V_{OUT} = 0.5 V	9.0	1	1.00		
				2	0.70		
				3	1.30		
High level sourcing current, lock detect	I_{OH}	V_{OUT} = 2.7 V	3.0	1	-0.20		mA
				2	-0.15		
				3	-0.25		
		V_{OUT} = 4.6 V	5.0	1	-0.51		
				2	-0.36		
				3	-0.64		
		V_{OUT} = 8.5 V	9.0	1	-1.00		
				2	-0.70		
				3	-1.30		
Low level sinking current, other outputs	I_{OL}	V_{OUT} = 0.3 V	3.0	1	0.20		mA
				2	0.15		
				3	0.25		
		V_{OUT} = 0.4 V	5.0	1	0.51		
				2	0.36		
				3	0.64		
		V_{OUT} = 0.5 V	9.0	1	1.00		
				2	0.70		
				3	1.30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/		Unit
					Min	Max	
High level sourcing current, other outputs	I_{OH}	V_{OUT} = 2.7 V	3.0	1	-0.20		mA
				2	-0.15		
				3	-0.25		
		V_{OUT} = 4.6 V	5.0	1	-0.51		
				2	-0.36		
				3	-0.64		
		V_{OUT} = 8.5 V	9.0	1	-1.00		
				2	-0.70		
				3	-1.30		
Output leakage current, PD_{OUT}	I_{OZ}	$V_{OUT} = V_{DD}$ or V_{SS}, output in off state	9.0	1	-0.1	+0.1	µA
				2	-1.0	+1.0	
				3	-0.3	+0.3	
Input capacitance	C_{IN}	5/ 7/	---	4,5,6		15	pF
Output capacitance	C_{OUT}	3-state 5/ 7/	9.0	4,5,6		15	pF
Input frequency 4/ 5/ (f_{IN}, OSC_{IN})	f_{IN}	R ≥ 8, A ≥ 0, N ≥ 8, V_{IN} = 500 mV_{PP} ac coupled square wave, see figure 3	3.0	4,5,6		6	MHz
			5.0	4,6		15	
				5		13	
			9.0	4,6		15	
				5		13	
		R ≥ 8, A ≥ 0, N ≥ 8, V_{IN} = 1 V_{PP} ac coupled square wave, see figure 3	3.0	4,6		12	
				5		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/ Min	Limits 3/ Max	Unit
Input frequency 4/ 5/ (f_{IN}, OSC_{IN})	f_{IN}	R ≥ 8, A ≥ 0, N ≥ 8, V_{IN} = 1 V_{PP} ac coupled square wave, see figure 3	5.0	4		20	MHz
				5		15	
				6		22	
			9.0	4		21	
				5		20	
				6		22	
		R ≥ 8, A ≥ 0, N ≥ 8, V_{IN} = V_{DD} to V_{SS} dc coupled square wave, see figure 3	3.0	4		12	
				5		8	
				6		13	
			5.0	4,5		22	
				6		25	
			9.0	4,5,6		25	
Propagation delay, f_{IN} to modulus control	t_{PLH}, t_{PHL}	See figure 4 5/	3.0	9		110	ns
				10,11		120	
			5.0	9		60	
				10,11		70	
			9.0	9		35	
				10,11		45	
Output pulse width, ϕ_R, ϕ_V, and LD with f_R in phase with f_V	$t_{W\phi}$	See figure 4 5/	3.0	9	25	200	ns
				10,11	20	260	
			5.0	9	20	100	
				10,11	15	125	
			9.0	9	10	70	
				10,11	5	80	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Output transition time, modulus control	t_{TLH}	See figure 4 5/	3.0	9,10,11		115	ns
			5.0	9		60	
				10,11		75	
			9.0	9		40	
				10,11		60	
Output transition time, modulus control	t_{THL}	See figure 4 5/	3.0	9		60	ns
				10,11		70	
			5.0	9		34	
				10,11		45	
			9.0	9		30	
				10,11		38	
Maximum output transition time, lock detect	$t_{TLH'}$ t_{THL}	See figure 4 5/	3.0	9		180	ns
				10,11		220	
			5.0	9		90	
				10,11		130	
			9.0	9		70	
				10,11		100	
Maximum output transition time, other outputs	$t_{TLH'}$ t_{THL}	See figure 4 5/	3.0	9		160	ns
				10,11		175	
			5.0	9		80	
				10,11		100	
			9.0	9		60	
				10,11		65	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{DD}	Group A subgroups	Limits 3/		Unit
					Min	Max	
Setup time, data to ST	t_{SU}	See figure 4 5/	3.0	9,10,11	10		ns
			5.0		10		
			9.0		10		
Hold time, address to ST	t_H	See figure 4 5/	3.0	9,10,11	25		ns
			5.0		20		
			9.0		15		
Setup time, address to ST	t_{SU}	See figure 4 5/	3.0	9,10,11	40		ns
			5.0		30		
			9.0		25		
Hold time, data to strobe	t_H	See figure 4 5/	3.0	9,10,11	25		ns
			5.0		20		
			9.0		15		
Input pulse width, ST	$t_W(H)$	See figure 3 5/	3.0	9,10,11	40		ns
			5.0		35		
			9.0		25		

1/ All 9.0 V test are performed at V_{DD} = 6.75 V and V_{SS} = -2.25 V (except I_{IL} (pull down): V_{DD} = 7.0 V, V_{SS} - 2.0 V) in lieu of V_{DD} = 9.0 V, V_{SS} = 0 V because test equipment limitations.

2/ All 9.0 V tests requiring a square wave input which are specified with the amplitude of V_{SS} to V_{DD}, are tested with a 8.5 V peak to peak square wave equal to V_{SS} + 0.25 V and V_{DD} - 0.25 V because of test equipment limitations.

3/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be as defined as conventional current flow out of a device terminal.

4/ Test requiring a sine wave input are tested using square wave of the specified amplitude and frequency due to test equipment limitations.

5/ Oscillator output C_L = 20 pF.

6/ Input dc-coupled square wave.

7/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device type	01
Case outline	R
Terminal number	Terminal symbol
1	D1
2	DO
3	f_{IN}
4	V_{SS}
5	PD_{OUT}
6	V_{DD}
7	OSC_{IN}
8	OSC_{OUT}
9	AO
10	A1
11	A2
12	ST
13	LD
14	MODULUS CONTROL
15	f_V
16	ϕV
17	ϕR
18	f_R
19	D3
20	D2

FIGURE 1. Terminal connections.

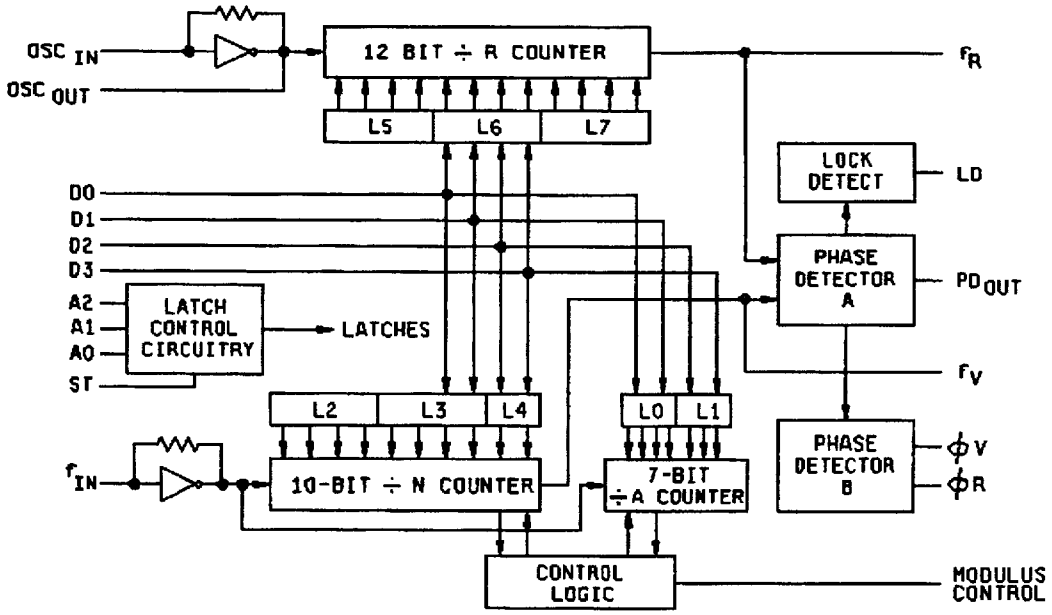


FIGURE 2. Block diagram.

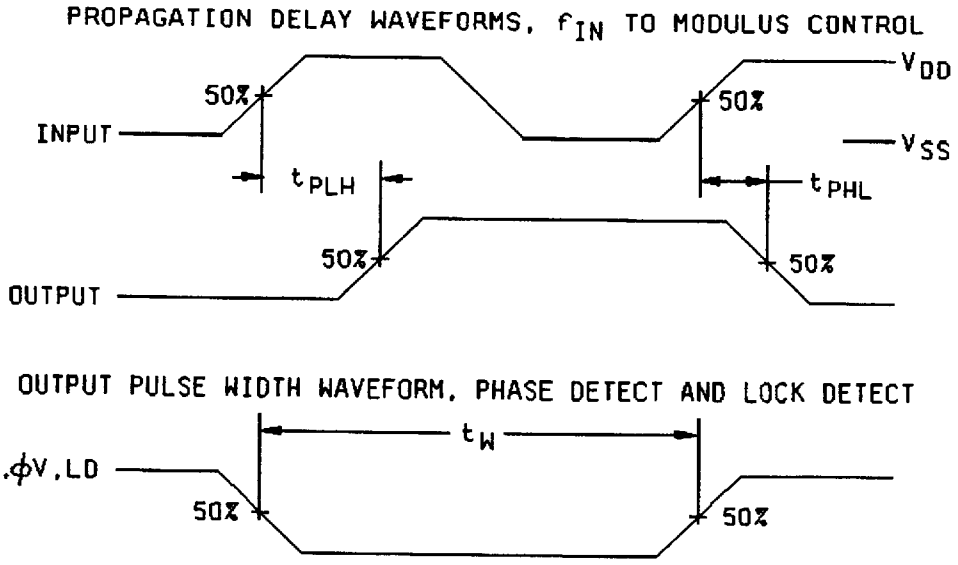


FIGURE 3. Switching waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-94641
		REVISION LEVEL	SHEET 15

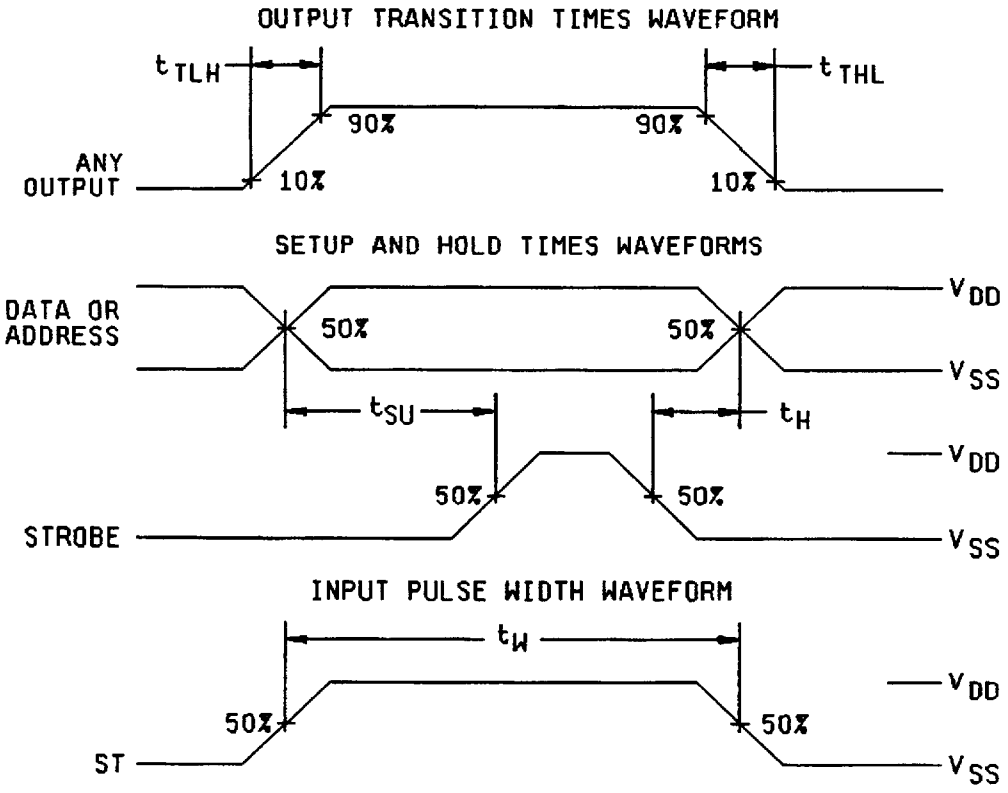
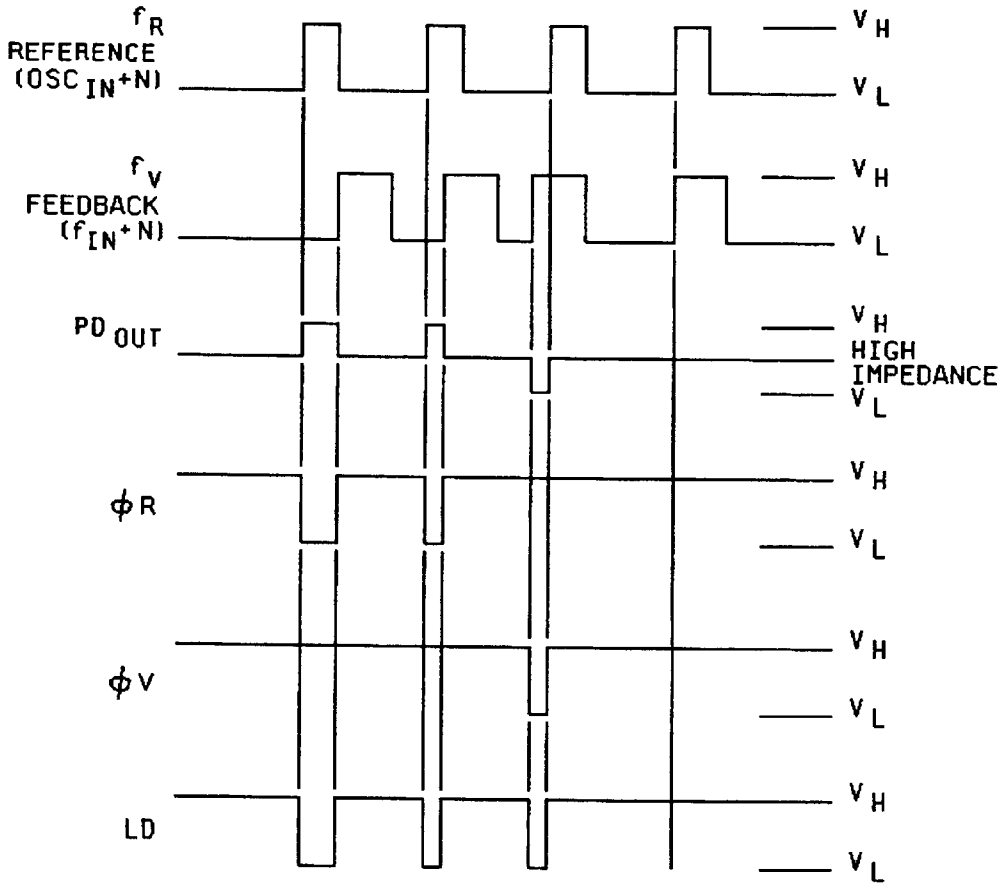


FIGURE 3. Switching waveforms - Continued.

Phase/frequency detectors and lock detector.



NOTES:

V_H = high voltage level and V_L = low voltage level.

At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.

The PD_{OUT} generates error pulses during out of lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the pass filter capacitor.

FIGURE 4. Output waveforms.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,9	1,4,9	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5, 1/ 6,9,10,11	1,2,3,4,5, 1/ 6,9,10,11	1,2,3,4,5, 1/ 6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5, 6,9,10,11	1,2,3,4,5, 6,9,10,11	1,2,3,4,5, 6,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions.

DATA INPUTS (D0 - D3)	Information at these inputs is transferred to the internal latches when the ST input is in the high state. D3 is the most significant.
(f_{IN})	Input frequency. Input to ÷N portion of synthesizer. f_{IN} is typically derived from loop VCO and is AC coupled. For larger amplitude signals (standard CMOS-logic levels), DC coupling may be used.
V_{SS}	Circuit ground.
(PD_{OUT})	Phase detector output. Three-state output of phase detector for use as loop error signal. Frequency $f_V > f_R$ or f_V leading: Negative pulses. Frequency $f_V < f_R$ or f_V lagging: Positive pulses. Frequency $f_V = f_R$ and phase coincidence: High impedance state.
V_{DD}	Positive power supply.
(OSC_{IN}, OSC_{OUT})	Oscillator input, Oscillator output. These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{IN} to ground and OSC_{OUT} to ground. OSC_{IN} may also serve as an input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{IN} , but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{OUT}.

A0 - A2

Address inputs A0, A1, and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	SELECTED	FUNCTION	D0	D1	D2	D3
0	0	0	Latch 0	÷A Bits	0	1	2	3
0	0	1	Latch 1	÷A Bits	4	5	6	-
0	1	0	Latch 2	÷N Bits	0	1	2	3
0	1	1	Latch 3	÷N Bits	4	5	6	7
1	0	0	Latch 4	÷N Bits	8	9	-	-
1	0	1	Latch 5	Reference Bits	0	1	2	3
1	1	0	Latch 6	Reference Bits	4	5	6	7
1	1	1	Latch 7	Reference Bits	8	9	10	11

ST

When high, this input will enter the data that appears at the D0, D1, D2, and D3 inputs, and when low will latch that information. When high, any changes in the data information will be transferred into the latches.

LD

Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

MODULUS CONTROL

Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷A counter has counted the rest of the way down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down its programmed value (N-A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (NT) = N-P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷N counter and A the number programmed into the ÷A counter.

f_V

This is the output of the ÷N counter that is internally connected to the phase detector input. With this output available, the ÷N counter can be used independently.

ϕV, ϕR

These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{OUT}). If frequency f_V is greater than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high. If the frequency of $f_V = f_R$ are both in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

f_R

This is the output of the ÷R counter that is internally connected to the phase detector input. With this output available, the ÷R counter can be used independently.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.