DATA SHEET

74ABT4764
Programmable DRAM Controller

Product Specification

IC23

March 22, 1994

PHILIPS

Programmable DRAM Controller

74ABT4764

FEATURES

- 80MHz programmable sequencer
- Four active pages with hit/miss detection
- Addresses up to 4 Mega–bytes of address space with multiplexing of 11 row and 11 column addresses including 16 Megabyte DRAMs (4MB x 4).
- Addresses 16 and 64 Mega–byte DRAMs (to 64MB x 1) with a few inexpensive external parts.
- Memory access modes: page, fast page, interleaved page, nibble and static column
- Datapath word widths of 4 or 8 bytes or other sub-words are selectable by system designer
- Glueless dual port interface to any combination of CISC or, RISC processors, or DMA channels
- High speed block transfer capability controlled by row and column address counters and a presettable loop counter.
- Capable of 640 megabytes/second DMA transfers using a 64 bit data path
- Integrates 65,000 transistors using the QUBiC Advanced BiCMOS process

DESCRIPTION

The 74ABT4764 is a highly programmable dual port DRAM controller. At its core is a 80MHz PLD type sequencer that may be programmed using a simple assembly language consisting of three instructions: multi-way conditional call, conditional return and conditional toggle or assertion of output(s).

The following building blocks have been added to the PLD sequencer core with control split between the PLD and direct inputs:

- a row/column multiplexer,
- row and column address counters for auto incremented (burst or DMA) accesses.
- an eleven bit loop counter loadable from the row address or from the serial configuration register.
- four $\overline{RAS}$ signals and sixteen $\overline{CAS}$ signals to control four banks of DRAM with byte selection
- hit/miss logic for the four active pages.
- precharge circuitry which times the precharge of the last $\overline{RAS}$ while a new access is in progress,
- asynchronous arbitration of two access requests and refresh request,
- the metastable decay rate both for the arbiter and for the optional synchronizing flops is around 75ps.
- five each spare PLD inputs and outputs for customized handshaking,
- optional 3ns delay generators can be programmed into either the rising or falling edge of any of the twenty sequencer outputs.

The following capabilities arise from the listed pieces of hardware:

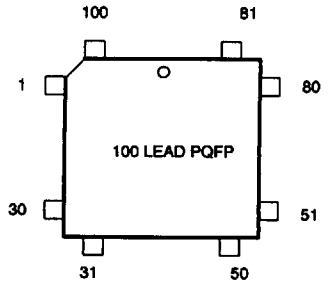
- two "glueless ports" can be built with very different functions and handshaking (eg., processor on one port with ultra high speed DMA on the other),
- current standard and most special DRAM features can be implemented according to system design requirements.
- the glueless ports can be designed with very different functions and handshaking
- very high speed burst accesses can be achieved using interleaved page or nibble mode
- large burst accesses (128K) can be handled across page boundaries
- very high speed burst accesses can be provided using interleaved page or nibble mode,
- very large (128K bytes) burst accesses can be done across page boundaries.

ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
100-pin Quad Flatpack	0° C to + 70° C	74ABT4764BB	SOT382-1

PIN CONFIGURATION

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	V_{CC}	26	$\overline{CAS02}$	51	BYTEN3	76	RADD5
2	Gnd	27	$\overline{CAS03}$	52	BYTEN4	77	CADD5
3	OUT5	28	CAS10	53	BYTEN5	78	RADD6
4	OUT4	29	$\overline{CAS11}$	54	BYTEN6	79	CADD6
5	OUT3	30	$\overline{CAS12}$	55	BYTEN7	80	RADD7
6	OUT2	31	Gnd	56	SERIN	81	CADD7
7	OUT1	32	$\overline{CAS13}$	57	B50	82	RADD8
8	Gnd	33	$\overline{CAS20}$	58	B51	83	CADD8
9	MA0	34	$\overline{CAS21}$	59	REFREQ	84	RADD9
10	MA1	35	$\overline{CAS22}$	60	REQ2	85	CADD9
11	MA2	36	$\overline{CAS23}$	61	REQ1	86	RADD10
12	MA3	37	$\overline{CAS30}$	62	RADD0	87	CADD10
13	MA4	38	Gnd	63	CADD0	88	OE
14	MA5	39	V_{CC}	64	RADD1	89	IN1
15	Gnd	40	$\overline{CAS31}$	65	V_{CC}	90	IN2
16	V_{CC}	41	$\overline{CAS32}$	66	Gnd	91	IN3
17	MA6	42	$\overline{CAS33}$	67	CADD1	92	IN4
18	MA7	43	$\overline{RAS0}$	68	RADD2	93	IN5
19	MA8	44	$\overline{RAS1}$	69	CADD2	94	$\overline{RESET}$
20	MA9	45	$\overline{RAS2}$	70	RADD3	95	CLK
21	MA10	46	$\overline{RAS3}$	71	CADD3	96	$\overline{TEST}$
22	NC	47	Gnd	72	NC	97	$\overline{SLAV/MSTR}$
23	$\overline{CAS00}$	48	BYTEN0	73	NC	98	$\overline{ADD2}$
24	Gnd	49	BYTEN1	74	RADD4	99	$\overline{ADD1}$
25	$\overline{CAS01}$	50	BYTEN2	75	CADD4	100	SERCLK



BLOCK DESCRIPTION

Boot-up loader

The 74ABT4764 is a shift register programmed part. This means that once the part has been powered up it must be programmed ("booted") before it will operate. The loading can take place in one of two modes, master and slave. In master mode, the part will divide the master clock (CLK) by 64 to create a shift clock signal with which it will drive the SCLK I/O. On each rising edge of SCLK the part will shift a new bit of information from SERIN into the program shift register until the part has loaded 4096 bits of information at which time SCLK will go back to the low state and then stop toggling. In slave mode the SCLK I/O will be in input, and the program shift register will accept a new bit of information from SERIN with each rising edge of SCLK. In this and other documents, the bit pattern loaded into the program shift register will be numbered from the trailing bit in the sequence (the first flip-flop in the serial chain). The last bit shifted in will reside in the *first flip-flop* in the program shift register and will be referred to as bit #1. The second to the last bit shifted in will be referred to as bit #2 and so on. There is a software package which allows the 74ABT4764 to be programmed without a detailed knowledge of the mapping of these bits into the actual hardware of the part, but the mapping is given in this document as a possible aid to the user.

80MHz user programmable sequencer

As mentioned before the sequencer core supports three simple instructions: conditional call, conditional return and conditional toggle or assertion of an output. Multiple instructions can be used on a given program line. For instance, the first program line might contain four or five call instructions each with its own set of conditions in order to differentiate the treatment of the accesses to active vs. inactive pages or burst versus conventional accesses. The line might also contain several conditional toggle instructions to handle the assertion of $\overline{CAS}$ for a page hit, the negation of $\overline{RAS}$ for a page miss, and/or various handshaking signals.

The programmable sequencer block is broken into three AND/NOR arrays (one for each instruction type) with 23 common inputs, a next address controller and output macros (see sequencer block diagram).

The largest of the three AND/NOR arrays has 38 product terms and 20 outputs. The 20 outputs are the outputs from the sequencer block. This organization allows a toggle instruction's program location and conditions to be encoded along a given product term in the AND array and its argument (the outputs to be toggled) to be encoded in the NOR array along the output of the product term. The 20 sequencer outputs have output macros which are individually programmable. The options available in these macros are: polarity, toggle flop registered or combinatorial, 3ns delayed falling edge, or no delay 3ns delayed rising edge. The delayed edge option can be useful in controlling the $\overline{OE}$ lines of the data transceivers in an interleaved page mode system where the $\overline{OE}$ of one bank should be negated before the $\overline{OE}$ of another bank is asserted.

The second of the three AND/NOR arrays has eight product terms and 7 outputs. The first of the 7 outputs from this array is an eight wide fixed NOR. This output drives the $\overline{CALL}$ line on the next address controller. The other six of the seven outputs use a programmable eight wide NOR. These outputs drive the call address lines of the next address controller. A call instruction's location and conditions are encoded along a given product term and the argument (destination address) in encoded along the output of this product term as it traverses the programmable NOR array.

The last of the AND/NOR arrays has 4 product terms with one fixed NOR output. This output line drives the $\overline{RET}$ line of the next address controller. A return instruction's program location and conditions are encoded along a given product term.

The next address controller handles three operations: call, return, and increment last address. The call instruction takes the incoming call address and makes it the new next address. At the same time it saves the incremented last address in the return address register. A return instruction restores the contents of this register to the next address. Since only the last return address is preserved, subroutine calls can only be one level deep. A call without a corresponding return becomes a jump instruction. The increment instruction is executed on any cycle where the $\overline{CALL}$ and $\overline{RET}$ signals are not asserted. The increment instruction simply increments the last address and uses it for the next address.

The sequencer block is programmed with bits 34 – 3241 of the program shift register. See the sequencer loading diagram for the proper mapping of these bits to a particular "fuse" location. A logical one programmed into any particular location will program that location to behave as an intact fuse, while a logical zero will program it to behave as a blown fuse.

Configurable 3 input arbitration block

This block has two access request inputs, a refresh request input (rising edge assertion), and a clear refresh request input (high REFCLR negates the refresh request). The arbitration block generates six outputs (REQ1, REQ2, REFRQ, GNT1, GNT2, REFG) which go to the sequencer and 2 more outputs ($\overline{ADD1}$ and $\overline{ADD2}$) which are outputs from the chip.

Since any or all of the requests can be asynchronous to the 4764 clock, the request/grant output pair generated from each request input can be programmed individually to go either directly into the sequencer or synchronized to the 4764 clock using 50ps tau synchronizing flops and then sent to the sequencer. This will avert any metastability problems in the sequencer.

The outputs REQ1 and REQ2 are either the raw processor request or their synchronized counterparts. REFRQ is a signal which is asserted on the rising edge of REFR and negated upon assertion of REFCLR and then is optionally synchronized to the 4764 clock. The dual signal control of REFRQ is used so the REFR can be driven by a free running oscillator.

The outputs GNT1, GNT2 and REFG are either the raw outputs of a 75ps tau asynchronous arbiter or synchronized outputs of the same. The inputs to this arbiter are the processor requests and REFRQ (before synchronization).

Both the requests and grants are sent to the sequencer to facilitate wait state generation, hidden refreshes and requests.

Programmable DRAM Controller

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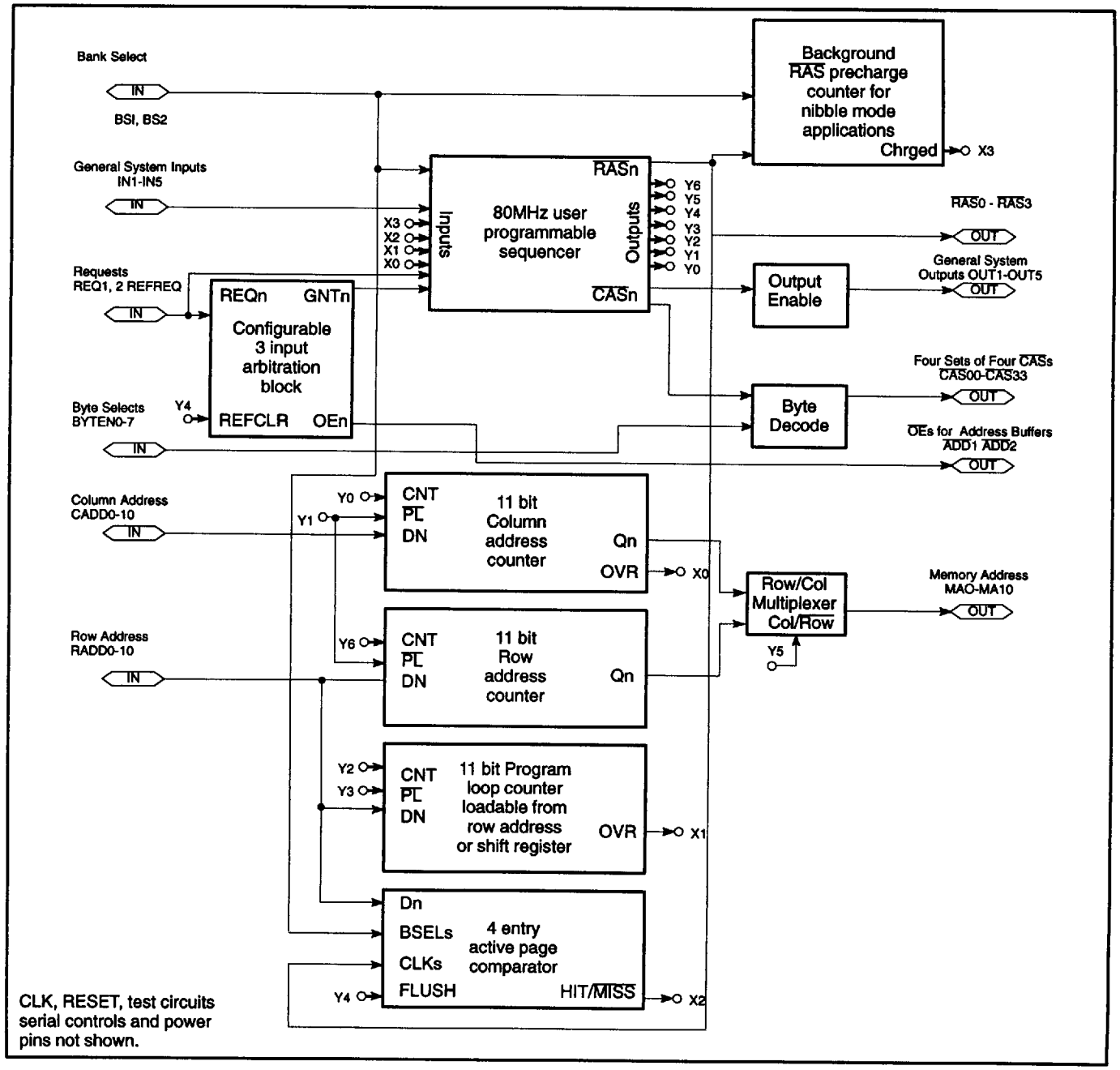
BLOCK DIAGRAM



The outputs $\overline{ADD1}$ and $\overline{ADD2}$ are generated to enable the appropriate processor's address bus and control signals onto the 4764 address and control inputs. The assertion on these signals lags the negation by about 3ns so contention between tristate drivers can be avoided. When neither one of the two processors has been granted an access, processor one's address is enabled so that this processor's access can be optimized for speed.

Bits 31, 32 and 33 of the program shift register enable the synchronization flip-flops for inputs REFREQ, REQ2, and REQ1 respectively. A logical one in any of these bits will cause the corresponding inputs and its associated grant to go through synchronizing flip-flops before being passed to the sequencer block. A signal which has been synchronized in this manner will always make transitions in response to the low to high transition of the master clock (CLK).

Four entry active page comparator

This block contains four active page registers. On the falling edge of $\overline{RAS}n$ register n is updated to the current row address. The register addressed by bank bits BS0 and BS1 is continually compared to the row address inputs and the results of this comparison is indicated by the internal signal HIT/$\overline{MISS}$.

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Precharge counter

$\overline{RAS}$ precharge time is independently monitored for each of the four $\overline{RAS}$ lines. The precharge status of a particular bank (particular $\overline{RAS}$ line) is selected by the bank bits BS0 and BS1. The precharge time is determined by a 3 bit code P programmed into the precharge counter block. For 8-P clock cycles following a low to high transition of a particular $\overline{RAS}$ line, the precharge status of the memory bank served by that line will not be charged (CHRGED=0). It is of course up to the programmer to decide when (if ever), and how this information will be used. The 3 bit code P resides in program shift register bits 1 through 3, with bit 1 being the most significant bit and bit 3 the least significant bit.

Program loop counter

This counter allows looping control for large block moves. The operation should be programmed as follows. First, the counter is loaded from either the row address or from the program shift register. Each time through the loop the controller will access a predetermined number of sequential words in memory and strobe the internal Loop Count line (Y2) to increment the counter. A conditional call might need to be placed strategically in this loop to handle page overflow on large blocks. At the end of the loop a call instruction to the beginning of the loop would be made on condition the internal signal Loop Counter Overflow (I1) is not asserted.

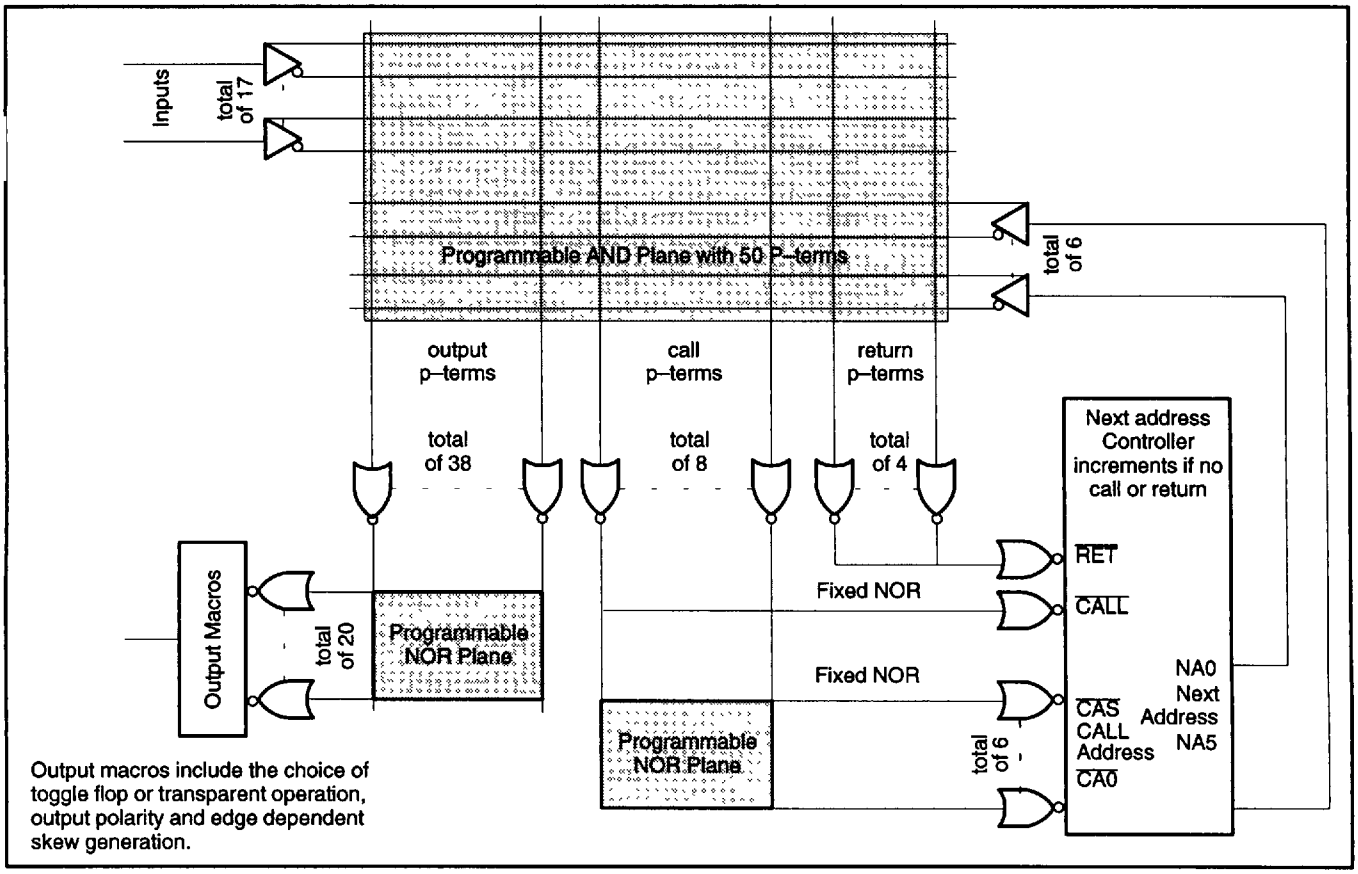
If bit 15 of the program shift register has been programmed to a logical one, the 11 bit counter will get loaded from the row address input bus, but apart from this difference, the operation of the counter will remain as described.

Byte decode

The byte decode block was designed primarily with 32 bit and 64 bit processors in mind. since the 4764 has only 16 $\overline{CAS}$ outputs for 4 memory banks, the 64 bit processor must use at least a two way interleaved access where the $\overline{CAS}$ lines of two banks are shared. To allow this, the eight CASEN inputs are mapped onto a first and second set of eight $\overline{CAS}$ outputs. As a result, 32 bit processors will need to tie the first set of four CASEN signals to the second set. (Application notes detailing 32 bit, 64 bit and mixed bit width designs are being written.)

The signal RFSH (Y4) from the sequencer is a refresh output which will enable all $\overline{CAS}$ outputs (overriding the BYTN inputs) as well as clearing the active flag open all of the active pages and clearing the refresh request flip-flop.

BLOCK DIAGRAM FOR HIGH SPEED SEQUENCER PORTION



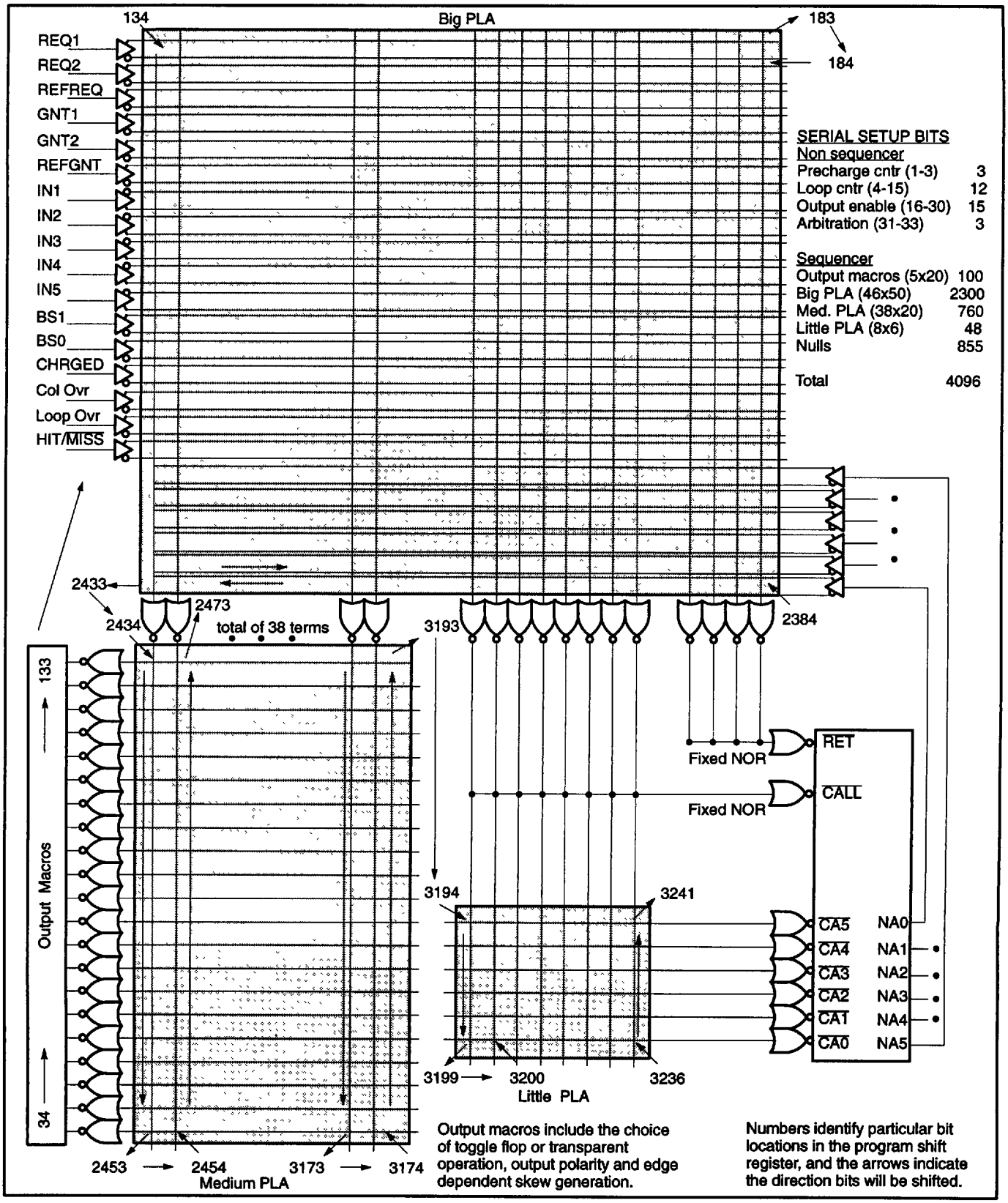
Output macros include the choice of toggle flop or transparent operation, output polarity and edge dependent skew generation.

Output enabling macros

The general system outputs have individually programmable tristate controls. They can be configured to be enabled by processor one's request, processor two's request or always. This allows them to directly drive wait, ready or acknowledge lines which are shared with other devices.

Bits 16 - 30 of the program shift register are divided into 5 groups of three bits each. Each group controls the output enable to one of the five general system outputs (16 - 18 control OUT1's OE and so on). In each group of three bits there must be one and only one bit set to a one. Setting the first bit in a group will assert the OE all the time, setting the second bit in a group will assert the OE when REQ2 is asserted, and setting the third bit will assert the OE when REQ1 is asserted.

SERIAL SET UP LOADING DIAGRAM



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PIN DESCRIPTIONS

PIN NAME(s)	I/O	FUNCTION
RADD0 – RADD10	I	Row address inputs. These inputs can also be used to load the program loop counter
CADD0 – CADD10	I	Column address inputs.
MA0 – MA10	O	Memory address outputs
BS0, BS1	I	Bank select inputs. These two lines tell the 4764 which of the four possible memory banks the selected processor would like to access. The 4764 will use this information together with the incoming row address to generate the internal signals. HIT/$\overline{\text{MISS}}$ and CHRGED.
$\overline{\text{RAS0}}$ – $\overline{\text{RAS3}}$	O	Row address strobe outputs. There is one $\overline{\text{RAS}}$ signal for each of four potential banks of DRAM.
BYTEN0 – BYTEN7	I	Byte enable inputs. Each BYTEN controls a byte in each of two 8 byte wide memory banks. For 32 bit processors, BYTEN0–3 should be tied to BYTEN4–7 respectively, so that each BYTEN pair now controls a byte in each of four 4 byte wide memory banks. For example: since BYTEN0 enables $\overline{\text{CAS}}$00 and 20 and BYTEN4 enables $\overline{\text{CAS}}$10 and 30, the pair BYTEN0, 4 will enable $\overline{\text{CAS}}$00, 10, 20 and 30.
$\overline{\text{CAS00}}$ – $\overline{\text{CAS03}}$ $\overline{\text{CAS10}}$ – $\overline{\text{CAS13}}$ $\overline{\text{CAS20}}$ – $\overline{\text{CAS23}}$ $\overline{\text{CAS30}}$ – $\overline{\text{CAS33}}$	O	Sixteen column address strobe outputs grouped in four groups of four. Each $\overline{\text{CAS}}$ line is meant to control a single byte in the memory array. The first digit in the $\overline{\text{CAS}}$ number designates the bank and the second digit designates the byte. The numbering on these pins is appropriate for a 32 bit system where there are four bytes in each of four memory banks. For a 64 bit system, group bank zero with bank one and bank two with bank three.
REQ1, REQ2	I	Access request inputs for ports one and two.
REFREQ	I	Refresh request input. This input is rising edge triggered so it can be driven by a free running oscillator or as a derivative of the main clock.
$\overline{\text{ADD1}}$, $\overline{\text{ADD2}}$	O	Address enable outputs. These signals are meant to directly drive the $\overline{\text{OE}}$ pins on the address buffers from the respective processors. these two pins have circuitry which delays the assertion with respect to the negation, so any "cross-over glitch" can be avoided. $\overline{\text{ADD1}}$ will be asserted in REQ1 is asserted before REQ2 or if neither request is asserted. $\overline{\text{ADD2}}$ will be asserted if REQ2 is asserted before REQ1. This operation permits optimizing assumptions to be made about the address setup time on port one.
IN1 – IN5	I	General system inputs. These inputs are useful for handling special handshake signals like burst request, etc.
OUT1 – OUT5	O	General system outputs. These outputs have special output macros (in addition to the sequencer output macros) that determine when they will be enabled. The output macros can be programmed to enable a particular output when REQ1 is asserted, when REQ2 is asserted, or always. This is especially useful when using an output to drive a DTACK or WAIT signal that might also be driven by some other device.
CLK	I	Master clock input. Rising edge triggered.
$\overline{\text{RESET}}$	I	Active low master reset. Sets the internal state bits to all zeros, clears the valid bit in each of the four active page registers, clears the counter in the master mode serial loader, and clears the flops in the 20 output macros from the sequencer.
OE	I	Output enable input. A low on OE disables the memory address lines, the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lines and $\overline{\text{ADD1}}$ and $\overline{\text{ADD2}}$. A high on OE enables them.
SERIN	I	Serial data input. The bit pattern which configures the 74ABT4764 is loaded through SERIN on boot-up.
SERCLK	I	Serial CLK input for slave mode and output for master mode. A rising edge on SERCLK clocks data through SERIN into the input of the configuration shift register.
SLAV/$\overline{\text{MASTR}}$	I	Slave/not Master input. A high SLAV/$\overline{\text{MASTR}}$ dictates that some outside controller must drive the SERCLK line while presenting data to the SERIN input. A high on SLAV/$\overline{\text{MASTR}}$ will cause the 74ABT4764 to clock 4K bits from some outside data source using the SERCLK and SERIN pins.
$\overline{\text{TEST}}$	I	Active low test input. A low on this pin provides tester access to internal nodes of the chip and splits the serial loading into several separate pieces.

INTERNAL SIGNAL DESCRIPTION

SIGNAL NAME	NODE LABEL	FUNCTION
Column Count	Y0	Rising edge clocks the column address counter.
$\overline{\text{Address Load}}$	Y1	Low level loads the new address into the address counters.
Loop Count	Y2	Rising edge clocks the loop counter.
$\overline{\text{Loop Load}}$	Y3	Low level loads the loop counter from the row address or from the serial configuration register (as directed by the serial configuration register).
RFSH	Y4	High level enables all bytes (over-riding the byte enables), clears the valid bit in each of the four active page registers, and clears the refresh request flip-flop.
Column/$\overline{\text{Row}}$	Y5	A high level selects the column address to be multiplexed to the memory address outputs and a low level selects the row address.
Row Count	Y6	Rising edge clocks the row address counter has rolled over to all zeros.
Column Overflow	X0	A high signals that the column address has rolled over to all zeros.
Loop Counter Overflow	X1	A high signals that the loop counter has rolled over to all zeros.
HIT/$\overline{\text{MISS}}$	X2	A high on this line signals that the incoming row address matches the last one used to access the bank currently addressed by BS0 and BS1, and that the appropriate $\overline{\text{RAS}}$ line has been held low since that time (page hit). A low on this line signals that one of these two conditions has not been met (page miss).
CHRGED	X3	A high on this line signals that the $\overline{\text{RAS}}$ line addressed by BS0 and BS1 has met the precharge criteria set forth in the serial configuration register.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min.	Max.	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH1} I_{OH2}	High-level output current		−15 −25	mA
I_{OL1} I_{OL2}	Low-level output current		24 60	mA
$\Delta t/\Delta V$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	0	+70	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	V
V_I	DC input voltage[2]		−1.2 to + 7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	V
V_O	DC output voltage[2]	output in Off or High state	−0.5 to + 5.5	V
I_O	DC output current	output in Low state	128	mA
T_{STG}	Storage temperature range		−65 to 150	mA

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			LIMITS		UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85 °C		
			Min	Typ	Max	Min	Max	
V_{CD}	Clamp diode voltage	V_{CC} = 5.5V	−1.2	−0.8		−1.2		V
I_{IL}	Low-level input current	V_{CC} = 5.5V	−20.0	0	20.0	−20.0	20.0	µA
I_{IH}	High-level output current	V_{CC} = 5.5V	−20.0	0	20.0	−20.0	20.0	µA
V_{OL1}	Low-level output voltage	V_{CC} = 4.5V; I_O = 24mA		350	500.0		500.0	mV
V_{OL2}	Low-level output voltage	V_{CC} = 4.5V; I_O = 60mA		550	800.0		550	mV
V_{OH1}	High-level output voltage	V_{CC} = 4.5V; I_O = −15mA	2.5	3.7		2.5	3.7	V
V_{OH2}	High-level output voltage	V_{CC} = 4.5V; I_O = −35mA	2.4	3.5		2.4	3.5	V
I_O	Output current	V_{CC} = 5.5V; V_O = 2.25V	−200	−140	−50	−200	−140	mA
I_{OZL}	Off state output current, low level voltage applied	V_{CC} = 5.5V; V_O = 0.5V	−50.0	0	50.0	−50.0	0	µA
I_{OZH}	Offstate output current, high level voltage applied	V_{CC} = 5.5V; V_O = 2.7V	−50.0	0	50.0	−50.0	0	µA
I_{CC}	Supply current							
I_{CC0}	– Serial register at 0's			85	130		130	mA
I_{CCL}	– Outputs low	V_{CC} = 5.5V		137	200		200	mA
I_{CCH}	– Outputs high			75	110		110	mA
I_{CCZ}	– Outputs off			57	90		90	mA

AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V RL = 70Ω CL = 50pf			T_{amb} = 0 to +70°C V_{CC} = +5.0V ±0.5V RL = 70Ω CL= 50pf		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum CLK frequency	Waveform 1	90	95		80		MHz
t_{PLH} t_{PHL}	Skew – no skew delta[1]	Waveform 2	1.9	3.0	5.5	1.5	6.0	ns
t_{PLH} t_{PHL}	CLK to RASn[2]	Waveform 1	5.0	8.3	12.0	4.5	13.0	ns
t_{PLH} t_{PHL}	CLK thru CAS0-3 inverted to CAS00-33	Waveform 1	6.0	9.0	12.0	5.0	13.0	ns
t_{PLH} t_{PHL}	BYTEN to CAS00-33[2]	Waveform 2	1.0	4.2	8.0	1.0	8.5	ns
t_{PLH} t_{PHL}	CLK thru Y0, Y6 (row column count) to MAn	Waveform 1	6.5	12.0	20.0	5.5	22.0	ns
t_{PLH} t_{PHL}	CLK thru Y1 (row/column parallel load) to MAn[2]	Waveform 1	7.0	12.0	18.0	6.5	19.0	ns
t_{PLH} t_{PHL}	CLK thru Y5 (row/column mux) rising or falling to MAn[2]	Waveform 1	6.0	10.0	14.5	5.0	16.0	ns
t_{PLH} t_{PHL}	IN1-5 to OUT1-5 transparent	Waveform 2	4.0	8.5	13.0	3.5	13.5	ns
t_{PLH} t_{PHL}	RADDn or CADDn to MAn, non-inverting	Waveform 2	3.0	7.0	12.0	2.5	13.5	ns
t_{PLH} t_{PHL}	CLK to OUTn[2]	Waveform 1	5.0	8.0	11.5	4.5	12.5	ns
t_{PZH} t_{PZL}	REQ1 or REQ2 to OUT1-5	Waveform 2	3.0	5.8	9.0	2.5	9.5	ns
t_{PHZ} t_{PLZ}	REQ1 or REQ2 to OUT1-5	Waveform 2	1.2	4.0	7.0	0.8	7.5	ns
t_{PLH}	REQ1 or REQ2 high or low to ADD1 or ADD2	Waveform 2	1.5	5.2	9.0	1.0	9.5	ns
t_{PHL}	REQ1 to ADD1 or REQ2 to ADD2	Waveform 2	5.0	8.5	12.0	4.5	13.0	ns

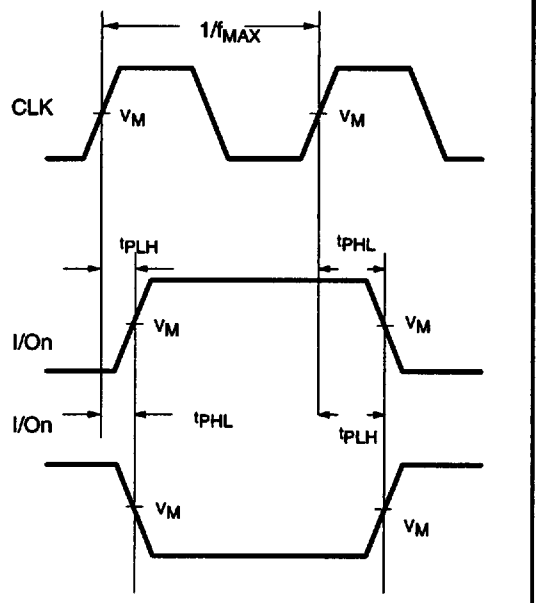
NOTES:

1. All propagation delays are shown with no skew except this delta which shows the difference between skewed and unskewed data. To calculate a propagation delay with skews, add to the given unskewed delays the skew minus no skew delta parameters as given on line two of the table — minimum to minimum, typical to typical and maximum to maximum. For example, the unskewed CLK to RASn data becomes (5.0 + 1.9) = 6.9ns minimum, (8.3 + 3.0) = 11.3ns typical and (12.0 + 5.5) = 17.5ns maximum at nominal conditions.
2. These parameters are skewable by selecting the appropriate output macro codes for the sequencer whose delays follow the rule mentioned in Note 1.

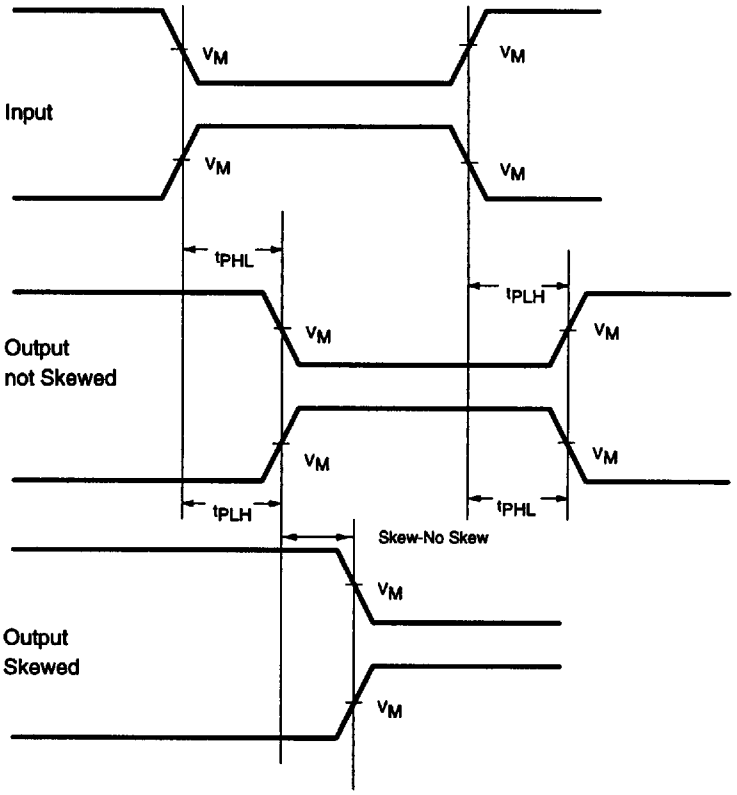
AC SETUP/HOLD REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = 0 to +70°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{SH} t_{SL}	REQ to CLK to output macro, toggle or no toggle	Waveform 3	1.5	4.7	8.5	1.0	9.5	ns
t_{HH} t_{HL}	REQ to CLK to output macro, toggle or no toggle	Waveform 3	–8.5	–4.7	–1.5	–9.5	–1.0	ns
t_{SH}	REFREQ to CLK to output macro	Waveform 3	3.0	5.7	9.0	2.0	10.0	ns
t_{SH} t_{SL}	INn to CLK to output macro, toggle or no toggle	Waveform 3	–1.0	2.7	6.5	–2.0	7.0	ns
t_{HH} t_{HL}	INn to CLK to output macro, toggle or no toggle	Waveform 3	–6.5	–2.7	1.0	–7.0	2.0	ns
t_{SH}	REQ1-2 to CLK to sequencer address	Waveform 3	2.0	5.0	8.5	1.0	9.0	ns
t_{HL}	REQ1-2 to CLK to sequencer address	Waveform 3	–8.5	–5.0	–2.0	–9.0	–1.0	ns
t_{SH}	IN1-5 to CLK to sequencer address	Waveform 3	0.5	4.0	7.5	0.0	8.5	ns
t_{HL}	IN1-5 to CLK to no sequencer address	Waveform 3	–7.5	–4.0	–0.5	–8.5	0.0	ns
t_{SH} t_{SL}	BS0 to HIT to CLK to sequencer address	Waveform 3		7.0				ns
t_{SH} t_{SL}	RADD0 to HIT/$\overline{MISS}$ to CLK to sequencer address	Waveform 3		5.3				ns

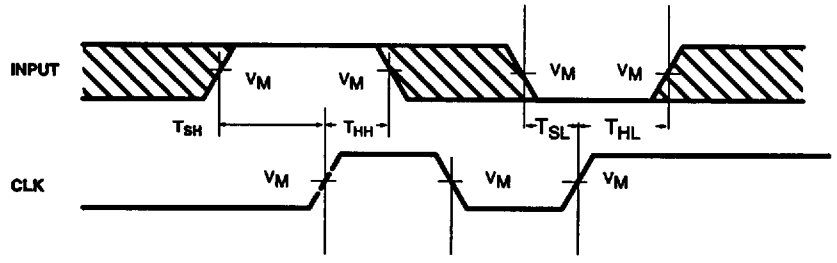
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output and Maximum Clock Frequency

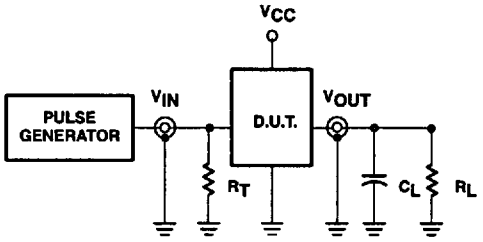


Waveform 2. General Propagation Delay, Input to Output, Skewed vs. Non Skewed Outputs



Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS



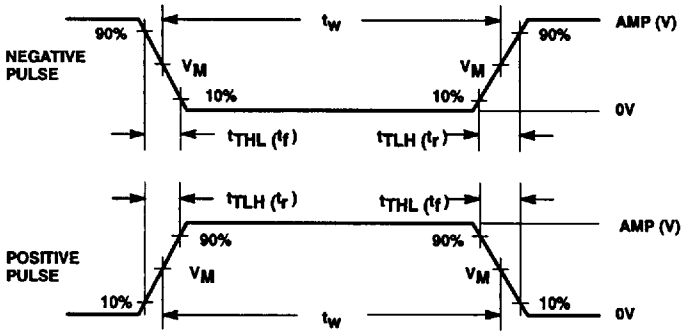
Test circuit for Totem-Pole Outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74ABT	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

1420A/SOT382-1 100-PIN PLASTIC QUAD FLAT PACK, RECTANGULAR (BB) PACKAGE