



GAL20V8A/883

High Performance E²CMOS PLD

T-46-19-07 Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
 - 15 ns Maximum Propagation Delay
 - $F_{max} = 50$ MHz
 - 12 ns Maximum from Clock Input to Data Output
 - TTL Compatible 24 mA Outputs
 - UltraMOS™ Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
 - 75mA Typ I_{cc} on Low Power Device
 - 45mA Typ I_{cc} on Quarter Power Device
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<100ms)
 - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Programmable Output Polarity
 - Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

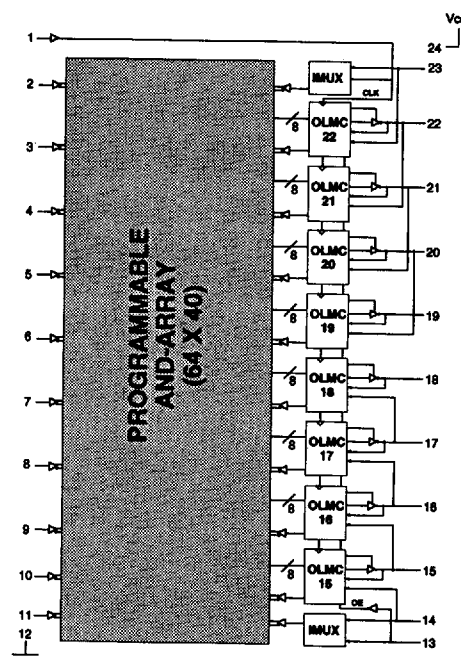
DESCRIPTION

The GAL20V8A/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. The GAL20V8A/883, at 15ns maximum propagation delay time, is the world's fastest military qualified 24-pin CMOS PLD. CMOS circuitry allows the GAL20V8A quarter power device to consume just 45mA typical I_{cc} , which represents a 75% savings in power when compared to bipolar counterparts.

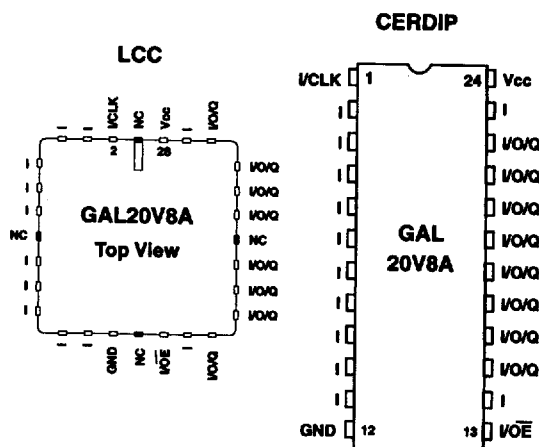
Generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20V8A/883 is capable of emulating all standard 24-pin PAL® devices with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

May 1992

Specifications **GAL20V8A/883****ABSOLUTE MAXIMUM RATINGS⁽¹⁾**

Supply voltage V_{CC} -0.5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 150°C
 Case Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) -55 to 125°C
 Supply voltage (V_{CC})
 with Respect to Ground +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	—	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. \quad V_{IN} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	12	mA
I_{OH}	High Level Output Current		—	—	-2.0	mA
I_{OS}^1	Output Short Circuit Current	$V_{CC} = 5V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$	-30	—	-150	mA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V \quad V_{IH} = 3.0V$ L -15/-20/-30	—	75	130	mA
		Outputs Open (no load) $f_{toggle} = 25MHz$ Q -20/-25	—	45	65	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at $V_{CC} = 5V$ and $T_A = 25^\circ C$

CAPACITANCE ($T_A = 25^\circ C, f = 1.0 MHz$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	10	pF	$V_{CC} = 5.0V, V_i = 2.0V$
C_{iO}	I/O Capacitance	10	pF	$V_{CC} = 5.0V, V_{iO} = 2.0V$

*Guaranteed but not 100% tested.

Specifications **GAL20V8A/883****AC SWITCHING CHARACTERISTICS**

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Over Recommended Operating Conditions

PARAMETER	TEST COND ¹	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	Input or I/O to Combinational Output	3	15	3	20	3	25	3	30	ns
t_{co}	1	Clock to Output Delay	2	12	2	15	2	15	2	20	ns
t_{cf}	—	Clock to Feedback Delay	—	12	—	15	—	15	—	20	ns
t_{su}	—	Setup Time, Input or Feedback before Clock	12	—	15	—	20	—	25	—	ns
t_h	—	Hold Time, Input or Feedback after Clock	0	—	0	—	0	—	0	—	ns
f_{max} ³	1	Maximum Clock Frequency with External Feedback, $1/(t_{su} + t_{co})$	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, $1/(t_{su} + t_{cf})$	41.6	—	33.3	—	28.5	—	22.2	—	MHz
	1	Maximum Clock Frequency with No Feedback	50	—	41.6	—	33.3	—	33.3	—	MHz
t_{wh}	—	Clock Pulse Duration, High	10	—	12	—	15	—	15	—	ns
t_{wl}	—	Clock Pulse Duration, Low	10	—	12	—	15	—	15	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	20	—	25	—	30	ns
	2	$\overline{OE}$ to Output Enabled	—	15	—	18	—	20	—	25	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	20	—	25	—	30	ns
	3	$\overline{OE}$ to Output Disabled	—	15	—	18	—	20	—	25	ns

1) Refer to Switching Test Conditions section.

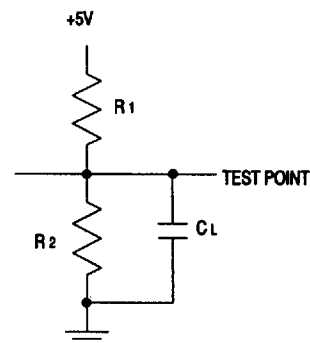
2) Calculated from f_{max} with internal feedback. Refer to f_{max} Descriptions section.3) Refer to f_{max} Descriptions section.**SWITCHING TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

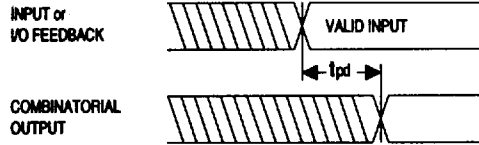
Test Condition	R_1	R_2	C_L
1	390 Ω	750 Ω	50pF
2	∞	750 Ω	50pF
3	∞	750 Ω	5pF

FROM OUTPUT (O/Q)
UNDER TEST C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

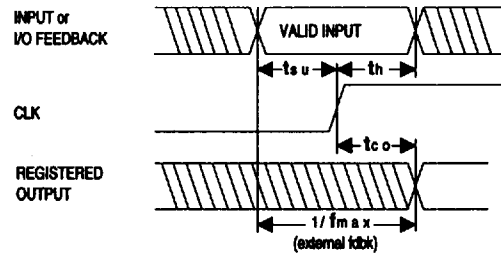
Specifications ***GAL20V8A/883***

SWITCHING WAVEFORMS

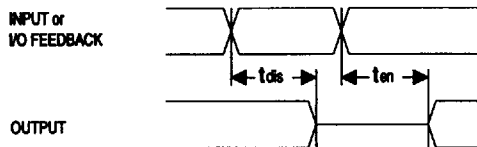
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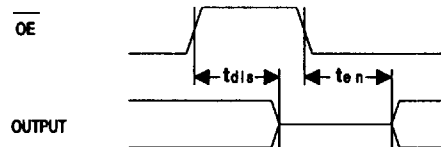
Combinatorial Output



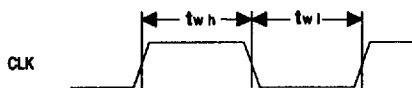
Registered Output



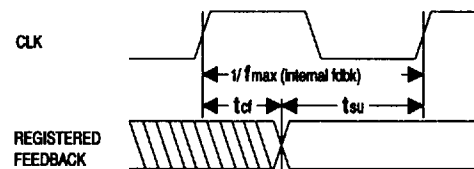
Input or VO to Output Enable/Disable



OE to Output Enable/Disable

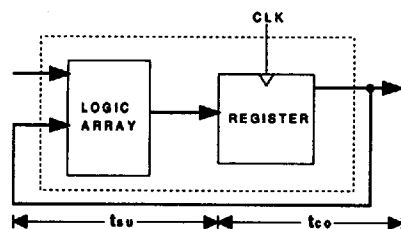


Clock Width

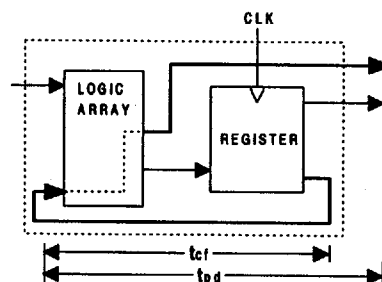
 f_{max} with Feedback

Specifications **GAL20V8A/883**

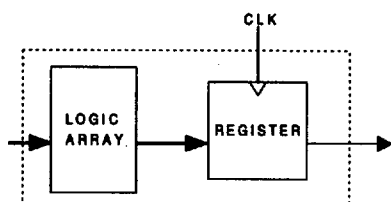
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f_{max} DESCRIPTIONS**f_{max} with External Feedback $1/(t_{su}+t_{co})$**

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.

**f_{max} with Internal Feedback $1/(t_{su}+t_{cf})$**

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback ($t_{cf} = 1/f_{max} - t_{su}$). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

**f_{max} Without Feedback**

Note: f_{max} with no feedback may be less than $1/(t_{wh} + t_{wf})$. This is to allow for a clock duty cycle of other than 50%.

Specifications **GAL20V8A/883**

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GAL20V8A ORDERING INFORMATION (MIL-STD-883 and SMD)

					Ordering #	
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	MIL-STD-883	SMD #
15	12	12	130	24-Pin Cerdip	GAL20V8A-15LD/883	5962-8984003LA
			130	28-Pin LCC	GAL20V8A-15LR/883	5962-89840033A
20	15	15	65	24-Pin Cerdip	GAL20V8A-20QD/883	Contact Factory
			65	28-Pin LCC	GAL20V8A-20QR/883	Contact Factory
			130	24-Pin Cerdip	GAL20V8A-20LD/883	5962-8984002LA
			130	28-Pin LCC	GAL20V8A-20LR/883	5962-89840023A
25	20	15	65	24-Pin Cerdip	GAL20V8A-25QD/883	Contact Factory
			65	28-Pin LCC	GAL20V8A-25QR/883	Contact Factory
30	25	20	130	24-Pin Cerdip	GAL20V8A-30LD/883	5962-8984001LA
			130	28-Pin LCC	GAL20V8A-30LR/883	5962-89840013A

Note: Lattice recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number where it exists is recommended.

PART NUMBER DESCRIPTION