

# Product Preview

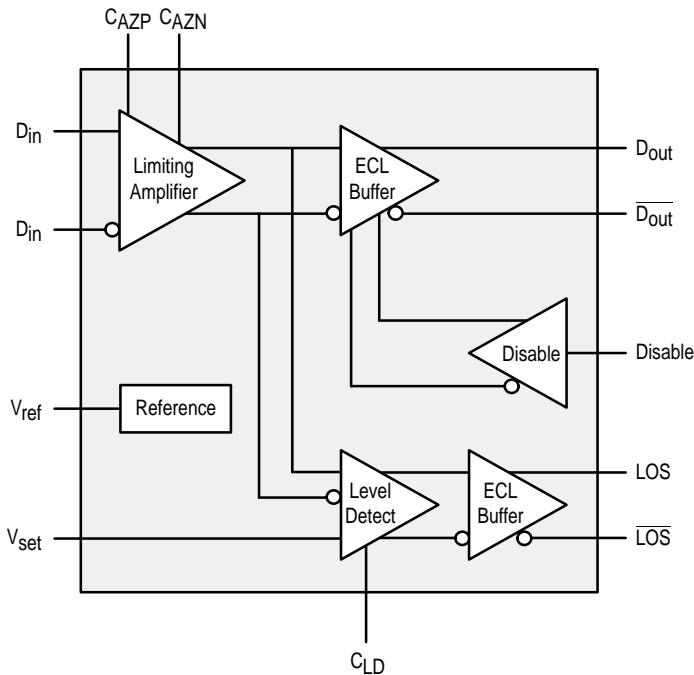
## 1.25Gb/s Fiber Optic Post Amplifier

The MC10SX1126 is an integrated limiting amplifier for high frequency fiber optic applications. The device interfaces directly to the trans-impedance amplifier of a typical optical to electrical conversion portion of a fiber optic link. With data rate capabilities in the 1.25Gb/s range, the high gain limiting amplification of the SX1126 is ideal for high speed fiber optic applications like SONET/SDM, ATM, FDDI, Fibre Channel or Serial Hippi. The device is functionally and pin compatible to the Signetics SA5225 with a significantly higher bandwidth. The CAZP and CAZN inputs to the limiting amplifier provide an auto-zero function to effectively cancel any input offset voltage present in the amplifier.

The SX1126 incorporates a programmable level detect function to identify when the input signal has been lost. This information can be fed back to the Disable input of the device to maintain stability under loss of signal conditions. Using the Vset pin the sensitivity of the level detect can be adjusted. The CLD input is used to filter the level detect input so that random noise spikes are filtered out.

The MC10SX1126 is compatible with MECL10H logic levels.

- Wideband Operation: 50MHz to 900MHz
- Programmable Input Signal Level Detection
- Operation with single +5V or standard ECL supply
- Standard 16-lead SOIC Package
- Fully Differential Design to Minimize Noise Affects
- 10KH Compatible



**Figure 1. MC10SX1126 Block Diagram**

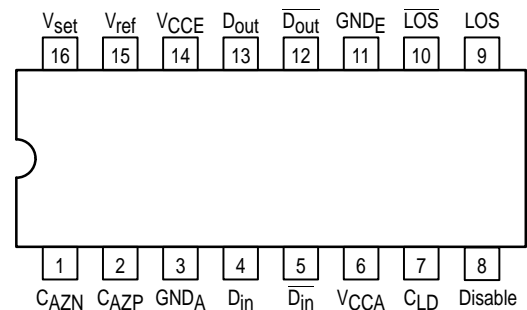
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# MC10SX1126

## FIBER OPTIC POST AMPLIFIER



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B-05

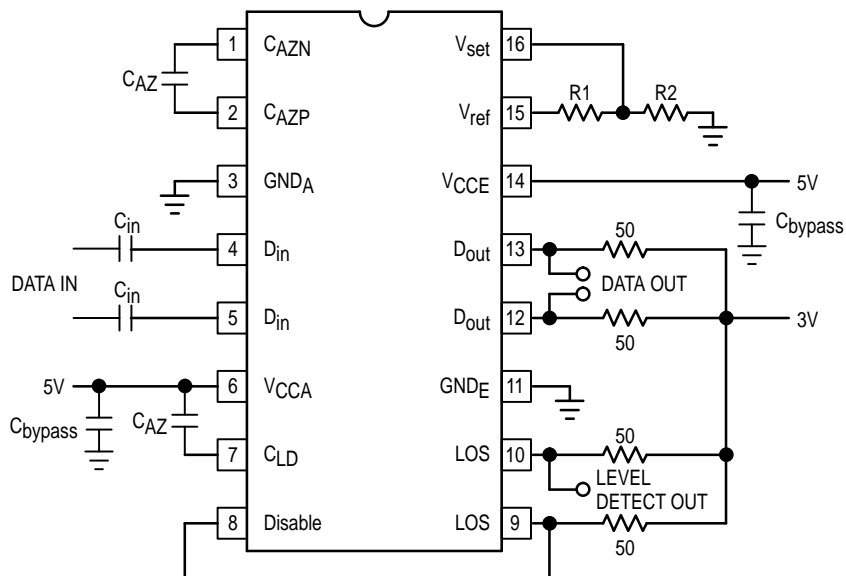


**Figure 2. 16-Lead Pinout (Top View)**



**FUNCTION TABLE**

| Pin                                     | Function  |
|---|---|
| CAZN                                    | Auto-zero capacitor pin. A capacitor between this pin and CAZP cancels any offset inherent to the limiting amplifier.   |
| CAZP                                    | Auto-zero capacitor pin. A capacitor between this pin and CAZN cancels any offset inherent to the limiting amplifier.   |
| GND <sub>A</sub>                        | Analog ground pin. Ground for PECL operation or -5.2V for standard ECL operation. GND <sub>A</sub> and GND <sub>E</sub> must be at the same potential.  |
| D <sub>in</sub> , $\overline{D}_{in}$   | Differential data input.  |
| V <sub>CCA</sub>                        | Analog power supply pin. +5V for PECL operation or ground for standard ECL operation. V <sub>CCA</sub> and V <sub>CCE</sub> must be at the same potential.  |
| C <sub>LD</sub>                         | Filter capacitor for the level detect comparator. Capacitor should be connected to V <sub>CCA</sub> .   |
| Disable                                 | When asserted LOW, or left open and pulled LOW via the input pulldown resistor, the output buffer will be enabled and will respond to the input stimulus on the D <sub>in</sub> input. Forcing Disable HIGH will force the D <sub>out</sub> output LOW and its complimentary output HIGH. |
| LOS                                     | Loss of signal. This output will go HIGH when the input signal falls below (V <sub>set</sub> /100) mVp-p.   |
| GND <sub>E</sub>                        | Digital ground pin. Ground for PECL operation or -5.2V for standard ECL operation. GND <sub>A</sub> and GND <sub>E</sub> must be at the same potential.   |
| D <sub>out</sub> , $\overline{D}_{out}$ | Differential data outputs.  |
| V <sub>CCE</sub>                        | Digital power supply pin. +5V for PECL operation or ground for standard ECL operation. V <sub>CCA</sub> and V <sub>CCE</sub> must be at the same potential.   |
| V <sub>ref</sub>                        | Reference voltage for threshold level set voltage division network (2.64V).   |
| V <sub>set</sub>                        | Input threshold level detect setting input. Input generated from voltage divider between V <sub>ref</sub> and GND <sub>A</sub> .  |



**Figure 3. Typical Operating Circuit**

**Coupling Capacitors**

The SX1126 inputs must be AC coupled to allow proper operation of the offset correction function. The coupling capacitors,  $C_{in}$ , must be large enough to pass the lowest input frequency of interest.

$$C_{in} = \frac{1}{2\pi (R_{in}) (f_{low})}$$

where  $R_{in}$  = input resistance = 5000Ω  
 $f_{low}$  = lowest frequency.

**Auto-zero Capacitors**

A feedback amplifier is used to cancel the offset voltage of the forward signal path, so the input to the internal ECL comparator is at its toggle point in the absence of any input signal. The time constant of the cancelling circuitry is set by an external capacitor ( $C_{AZ}$ ) connected between Pins 1 and 2. The formula for the calculation of the auto-zero capacitor is:

$$C_{AZ} = \frac{150}{2\pi (R_{AZ}) (f_{low})}$$

where  $R_{AZ}$  = internal driving impedance = 290kΩ  
 $f_{low}$  = lowest frequency.

**Input Signal Level Detector**

The SX1126 allows for user programmable input signal level-detection and can automatically disable the switching of its ECL data output if the input level is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and ensures that data will only be transmitted when the signal-to-noise ratio is sufficient for low bit-error-rate system operation. Complimentary ECL flags (LOS and LOSB) indicate whether the input signal is above or below the desired threshold level. In the level detect system, the input signal is amplified and rectified before being compared to a programmable reference. A filter is included to prevent noise spikes from triggering the level-detector. The filter has a nominal 1μs time constant, and additional filtering can be achieved by using an external capacitor ( $C_{LD}$ ) from Pin 7 to  $V_{CCA}$  (the internal driving impedance is nominally 28k). The formula for the calculation of the  $C_{LD}$  capacitor is:

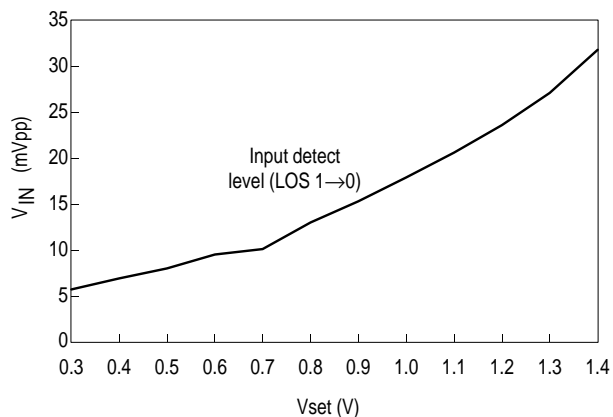
$$C_{LD} = \frac{t}{R_Z}$$

where  $R_Z$  = internal driving impedance = 28kΩ  
 $t$  = LOS filter time constant.

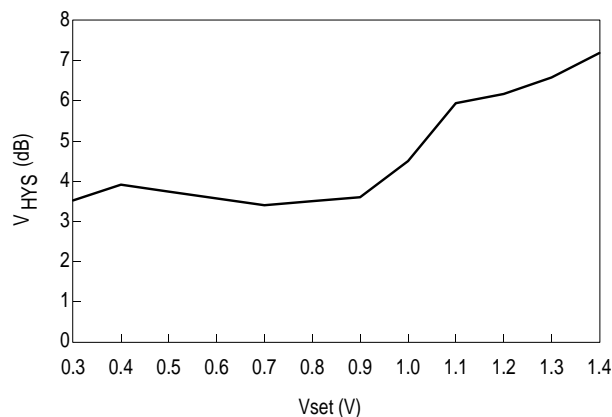
**DC CHARACTERISTICS** ( $GND_A = GND_E = \text{Ground}$ ;  $V_{CCA} = V_{CCE} = 4.5V \text{ to } 5.5V$ )

| Symbol    | Characteristic                                 | Min   | Typ | Max | Unit              | Condition |
|-----------|--|-------|-----|-----|-------------------|-----------|
| $V_{IN}$  | Input Signal Voltage ( $D_{in}$ ) Single-Ended | 0.008 |     | 1.5 | V <sub>P-P</sub>  | Note 1.   |
| $V_{OS}$  | Input Offset Voltage                           |       |     | 50  | μV                |           |
| $V_N$     | Input RMS Noise                                |       |     | 225 | μV                |           |
| $V_{TH}$  | Input Level Detect Programmability             | 8.0   |     | 20  | mV <sub>P-P</sub> |           |
| $V_{HYS}$ | Level Detect Hysteresis                        | 1.5   | 2.5 | 7.0 | dB                | Note 2.   |
| $I_{IH}$  | Input HIGH Current Disable                     |       |     | 150 | μA                |           |
| $I_{CC}$  | Power Supply Current                           |       | 33  | 45  | mA                |           |

1. This device functions with  $V_{INmin} = 6mV_{P-P}$ , but with increased BER (See BER data).
2. This device has an anomaly in  $V_{HYS}$  when  $0.65 < V_{SET} < 0.75V$ . Operation in this region is not recommended. (See Figure 5)



**Figure 4. LOS versus Vset** ( $T_A = 25^\circ C$ )



**Figure 5. LOS Hysteresis** ( $T_A = 25^\circ C$ )

**I/O DC CHARACTERISTICS** (Note 3.)

| Symbol          | Characteristic  | -40°C         |               | 0°C           |               | 25°C          |               | 85°C          |               | Unit |
|-----------------|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|------|
|                 |   | Min           | Max           | Min           | Max           | Min           | Max           | Min           | Max           |      |
| V <sub>OH</sub> | Output HIGH Voltage<br>V <sub>CC</sub> = -4.5 to -5.5V<br>V <sub>CC</sub> = 5.0V (Note 4.)          | 1080<br>3920  | -890<br>4110  | 1020<br>3980  | -840<br>4160  | -980<br>4020  | -810<br>4190  | -910<br>4090  | -720<br>4280  | mV   |
| V <sub>OL</sub> | Output LOW Voltage<br>V <sub>CC</sub> = -4.5 to -5.5V<br>V <sub>CC</sub> = 5.0V (Note 4.)           | -1950<br>3050 | -1650<br>3350 | -1950<br>3050 | -1630<br>3370 | -1950<br>3050 | -1630<br>3370 | -1950<br>3050 | -1595<br>3405 | mV   |
| V <sub>IH</sub> | Input HIGH Voltage (Note 5.)<br>V <sub>CC</sub> = -4.5 to -5.5V<br>V <sub>CC</sub> = 5.0V (Note 4.) | -1230<br>3770 | -890<br>4110  | -1170<br>3830 | -840<br>4160  | -1130<br>3870 | -810<br>4190  | -1060<br>3940 | -720<br>4280  | mV   |
| V <sub>IL</sub> | Input LOW Voltage (Note 5.)<br>V <sub>CC</sub> = -4.5 to -5.5V<br>V <sub>CC</sub> = 5.0V (Note 4.)  | -1950<br>3050 | -1500<br>3500 | -1950<br>3050 | -1480<br>3520 | -1950<br>3050 | -1480<br>3520 | -1950<br>3050 | -1445<br>3555 | mV   |
| I <sub>IL</sub> | Input LOW Current (Note 5.)   | 0.5           |               | 0.5           |               | 0.5           |               | 0.3           |               | μA   |

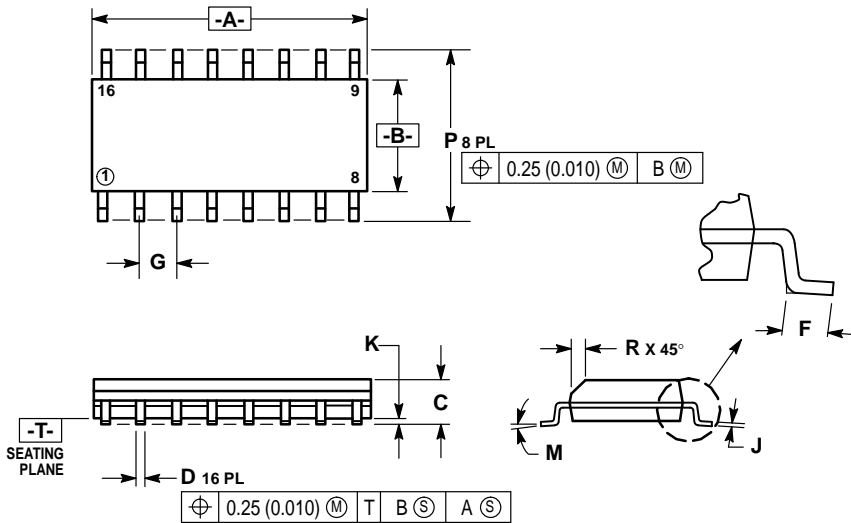
- 10SX circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts except where otherwise specified on the individual data sheets.
- Limits hold for V<sub>CC</sub> = 5.0V only. Parametric values will vary 1:1 with any variation of V<sub>CC</sub>.
- Parametric values for the Disable input only.

**AC CHARACTERISTICS** (V<sub>CCA</sub> = V<sub>CCE</sub> = 4.5V to 5.5V)

| Symbol                          | Characteristic                 | Min  | Typ | Max | Unit | Condition |
|---------------------------------|--------------------------------|------|-----|-----|------|-----------|
| BW <sub>min</sub>               | Lower -3dB Bandwidth           |      |     | 100 | MBPS |           |
| BW <sub>max</sub>               | Upper -3dB Bandwidth           | 1.25 |     |     | GBPS |           |
| t <sub>PWD</sub>                | Pulse Width Distortion         |      |     | 70  | ps   |           |
| t <sub>r</sub> , t <sub>f</sub> | Rise/Fall Times                | 150  | 250 | 650 | ps   | 20% - 80% |
| R <sub>AZ</sub>                 | Auto-Zero Output Resistance    | 200  | 325 | 450 | kΩ   |           |
| R <sub>F</sub>                  | Level Detect Filter Resistance | 14   | 25  | 41  | kΩ   |           |
| t <sub>LD</sub>                 | Level Detect Time Constant     | 0.5  |     | 4.0 | μs   |           |

OUTLINE DIMENSIONS

D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

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