P4C231
64Kx9 BIT SYNCHRONOUS SRAM with BURST MODE and SELF-TIMED WRITE

ADVANCE INFORMATION

FEATURES

- Pin-Compatible Upgrade from 32Kx9 Synchronous SRAM
- Built-in Burst Address Generator for i486 Burst Sequence
- Internal Write Pulse Generator
- Supports i486 Processor at 66MHz
- 5V ±10% Power Supply
- CMOS for Optimum Speed/Power
- TTL Compatible Inputs and Outputs
- Outputs Drive up to 85pF loads
- 44-pin PLCC Package

DESCRIPTION

The P4C231 is a 589,824-bit high-speed CMOS SRAM organized as 64x9 bits, with built-in input registers for fully synchronous operation. The built-in i486 Burst Sequence Address Generator and Self-Timed Write Operation make the P4C231 ideally suited for i486 secondary cache applications.

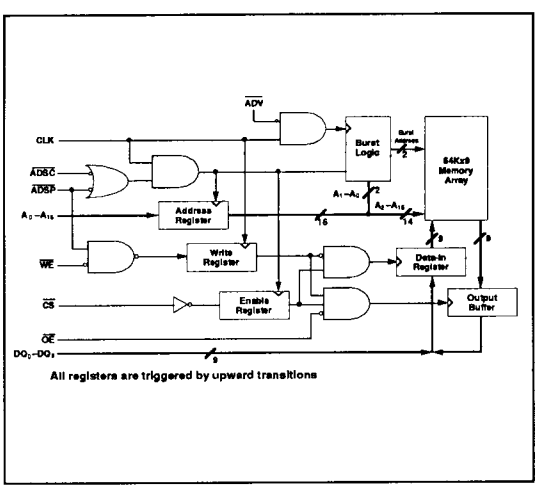
Clock-to-Output access times as fast as 11ns enable i486 processor operation at 66MHz with no wait states. Outputs drive up to 85pF loads without external buffering.

The P4C231 is pin-compatible with other 32Kx9 synchronous burst-mode SRAMs, permitting upgrade to 256KByte secondary cache with only four devices and no board space penalty. When deselected ($\overline{CS}$ is HIGH) power dissipation is less than 200mW.

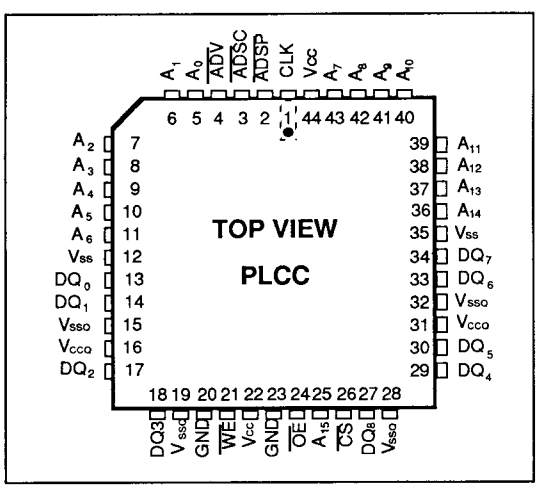
The P4C219 is manufactured using PACE III Technology and is available in a 44-pin PLCC surface-mount package providing excellent board-level density.

5

BLOCK DIAGRAM



PIN CONFIGURATION



i486 BURST SEQUENCE

	Case 1		Case 2		Case 3		Case 4		
	A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0	
Initial Cycle	0	0	0	1	1	0	1	1	From i486 processor
1st Burst Cycle	0	1	0	0	1	1	1	0	Internally generated
2nd Burst Cycle	1	0	1	1	0	0	0	1	Internally generated
3rd Burst Cycle	1	1	1	0	0	1	0	0	Internally generated

Note: The i486 burst sequence varies according to the initial address

BURST CONTROL

Address A_0 - A_{15} and Chip Select $\overline{CS}$ are clocked into registers only when $\overline{ADSP}$ = L (processor initiated) or $\overline{ADSC}$ = L (cache controller initiated) or both. To initiate transfer, $\overline{CS}$ must be clocked LOW. $\overline{ADSP}$ = L initiates only a read cycle, independent of $\overline{WE}$. $\overline{WE}$ = H is a read cycle, L is a write cycle. To enter burst mode, both $\overline{ADSP}$ and $\overline{ADSC}$ must be HIGH: $\overline{ADV}$ = L advances internal burst address, H suspends burst.

APPLICATION DIAGRAM: 256KByte Secondary Cache for i486