DESCRIPTION

The S5L9232 is a one-chip LSI for Compact Disc Players including a CMOS RF, Digital Servo, CD digital signal processor, Dynamic Bass Boost, Sigma-Delta D/A converter, and Shock-proof memory controller.

FEATURES

The S5L9232 has the following features:

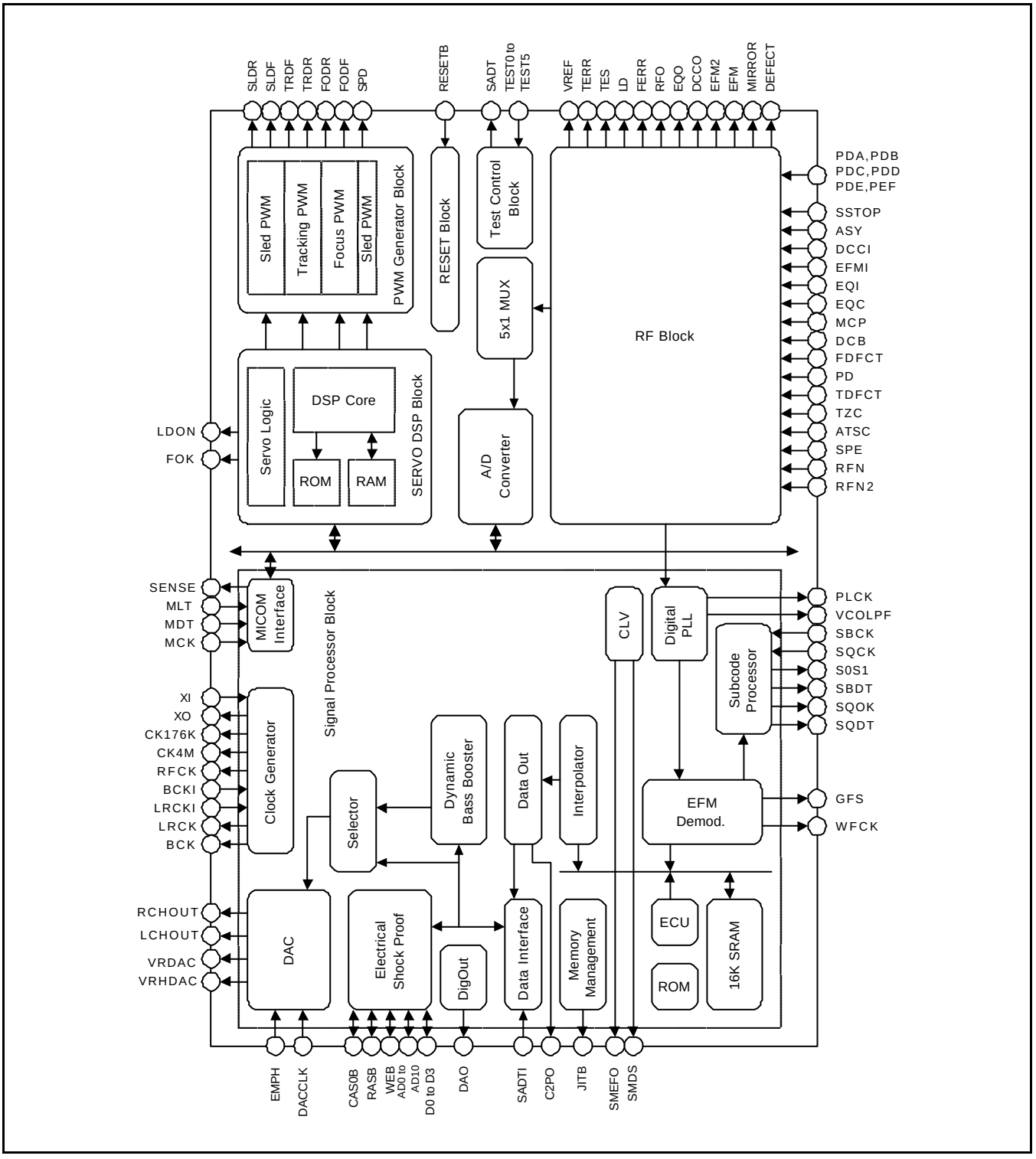
- CMOS RF block
  - Supports CD-RW (Re-Writable) Disc read
  - RF Summing Amplifier
  - Focus Error Amplifier
  - Tracking Error Amplifier
  - Automatic Focus/Tracking Balance Adjustment
  - Automatic Focus/Tracking Gain Adjustment
  - Defect Detection
  - Mirror Detection
  - Focus OK Detection
  - Automatic Laser Diode Power Control
  - EFM Comparator
  - Anti-Shock Function
  - RF AGC and EQ control
- Digital Servo block
  - Focus, Tracking, Sled, Spindle Servo
  - Focus/Tracking Offset Control
  - Focus/Tracking Input Gain Control
  - Focus Bias Control
  - Tracking Balance Control
  - Focus/Tracking Loop Gain Control
  - Built-in Digital Signal Processor
  - Drop Out and Shock countermeasure
  - Filter coefficients can be changed by MICRO-CONTROLLER
  - Built-in 8bit A/D and PWM output

- CDDSP, ESP, Audio DAC
  - — 1X and 2X play support
  - — C1: 2 error correction, C2: 2 error, 4 erasure correction
  - — Wide capture range playback mode
  - — EFM Data Demodulation
  - — Built-in Frame Sync Detection, Protection, and Insertion circuits
  - — Subcode Data Serial output
  - — Digital audio out
  - — Built-in ESP controller
  - — Built-in Sigma-Delta DAC & Audio Post-Filter
- Supports 2.4 — 3.6 Power Supply

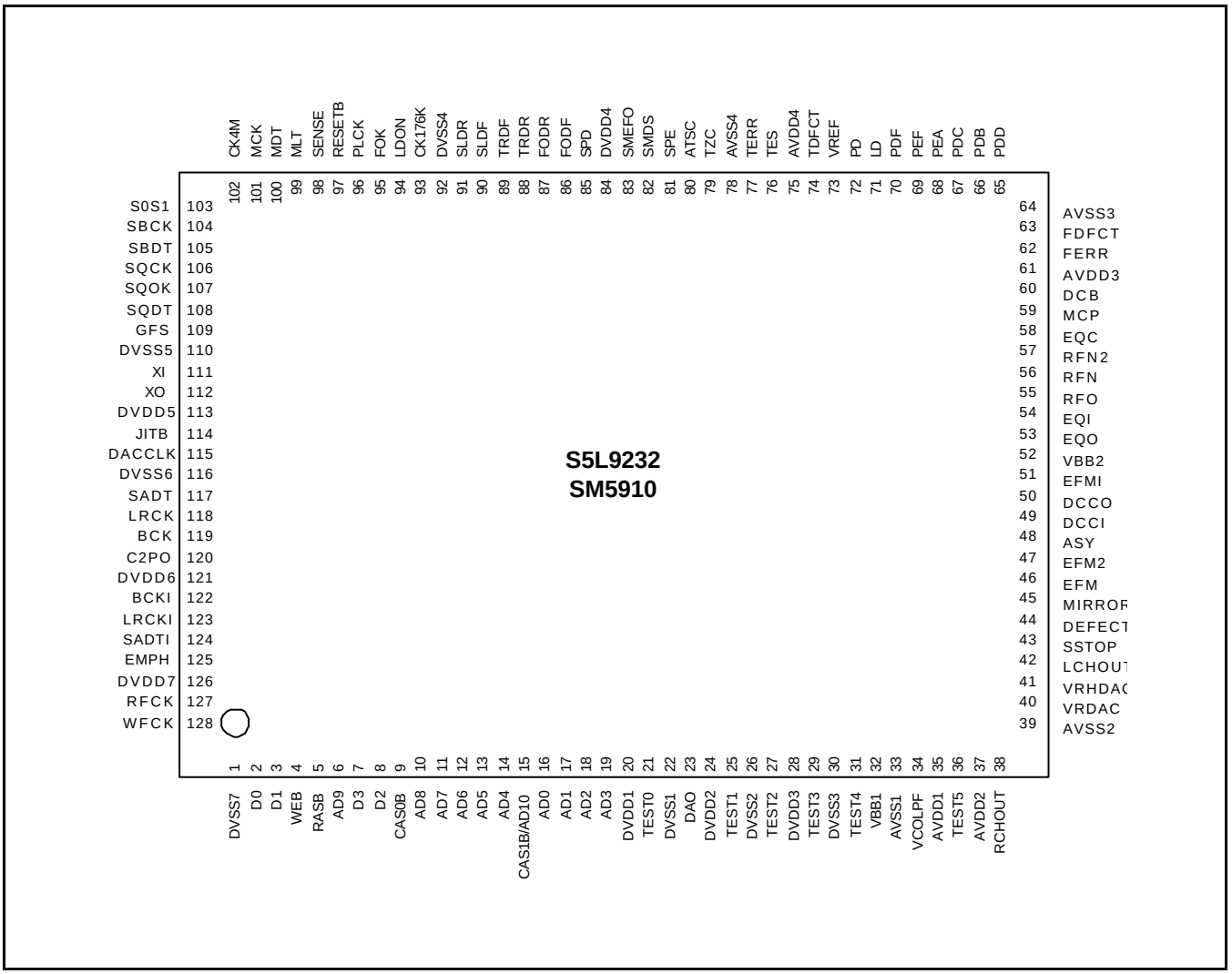
ORDERING INFORMATION

Device	Package	Operating Temperature
S5L9232	128-QFP-1420	-20 — 85°C

BLOCK DIAGRAM



PIN CONFIGURATION



SAMSUNG ELECTRONICS

S5L9232(SM5910) PIN DESCRIPTIONS (128QFP)

No	Pin Name	I/O	Descriptions	Note
1	DVSS7		Digital VSS (I/O PAD)	
2	D0	I/O	DRAM data Input/Output 0	
3	D1	I/O	DRAM data Input/Output 1	
4	WEB	I/O	DRAM Write Enable output. Active Low	
5	RASB	I/O	DRAM Row Address Selection output. Active Low	
6	AD9	I/O	DRAM Address output 9	
7	D3	I/O	DRAM data Input/Output 3	
8	D2	I/O	DRAM data Input/Output 2	
9	CAS0B	I/O	DRAM Column Address Selection output 0. Active Low	
10	AD8	I/O	DRAM Address output 8	
11	AD7	I/O	DRAM Address output 7	
12	AD6	I/O	DRAM Address output 6	
13	AD5	I/O	DRAM Address output 5	
14	AD4	I/O	DRAM Address output 4	
15	CAS1B /AD10	I/O	DRAM Column Address Selection output 1. Active Low	
16	AD0	I/O	DRAM Address output 0	
17	AD1	I/O	DRAM Address output 1	
18	AD2	I/O	DRAM Address output 2	
19	AD3	I/O	DRAM Address output 3	
20	DVDD1		Digital VDD (SERVO,CDDSP,ESP)	
21	TEST0	I	Test mode selection 0 (for ESP & DBB). Active High	
22	DVSS1		Digital VSS (SERVO,CDDSP,ESP)	
23	DAO	O	Digital audio output	
24	DVDD2		Digital VDD (PLL)	
25	TEST1	I	Test mode selection 1. Active High	
26	DVSS2		Digital VSS (PLL)	
27	TEST2	I	Test mode selection 2. Active High	
28	DVDD3		Digital VDD (Sigma-Delta DAC,ADC)	
29	TEST3	I	Test mode selection 3. Active High	
30	DVSS3		Digital VSS (Sigma-Delta DAC,ADC)	
31	TEST4	I	Test mode selection 4. Active High	
32	VBB1		VSS for Bulk Bias (PLL)	

S5L9232(SM5910) PIN DESCRIPTIONS (128QFP) (Continued)

No	Pin Name	I/O	Descriptions	Note
33	AVSS1		Analog VSS (PLL)	
34	VCOLPF	O	Pump out for VCO	
35	AVDD1		Analog VDD (PLL)	
36	TEST5	I	Test mode selection 5. Active High	
37	AVDD2		Analog VDD (Sigma-Delta DAC)	
38	RCHOUT	O	Right-channel audio output	
39	AVSS2		Analog VSS (Sigma-Delta DAC)	
40	VRDAC	O	Voltage reference for Sigma-Delta DAC	
41	VRHDAC	O	Half voltage reference for Sigma-Delta DAC	
42	LCHOUT	O	Left-channel audio output	
43	SSTOP	I	SSTOP input (internal 47kΩ pull-up)	
44	DEFECT	O	Defect Output	
45	MIRROR	O	Mirror output	
46	EFM	O	EFM output	
47	EFM2	O	EFM output2 (through resistor)	
48	ASY	I	LPF connection for EFM slicer	
49	DCCI	I	Defect bottom hold capacitor	
50	DCCO	O	Defect bottom hold output	
51	EFMI	I	EFM input	
52	VBB2		VSS for Bulk Bias (ADC, Sigma-Delta DAC)	
53	EQO	O	AGC-EQ output	
54	EQI	I	AGC-EQ input coupling capacitor	
55	RFO	O	RF summing output	
56	RFN	I	RF summing AMP (-) input	
57	RFN2	I	RF summing AMP (-) input for 2X Filter	
58	EQC	I	AGC-EQ capacitor	
59	MCP	I	Mirror hold capacitor	
60	DCB	I	Defect bottom hold capacitor	
61	AVDD3		Analog VDD (RF)	
62	FERR	O	Focus error output	
63	FDFCT	O	Focus error LPF	
64	AVSS3		Analog VSS (RF)	
65	PDD	I	RF I-V AMP D input from pick-up	

S5L9232(SM5910) PIN DESCRIPTIONS (128QFP) (Continued)

No	Pin Name	I/O	Descriptions	Note
66	PDB	I	RF I-V AMP B input from pick-up	
67	PDC	I	RF I-V AMP C input from pick-up	
68	PDA	I	RF I-V AMP A input from pick-up	
69	PDE	I	E I-V AMP input from pick-up	
70	PDF	I	F I-V AMP input from pick-up	
71	LD	O	APC output	
72	PD	I	APC input	
73	VREF	O	AVDD/2 DC voltage output	
74	TDFCT	O	Tracking error LPF	
75	AVDD4		Analog VDD (ADC)	
76	TES	O	Tracking Summing output	
77	TERR	O	Tracking error output	
78	AVSS4		Analog VSS (ADC)	
79	TZC	I	Tracking zero cross input	
80	ATSC	I	Anti-shock input from BPF	
81	SPE	I	Spindle error input	
82	SMDS	O	Spindle motor velocity control in Phase Mode	
83	SMEFO	O	CLV LPF connection	
84	DVDD4		Digital VDD (SERVO,CDDSP,ESP)	
85	SPD	O	Spindle servo output. 3-state	
86	FODF	O	Focus servo Forward output	
87	FODR	O	Focus servo Reverse output	
88	TRDR	O	Tracking servo Reverse output	
89	TRDF	O	Tracking servo Forward output	
90	SLDF	O	Sled servo Forward output	
91	SLDR	O	Sled servo Reverse output	
92	DVSS4		Digital VSS (SERVO,CDDSP,ESP)	
93	CK176K	O	176.4kHz(16.9344MHz/96) output (X'tal divided))	
94	LDON	O	LDON Status output. Active High	
95	FOK	O	Focus OK output. Active High	
96	PLCK	O	4.3218MHz output(1X) 8.6436MHz output (2X). (VCO divided)	
97	RESETB	I	MICRO-CONTROLLER reset. Active Low	

S5L9232(SM5910) PIN DESCRIPTIONS (128QFP) (Continued)

No	Pin Name	I/O	Descriptions	Note
98	SENSE	O	Internal status monitor.	
99	MLT	I	MICRO-CONTROLLER serial data latching signal input. Active Low	
100	MDT	I	MICRO-CONTROLLER data input	
101	MCK	I	MICRO-CONTROLLER clock signal input	
102	CK4M	O	4.2336MHz/16.9344MHz output(X'tal divided)	
103	SOS1	O	Subcode SYNC S0+S1 output	
104	SBCK	I	Subcode data bit clock input	
105	SBDT	O	Subcode data serial output	
106	SQCK	I	Subcode-Q data bit clock	
107	SQOK	O	Subcode-Q CRC check result signal	
108	SQDT	O	Subcode-Q data serial output	
109	GFS	O	Lock status output of Frame Sync	
110	DVSS5		Digital VSS (I/O PAD)	
111	XI	I	System clock input (16.9344MHz)	
112	XO	O	System clock output	
113	DVDD5		Digital VDD (I/O PAD)	
114	JITB	O	Jitter margin flag. Active Low	
115	DACCLK	I	Sigma-Delta DAC system clock input	
116	DVSS6		Digital VSS (SERVO,CDDSP,ESP)	
117	SADT	O	Serial audio data output	
118	LRCK	O	Channel clock output	
119	BCK	O	Serial audio data bit clock output	
120	C2PO	O	C2 pointer for serial audio data	
121	DVDD6		Digital VDD (SERVO,CDDSP,ESP)	
122	BCKI	I	Serial data bit clock input	
123	LRCKI	I	Channel clock input	
124	SADTI	I	Serial audio data input	
125	EMPH	I	Emphasis/non-emphasis output. H: emphasis	
126	DVDD7		Digital VDD (I/O PAD)	
127	RFCK	O	X'tal controlled read frame clock	
128	WFCK	O	VCO controlled write frame clock	

ABSOLUTE MAXIMUM RATINGS

No	Item	Symbol	Spec.	Unit
1	Supply Voltage	V_{DD}	-0.15 — 3.8	V
2	Input Voltage	V_I	-0.15 to $V_{DD+0.15}$	V
3	Output Voltage	V_O	-0.15 — 3.8	V
4	Operating Temperature	T_{OPR}	-20 — 85	°C
5	Storage Temperature	T_{STG}	-40 — 125	°C
6	Power Dissipation	P_D	500	mW

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	2.4	3.0	3.6	V
Operating Temp.	Topr	-20	25	85	°C

ELECTRICAL CHARACTERISTICS

LOGIC' S

DC Characteristics:

(V_{DD} = 2.5, VSS = 0V, Ta = 25°C)

No	Item	Symbol	Cond.	Min	Typ	Max	Unit	Misc.
1	'H' Input Voltage1	$V_{IH(1)}$		1.7	-	-	V	note 1
2	'L' Input Voltage1	$V_{IL(1)}$		-	-	0.7	V	
3	'H' Input Voltage2	$V_{IH(2)}$		-	-	1.9	V	note 2
4	'L' Input Voltage2	$V_{IL(2)}$		0.6	-	-	V	
5	'H' Output Voltage1	$V_{OH(1)}$	I_{OH} = -2mA	1.9	-	-	V	note 3
6	'L' Output Voltage1	$V_{OL(1)}$	I_{OL} = 2mA	-	-	0.5	V	
7	Three State Output Leak Current	$I_{O(LKG)}$	V_O = 0— V_{DD}	-10	-	10	uA	note 4
8	Current Consumption	I_{DD}	note 5		35		mA	
9	Low Level Input Current for with Pull-up	I_{IL}	V_{IN} = V_{SS}		33		uA	note6

NOTES:

1. Related pins: CMOS interface.
2. Related pins: CMOS Schmitt trigger interface, (MLT, MCK, MDT, RESETB pins).
3. Related pins: All output pins except #112(XO).
   Related pins: SMEFO (#83), SMDS (#82), SENSE (#98), and SPD (#85)
   All V_{DD}= 2.5, All V_{SS}= 0V, XI(#111) = 16.9344MHz
6. Related pins : All Bi-directional Pins. V_{DD}= 3.3 V condition.

<Pin Summary>

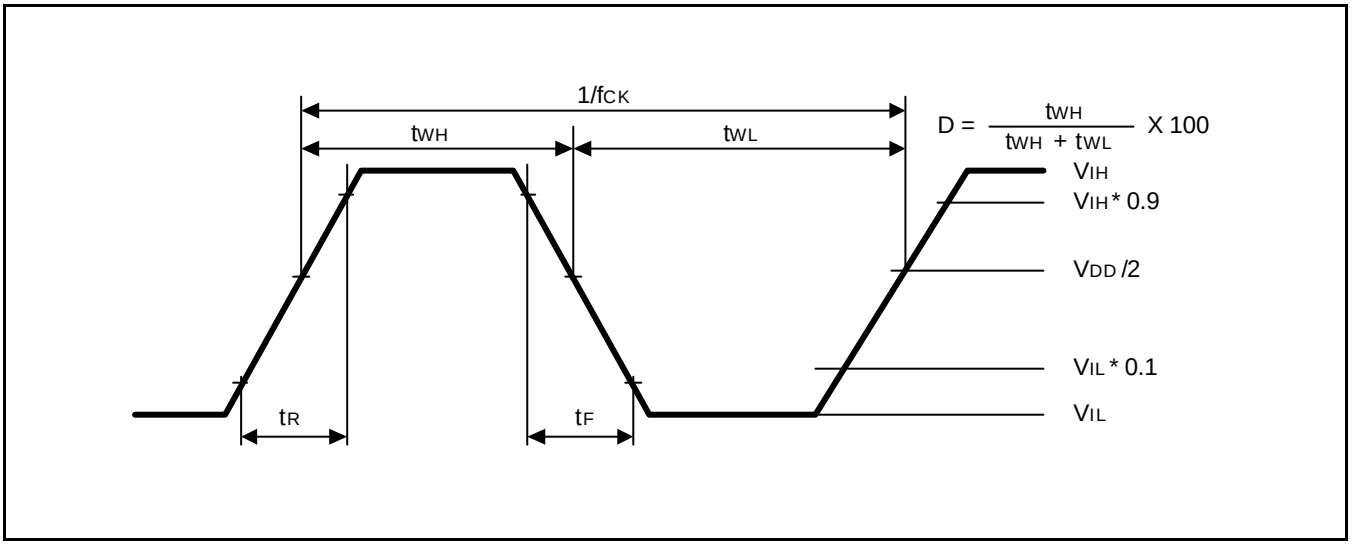
1	Pin Function	Clock Input/Output Pin
	Pin Name	XI/XO
2	Pin Function	Schmitt Input Pins
	Pin Name	RESETB, MLT, MDT, MCK
3	Pin Function	I/O Pins (Tri-state bi-directional buffer with Pull-up)
	Pin Name	D0, D1, D2, D3, WEB, RASB, CAS0B, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, AD8, AD9, AD10
4	Pin Function	Input Pins (Digital)
	Pin Name	TEST0, TEST1, TEST2, TEST3, TEST4, SBCK, SQCK, DACCLK, BCKI, LRCKI, SADTI, EMPH
5	Pin Function	Input Pins (Analog)
	Pin Name	TEST5, SSTOP, ASY, DCCI, EFMI, EQI, RFN, RFN2, EQC, MPC, DCB, FDFCT, PDD, PDB, PDC, PDA, PDE, PDF, PD, TDFCT, TZC, ATSC, SPE
6	Pin Function	Output Pins (Digital)
	Pin Name	DAO, FODF, FODR, TRDR, TRDF, SLDF, SLDR, CK176K, LDON, FOK, PLCK, CK4M, S0S1, SBDT, SQOK, SQDT, GFS, JITB, SADT, LRCK, BCK, C2PO, RFCK, WFCK
7	Pin Function	Output Pins (Tri-state)
	Pin Name	SMDS, SMEFO, SPD, SENSE
8	Pin Function	Output Pins (Analog)
	Pin Name	VCOLPF, RCHOUT, VRDAC, VRHDAC, LCHOUT, DEFECT, MIRROR, EFM, EFM2, DCCO, EQO, RFO, FERR, LD, VREF, TES, TERR

AC Characteristics:

When a pulse is input into XI pin:

(V_{DD} = 2.5V, V_{SS} = 0V, Ta = 25°C)

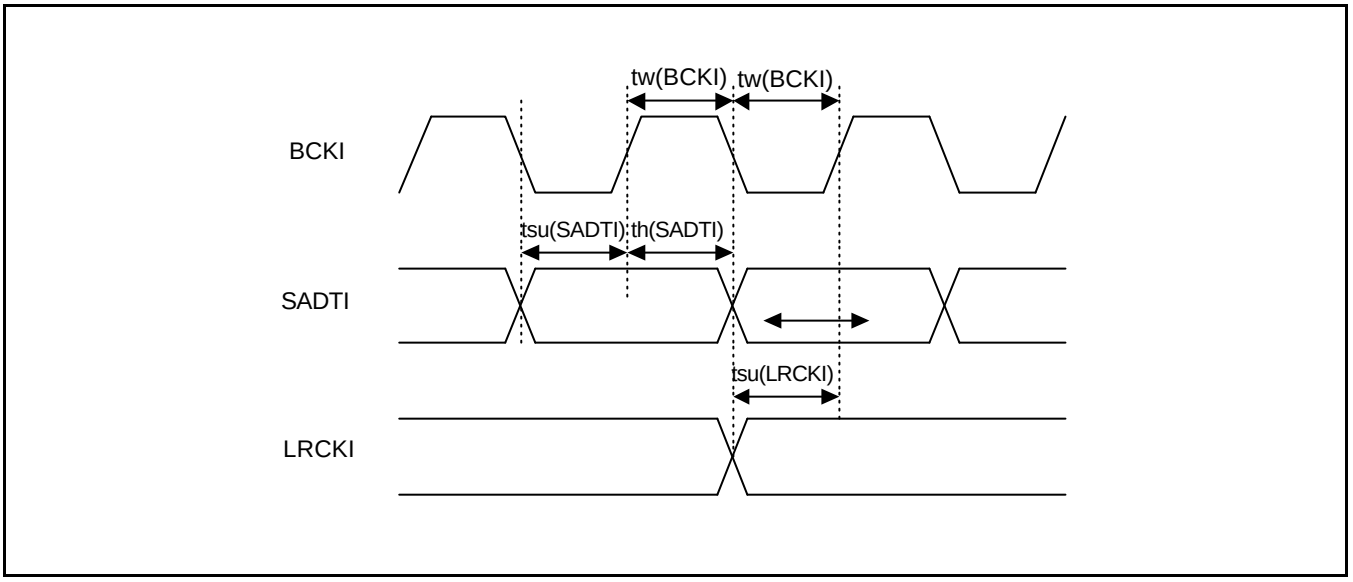
No	Item	Symbol	Min	Typ	Max	Unit
1	Clock Frequency	f_{CK}	-	16.9344	-	MHz
2	Clock Duty	D	-	50	-	%
3	Input 'H' Level	V_{IH}	V_{DD}-0.7	-	-	V
4	Input 'L' Level	V_{IL}	-	-	0.7	V
5	Rising & Falling Time	t_R, t_F	-	-	8	ns



BCKI, LRCKI, and SADTI (Same as BCK, LRCK, SADT Output) :

(V_{DD}= 2.5V ± 5%, V_{SS}= 0V, Ta = -20 — 85°C)

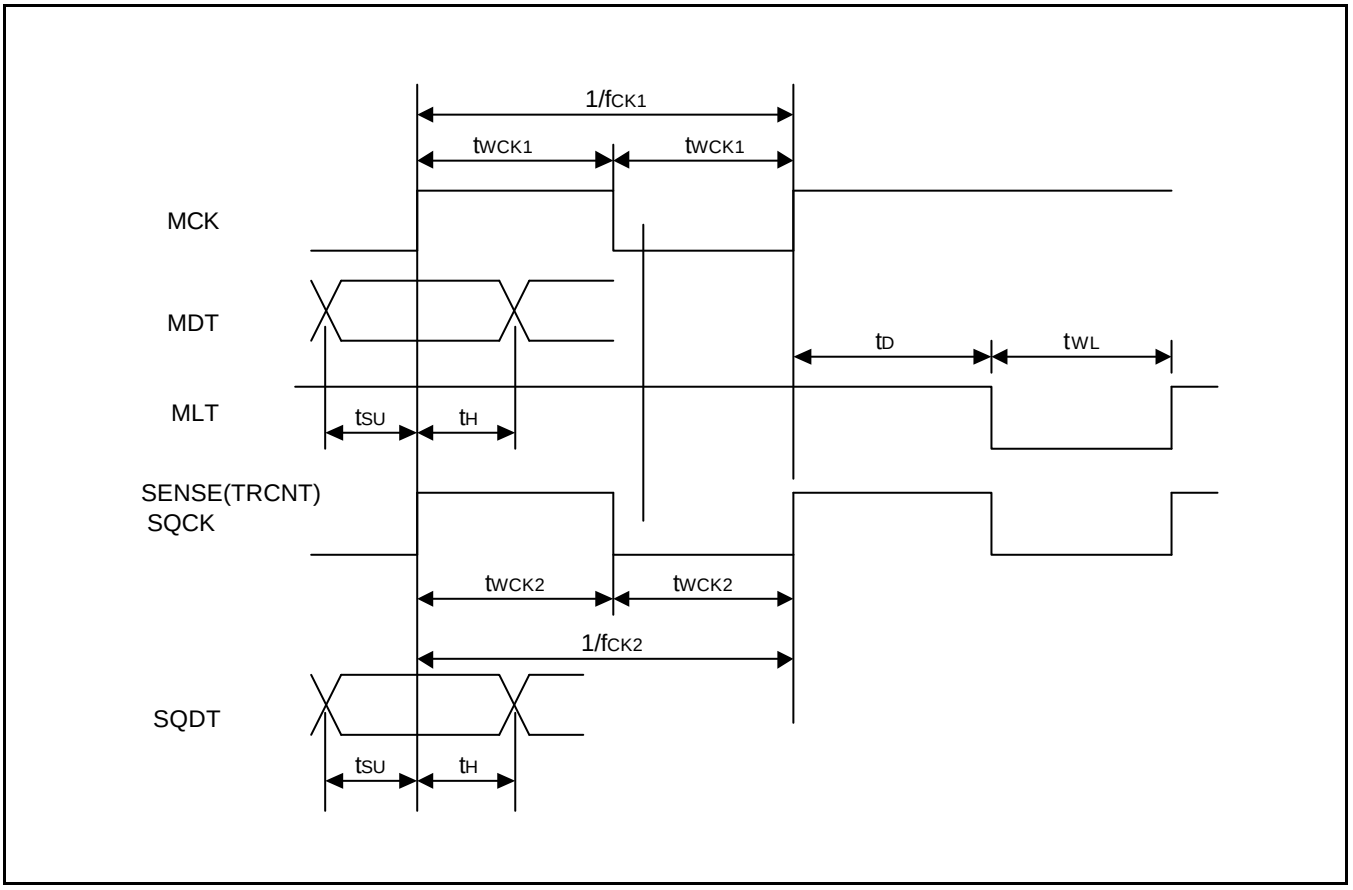
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCKI pulse width	tw			1/(96fs)		ns
SADTI setup time	tsu		20			ns
SADTI hold time	th		20			ns
LRCKI setup time	tsu		20			ns



MCK, MDT, MLT

(V_{DD} = 2.5, VSS = 0V, Ta = 25°C)

No	Item	Symbol	Min	Typ	Max	Unit
1	Clock Frequency	f_{CK1}	-	-	8	MHz
2	Clock Pulse Width	t_{WCK1}	500	-	-	ns
3	Setup Time	t_{SU}	300	-	-	ns
4	Hold Time	t_H	300	-	-	ns
5	Delay Time	t_D	300	-	-	ns
6	Latch Pulse Width	t_{WL}	500	-	-	ns
7	SENSE (TRCNT), SQCK Frequency	f_{CK2}	-	-	1	MHz
8	SENSE (TRCNT), SQCK Pulse Width	t_{WCK2}	500	-	-	ns



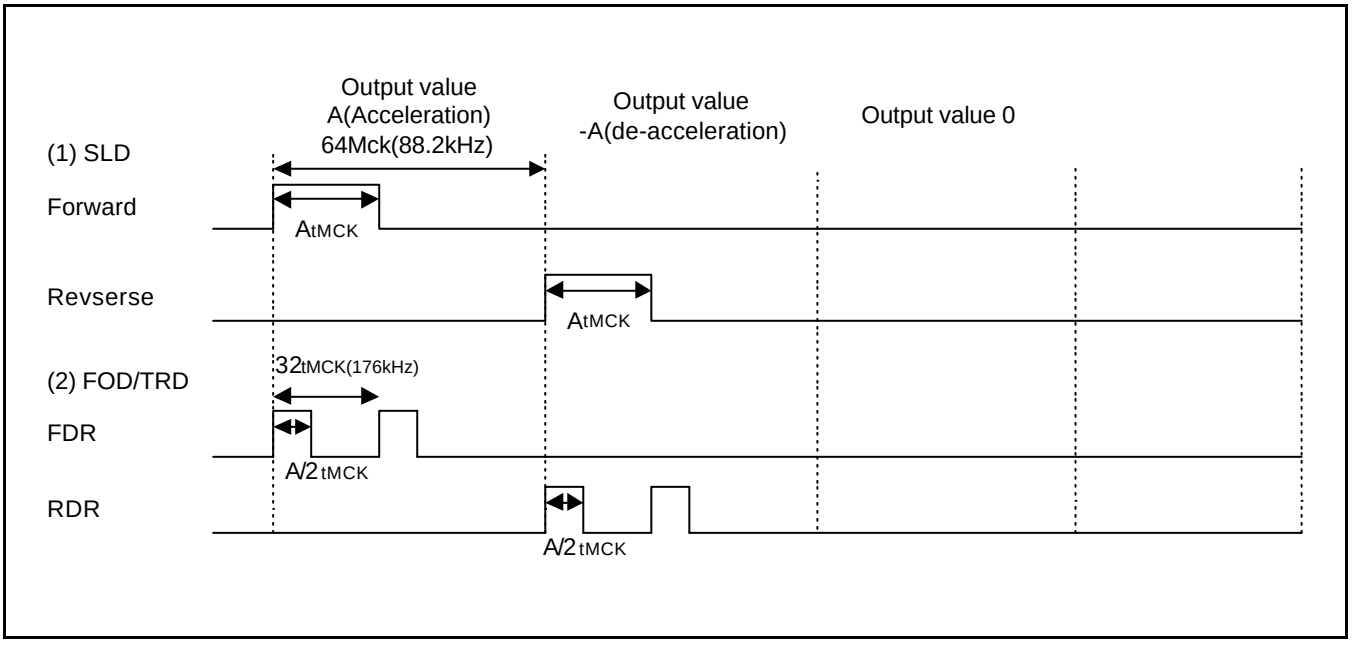
SIGMA-DELTA AUDIO DAC

(V_{DDD},V_{DDA} = 2.5V, Temp=25°C, Fs = 44.1kHz, Signal Frequency=20 — 20kHz, Cload of AoutL, AoutR = 10pF)

Parameter	Min	Typ	Max	Units
Resolution		16		bits
SNR[1]	92			dB
THD[2]		0.007		%
SND(THD+Noise)[3]		82		dB
Dynamic Range[4]	92			dB
Reference Voltage Output		$0.5 \times V_{DDA}$		V
Frequency Response		± 0.1	± 0.5	dB
Analog Output				
Voltage Range		$0.75 \times V_{DDA}$		Vpp
Load Impedance	10K			Ω

NOTES:
1. 1kHz 0dB Sine wave Input, EIAJ
2. 1kHz -3dB Sine wave Input
3. 1kHz 0dB Sine wave Input, (Not EIAJ)
4. 1kHz -60dB Sine wave Input, and then measured data + 60dB

PWM OUTPUT



FUNCTIONAL DESCRIPTIONS

MICRO-CONTROLLER INTERFACE

Data inputs from micro-controller are received through MDAT, and transmitted by MCK. This signal is stored in the Control Register by MLT. The Timing diagram for this process is shown in Figure 1. Each command is carried out by receiving data and commands (MSB first) from micro-controller.

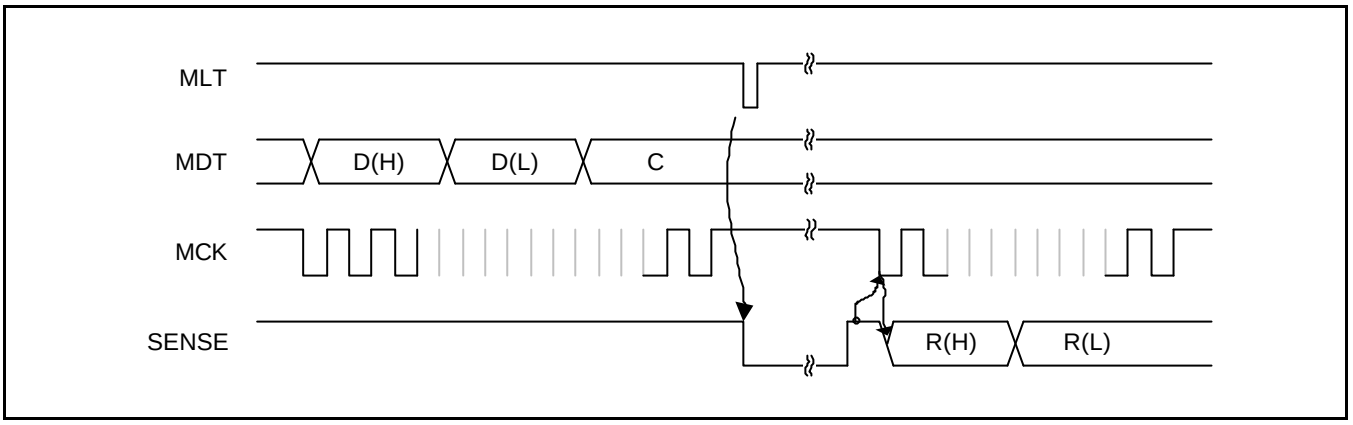


Figure 1. Micro-controller Interface Timing Chart

For CD-DSP, the command and data length is 8 bits respectively. In the case of the Servo, the command length is fixed at 8 bits, but the data length is varied from 0 to16 bits. When Data is 16 bits and command is 8 bits, the input is made starting with the MSB in the following order: D(H) = D15 — D8, D(L) = D7 — D0, and C = C7 — C0. In the case of a command with no data, you only need to input the command byte. When data input is finished, a pulse at MLT is generated to indicate that the command transmission is finished. From then on, command is decoded and carried out. The SENSE output shows READY (/BUSY) status at default. In other words, it is "L" when it receives a command, and "H" when the command is completed. In certain commands, SENSE output has a meaning other than that of Ready. For example, it can show the "on/off" information of the limit switch or the presence of a disc.

The detailed input timing of S5L9232 is shown in Figure 2. Micro-controller sends MDT to MCK falling edge, in the order of MSB, Data, and Command. S5L9232 latches the data at MCK's rising edge. Micro-controller no longer sends MCK when the transmission of all MDT is finished. At this time, MLT becomes "L" to indicate that the transmission of command and data from Micro-controller to S5L9232 is complete.

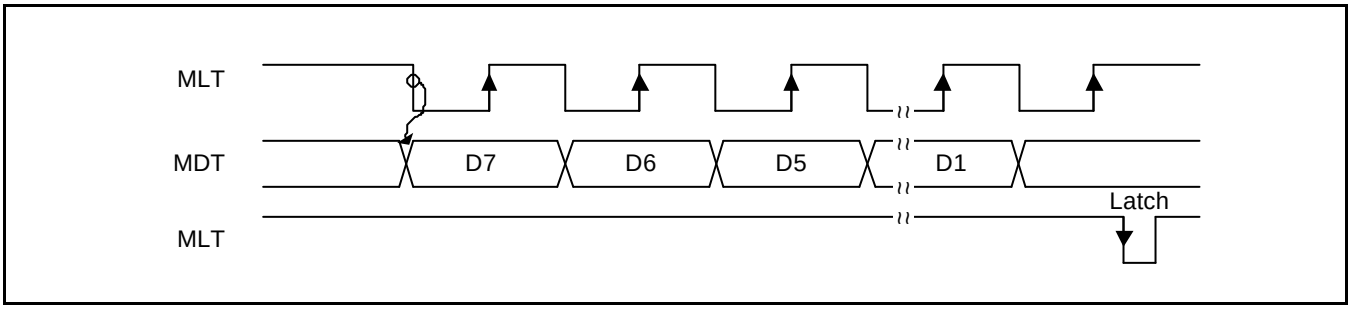


Figure 2. Micro-controller to S5L9232 Input Timing

The timing for sending data to Micro-controller is shown in Figure 3. In such a case the Digital Servo Signal Processor (DSSP) stores the data to be sent to Micro-controller after command has been carried out, in the output buffer. At the same time, it makes the SENSE output "H" to indicate that the DSSP's command processing routine is finished. If Micro-controller needs to read the response data, only MCK is sent to S5L9232. S5L9232 then sends the output serially through SENSE to Micro-controller, at MCK's falling edge. Since SENSE's Ssel (Serial Data Select Signal) is "1", the data in the output buffer should be output. The output to SENSE is carried out in units of byte, and in the order of R(H) = R15 — R8 and R(L) = R7 — R0, starting with MSB.

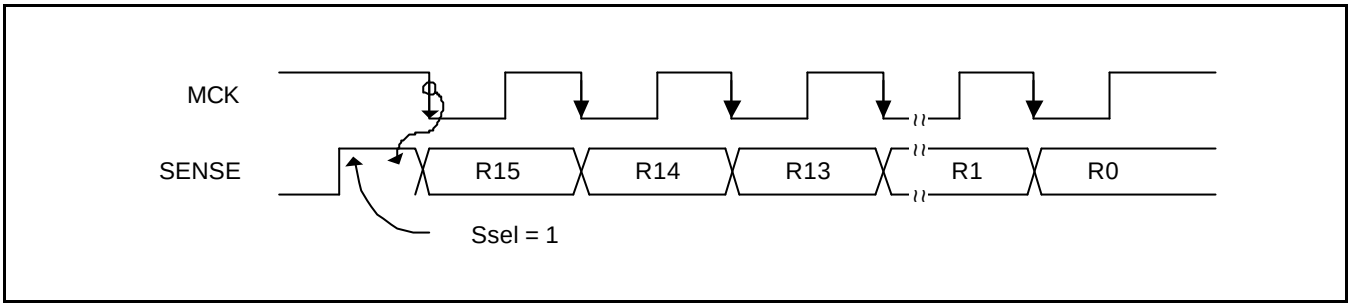


Figure 3. S5L9232 to Micro-controller Output Timing

S5L9232 generates one SENSE signal that makes the CD-DSP and Servo into a single chip and goes through MUX to Micro-controller. Hence, Micro-controller can use SENSE as a direct input signal.
As shown in Table 1 and Table 2, Micro-controller command can be divided into Micro-controller command for Digital Servo (00 — 5Fh), and Micro-controller command for CD-DSP (60h — FFh)

MICRO-CONTROLLER COMMAND SET

Table 1. Servo part MICRO-CONTROLLER command set

Addr.	CMD	Data								Sense	INIT. Value
		D15	D14	D13	D12	D11	D10	D9	D8		
		D7	D6	D5	D4	D3	D2	D1	D0		
00	STPcmd									/BUSY	-
						LDX	IDLE	ABRT	STOP		
01	DDTcmd									*SERIAL DATA	-
		AUTO	*UPDN*	FIGA	FBAL	RPT	FSP2	FSP1	FSP0		
02	FONcmd									/BUSY	-
		LYRX	Fmthd	*FOPI*	FSPC	PIL3	PIL2	PIL1	PIL0		
03	TONcmd									/BUSY	-
			SLSV		TOLB	MTLB	SFOG	STRG			
04	SLDcmd									/BUSY	-
							SPLY	SMOV	HOMEIN		
05	JMPcmd	DIR	JPM1	JPM0	JIT2	JIT1	JIT0	JPD9	JPD8	/BUSY	-
		JPD7	JPD6	JPD5	JPD4	JPD3	JPD2	JPD1	JPD0		
07	EMEcmd									/BUSY	004Fh
		TEST	SLST		upFv	dsAS	ASFO	ASTR			
08	HDWcmd									/BUSY	0008h
			SSTOP	LPDS	SPHOLD	PCUP		SLbrk	0		
09	INIcmd									/BUSY	0041h
			JPCK			BJJM	BTS	enJaP	Slref		
0B	SPDcmd									/BUSY	0000h
									SPD		
11	OFAcmd									/BUSY	-
								LDoff	FTS		
12	FBAcmd									/BUSY	-
13	TBAcmd									/BUSY	-
								RPTB	TIGA		
14	FGAcmd									/BUSY	-
15	TGAcmd									/BUSY	-

Table 1. Servo part MICRO-CONTROLLER command set (Continued)

Addr.	CMD	Data								Sense	INIT. Value
		D15	D14	D13	D12	D11	D10	D9	D8		
		D7	D6	D5	D4	D3	D2	D1	D0		
17	RFSNS cmd									**SIGNAL MONITOR	0000h
							SEN2	SEN1	SEN0		
18	SQDTc md									/BUSY	0000h
								SQDT 1	SQDT0		
19	SNScm d						SNS2	SNS1	SNS0	**SIGNAL MONITOR	0000h
								Ssel			
1A	FLGcm d	stp	Fptmg	SSVon	HOME	itvj	TSV	SSV	enTJn	*SERIAL DATA	2021h
		DFCTe d	ATSCed	Tbmthd			FSend		enLOCK		
1B	SNSCc md	RWB		*NORM*	FTLK				BANK	/BUSY	-
		MOD7	MOD6	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0		
1C	DPRWc md	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	*SERIAL DATA	-
		DD3	DD2	DD1	DD0	ST6	DPS2	DPS1	DPS0		
1D	FTSTc md									/BUSY	-
					WTF				WFF		
1E	RamRc md	NEXT	0	0	BANK	0	0	0	0	*SERIAL DATA	-
		RAM7	RAM6	RAM5	RAM4	RAM3	RAM2	RAM1	RAM0		
1F	RamWc md	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	/BUSY	-
		RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0		
20	TTKcm d	LK15	LK14	LK13	LK12	LK11	LK10	LK9	LK8	/BUSY	-
		LK7	LK6	LK5	LK4	LK3	LK2	LK1	LK0		

Table 1. Servo part MICRO-CONTROLLER command set (Continued)

Addr.	CMD	Data								Sense	INIT. Value
		D15	D14	D13	D12	D11	D10	D9	D8		
		D7	D6	D5	D4	D3	D2	D1	D0		
21	FTGcmd									/BUSY	-
						UP	Tchg	DWN	Fchg		
58	RFMRcmd								EQS	/BUSY	0000h
		MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0		
59	ADCKcmd									/BUSY	0000h
		TZCSEL	APCGAIN						ADCK		
5A	RFBALcmd									/BUSY	0010h
		STSL1	STSL0		TBAL4	TBAL3	TBAL2	TBAL1	TBAL0		
5B	RFSTcmd									/BUSY	0000h
		VISEL	SF2	RFB1	RFB0	LDON	PSTZCB	EQL1	EQL0		
5C	EFMScmd									/BUSY	0000h
		MODEC	SPEAK	ONOFF	DONOFF		FOKS	DFCTS	MIRRS		
5D	RFRWcmd									/BUSY	0000h
		RW3	RW2	RW1	RW0		RWT2	RWT1	RWT0		
5E	RFIGcmd									/BUSY	0000h
			FG2	FG1	FG0		TG2	TG1	TG0		
5F	TPWMcmd									/BUSY	-
		PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0		

*SERIAL DATA : User can read the response of the command after SENSE goes high which means ready.

**SIGNAL MONITOR : SENSE output can be used in order to monitor other signals such as TLK, ATSC, TZC, and so on.

Table 2. CD-DSP/ESP part Micro-Controller command set (Micro-Controller Write Command)

Addr.	CMD	Data								Sense	INIT. Value
		D7	D6	D5	D4	D3	D2	D1	D0		
60	DPLLCTL 1	WIDE	-	PGAIN	DLFGAIN	ROM1	COAT	-	RETREF	Z	00h
61	DPLLCTL 2	REF98[1:0]		REF[1:0]		MAXTGAIN[1:0]		CAPRANGE[1:0]		Z	F0h
62	DPLLCTL 3		DIVS1[1:0]		DIVP1[5:0]					Z	56h
64	DPLLCTL 5				MITEST[7:0]					Z	00h
65	DPLLCTL 6	CMDSPLT	PONLY		MRANGE[1:0]	FSREG	PLLTEST	PLLPWRDN	-	Z	00h
70	DBB	-	-	-	-	TST1	-	MAX	DBB	Z	00h
80	ESPMS	MSWREN	MSWACL	MSRDEN	MSRACL	MSDCN2	MSDCN1	WAQV	MSON	Z	00h
83	AUDCNTL1	ATT	MUTE	SOFT	NS	CMP12	-	-	-	Z	00h
84	ATTLEVEL	K7	K6	K5	K4	K3	K2	K1	K0	Z	40h
85	OPTIONSET1	RAMS1	RAMS2	-	-	COMPFB	COMP6B	COMP5B	COMP4B	Z	04h
86	DAUDIF	CP1	CP2	LBIT	DIT	-	-	-	-	Z	00h
A0	FUNCNTL	CDROM	ESPEN	DEEM	ERAOFF	C1PNT	DBBON	EMPHSEL	JITM	Z	20h
A1	FSYNCNTL	FSEL[1:0]		WSEL[1:0]		FSMD[1:0]		-	-	LKFS	00h
A2	MODECNTL1	PWRDNL	ESPDN	SVOPDL		CLVEMERG	EMERGP	NCLV	CRCQ	Z	e1h
A3	MODECNTL2	EFMSEL	-	-	-	-	-	YFLAG	JTFRV	Z	00h
A8	OUTCNTL1	-	PLCK MUTE		WFCK MUTE	-	DAO MUTE	SBDT MUTE	C4M MUTE	Z	00h
A9	OUTCNTL2	-	MNTSEL[2:0]			-	-	SC1	SC0	Z	00h
AA	OUTCNTL3	-	-	-	-		FREQS[3:0]			Z	00h

Table 2. CD-DSP/ESP part Micro-Controller command set (Micro-Controller Write Command) (Continued)

Addr.	CMD	Data								Sense	INIT. Value
		D7	D6	D5	D4	D3	D2	D1	D0		
AB	AUDCNTL2	AMUTE	ZCMT	-	ATTN	FLAG2V	-	DATXMUTE	DACMUTE	S0S1	81h
B0	TEST1	DION	-		TMODE[5:0]					Z	00h
C0	DATTN	-	-		DATTN[5:0]					Z	00h
C1	DACCNTL	ZDENL	-		FSEMPH[1:0]	DACCLK	-	BISTONP	TSEL	Z	00h
E0	CLVGAIN	-	WBN	WPN	RFCKSEL	-	WB	WP	GAIN	Z	07h
E1	CLVMODE	UNLOCK		CLVIDLE	PCEN	CM3	CM2	CM1	CM0	/CLVST	00h
E2	CLVCNTL1	STRIO	SMM	PME	SME	PCKSEL[1:0]			PGAIN[1:0]	Z	02h
E3	CLVCNTL2	LC	PML	SML[1:0]		POS	SGAIN[2:0]			Z	02h
E4	CLVCNTL3				POFFSET[7:0]					Z	00h
E5	CLVCNTL4	SPLUS	SDD	PHASEDIV[1:0]		SMOFFSET[3:0]				Z	00h
E6	CLVCNTL5				SOFFSET[7:0]					Z	00h
F0	PLAYCNTL	-	-	-	-	-	DASPEED	DS1	DS0	Z	00h

Table 2. CD-DSP/ESP part Micro-Controller command set (Micro-Controller Write Command) (Continued)

Addr.	CMD	Data												Sense
87	SUBQDAT	QAD3	QAD2	QAD1	QAD0	QD7	QD6	QD5	QD4	QD3	QD2	QD1	QD0	Z

Table 3. CD-DSP/ESP part Micro-Controller command set (Micro-Controller Read Command)

Addr.	CMD	D7	D6	D5	D4	D3	D2	D1	D0
90	ESPMEMST1	FLAG6	MSOVF	BOVF		DCOMP	MSWIH	MRSIH	
91	ESPMEMST2	MSEMP	OVFL	ENCOD	DECOD	QRDY			
Addr.	**CMD**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
92	MEMRESIDU	AM21	AM20	AM19	AM18	AM17	AM16	AM15	AM14
		AM13	AM12	AM11	AM10	AM09	AM08	AM07	AM06

DIGITAL SERVO MICRO-CONTROLLER COMMAND DESCRIPTIONS

This digital servo signal processor (DSSP) is a CD-only optical pickup system servo command. This LSI was developed to simplify the hardware through automatic control and digital filter. However, manual control commands are also included to be comprehensive, and those could make somewhat complex command table. It was simplified as much as possible through the use of defaults.

Basically, SENSE = "L", when S5L9232 receives commands from the MICRO-CONTROLLER, and SENSE = "H" when the command job ends. The SENSE output is usually assigned /BUSY, but some commands assign different definitions to SENSE. In particular, when there is no SENSE related comments, S5L9232 recognizes SENSE = /BUSY.

The commands can be divided largely into two types, executable commands and non-executable commands (setting/reference commands). The former types are the action commands that directly execute servo-related operations and the latter are filter coefficient setting/reference commands, initialization commands and system constant/time setting/reference commands. Action commands have codes below 05h. If any one of these commands is executed, repeat jump is cancelled. For some commands, the previous command should be saved when the commands are inserted, since the commands are affected by the previous command

There are various types of command data, namely the coefficient data length, from 0 — 16 bits depending on each command. Please refer the following digital servo command specification.

S5L9232 supports only the MSB first micro-controller command input format. In the micro-controller command table, Italics means active low; '0' specified locations must be set to '0' when the command is used, and empty location is defined as 'don't care.'

STPcmd (Address 00H)

The STPcmd stops the execution of JMPcmd (05H) or automatic adjustment related servo operations, or changes the operations to the STOP mode. It also reduces the operating speed of embedded digital signal processor to save power consumption, turns on/off the laser diode, and clears the control/measurement data. The following descriptions of 4bit constant data are assigned.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
STPcmd	00								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
						LDX	IDLE	ABRT	STOP

.STOP : Stop Mode. This command can be activated in any mode. This command reserve the STOP until the MON signal turns off. However, if the STOPcmd (0080H) is re-executed while STOP is being reserved, it immediately executes the STOP regardless of the MON condition.
"0" : No execution. Executes next(ABRT) bit check.
"1" : Reserves the STOP mode.

.ABRT : Stops track searching and automatic control operation and returns to the previous state
"0" : No execution. Executes IDLE bit check.
"1" : Stops the jumping and control and returns to the previous state
This command should not be used with 11h, 14h, 15h commands. We recommend that 11h, 14h, 15h command be used with STOP(D8) for the same operation.

.IDLE : Sets to the IDLE (POWER SAVE MODE). RAM DATA remains.
"0" : Returns to normal mode from the idle mode.
"1" : Sets to IDLE MODE.

.LDX : Turns the laser diode on and off.
"0" : Laser diode off
"1" : Laser diode on

The priority order of the data bits is STOP, ABRT, and IDLE and LDX are equal priority. If the higher priority bits are "1", the IDLE and LDX bits are not checked.
All RAMs are cleared only when STOP=ABRT = 1. Although the RAM can be cleared using the normal STPcmd, in this case, the automatically controlled value and measurement are not cleared so that the servo can be immediately turned on without re-control in the next play. However, if the disc is changed, these values must be cleared. Because it is best to start from the beginning when the disc is changed, the control values should be cleared using the STPcmd options.
In the IDLE mode, the embedded digital signal processor's speed becomes 1/256, reducing the power consumptions. The IDLE and LDX bits can be accepted only when the servo is off.
If another action command is to be used before the execution of the automatic control command completes, the command must be first aborted using the STPcmd.

DDTcmd (Address 01H)

The DDTcmd checks for the presence of the disc and outputs the result, and it simultaneously measures the offset. It can also control both the focus error input gain and focus balance.
Before it performs the focus search, it automatically turns on the laser diode. The auto mode, which automatically uses the triangular waveform, and MICRO-CONTROLLER manual mode can be used for the focus search. The speed is controlled through FPS2 — 0 in either mode.
The focus actuator should be moved faster during disc detection compare with focus pull-in to determine if the disc is present. (The focus is not pulled-in.) It can read the data that indicates the type and presence of the disc.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
DDTcmd	01								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		AUTO	UPDN	FIGA	FBAL	RPT	FSP2	FSP1	FSP0

./AUTO ./UPDN : sets focus search mode.
0 0 : Auto mode. SENSE output indicates busy(L)/ready(H).
0 1 : Auto mode. Automatically executes to focus pull-in DDTcmd's search
1 0 : Manual up mode(actuator up). Actuator(FZC) signal is output through SENSE.
1 1 : Manual down mode(actuator down). Actuator(FZC) signal is output through SENSE.

./FIGA : The Focus input gain is changed by the FE peak level. Because the input gain reference changes in every control, control must be completed with one try.
"0" : Control
"1" : No control (maintain previous gain)

./FBAL : Controls F-BAL so that the minimum focus S-curve value and the absolute value of its maximum value becomes the same at DDTcmd.
"0" : Control
Fbal=--FBk*(FEmax+FEmin) or Fbias=(FEmax+FEmin)/Fbmthd according to (FLGcmd)
"1" : No control (maintain previous balance)

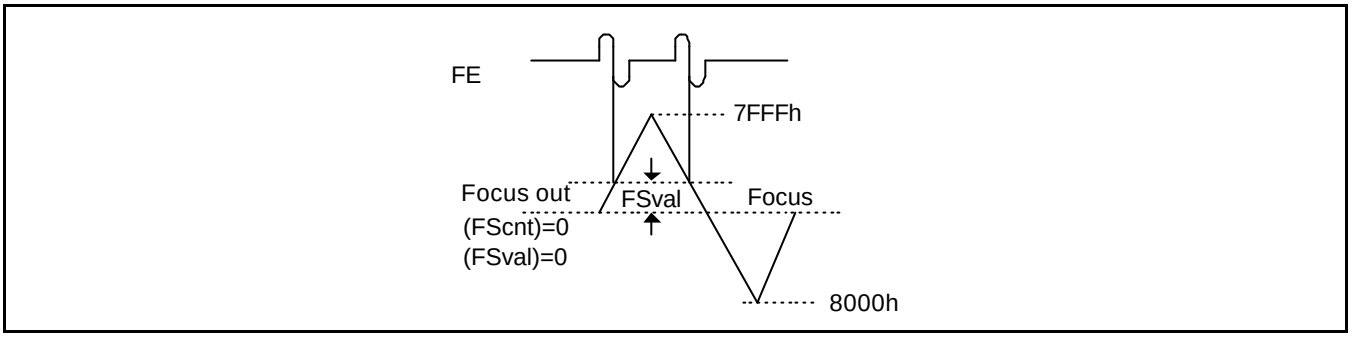
.RPT : Controls the number of Actuator's UP/DOWN searches
(when triangular waveform for the search is generated.)
"0" : Search only once.
"1" : REPEAT SEARCH (continues until the next command is input. However, SENSE becomes 'H" when the 1st run ends.)

.FSP2 .FSP1 .FSP0 : Bit that controls the DDTcmd and Focus pull-in actuator speed(slope).
0 0 0 : 2Hz (fast)
0 0 1 : 1Hz
0 1 1 : 1/2Hz
1 1 1 : 1/3Hz (slow) * Other settings are impossible.

*** Focus input gain control**

Manual and auto control methods are used for focus input gain control. The manual setting is recommended because of the unstable change in the FE peak signal, which is characteristics of the pickup. If the auto input gain control is chosen, the lookup table can be used to control the FEpk(00 — 7FH) , measured during disc detection, according to the size of FEpk so that the value becomes approximately 80% of the 8bit ADC full range (7FH). This can be set with direct port write command (1Ccmd:DPRWcmd) in the manual control method. Note, when the tracking balance is controlled in the off-track state using the auto control method, TEpk can be extracted from the first TZC component of TE to control tracking so that it equals the focus.

*** Focus search**



Focus out =(FScnt+FSval)*(FSpk)

If (FScnt)n = (FScnt)n-1 ± K (set K=3 in DDTcmd) for every M times, determined by FSP2 — 0, where M = 2m (the number of 1s of the m = FPS bit), fSRCH = fS/(2*216*M*K-1). where 2*216 is doubling the value since FScnt for 1 search cycle changes 0000h → 7FFFh → 0000h → 8000h → 0000h.

Register	Addr.	Function	Default	Value
FSpk	0055h	Output control coefficient at F-srch pull in(full swing %)	4000h	50%
unBal	004Fh	S-curve unbalance determination % reference	2003h	25%
DDT_J	0092h	Disc presence determination level	1000h	150mVp
NZM	0093h	Noise level determination reference	0800h	75mVp

- **DDT(Disc detect) Command Response format**

15 — 8	7	6	5	4	3	2	1	0
FE PEAK LEVEL	0	0	0	0	0	0	DIN	X

.FE PEAK LEVEL : S-curve peak level
.DIN : DISC presence
"0" : No disc
"1" : Presence
.X : Don't care

FONcmd (Address 02H)

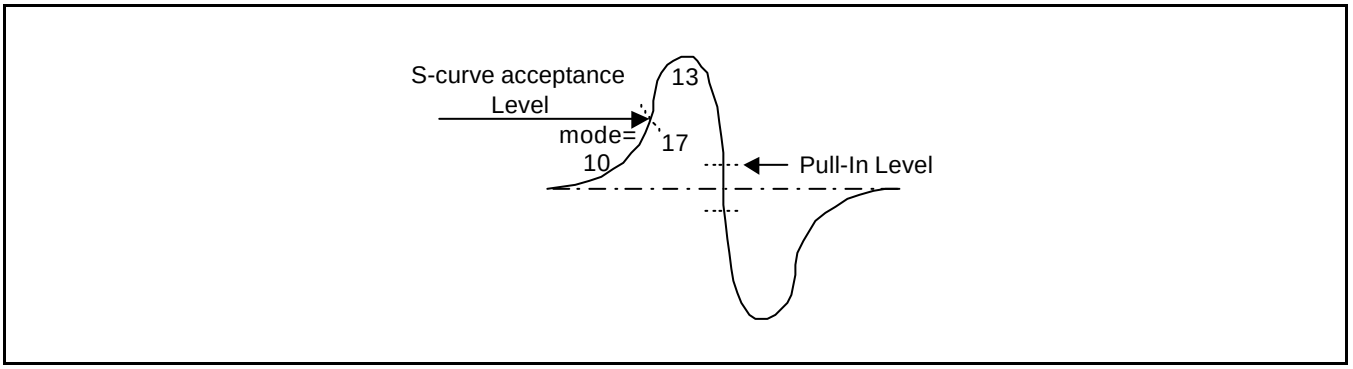
The FONcmd command turns the focus pull-in and tracking servo off. It automatically turns on the laser diode and selects from various forms of the pull-in method depending on the data accepted by the command. If the focus has already been turned on prior to the arrival of this command, nothing is executed. Furthermore, if FONcmd comes after TONcmd (03H), it turns on only the tracking servo.

- It turns on the focus loop filter when the AUTO bit of DDTcmd(01H) is '1'.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
FONcmd	02								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		LYRX	Fmthd	FOPI	FSPC	PIL3	PIL2	PIL1	PIL0

.LYRX : Assigns the focus search(pull-in) direction.
"0" : Pulls-in from the bottom. "1" : Pulls-in from the top.
.Fmthd : Assigns the focus pull-in method.
"0" : Pulls-in from the top and bottom of the S-curve.
"1" : Pulls -in either from the top or from the bottom of the S-curve.
./FOPI : Determines whether retrying pull-in should be within the search ranges(FSrng) at focus drop.
"0" : Auto mode (DSSP automatically tries to pull-in at focus drop)
"1" : Does not try to pull-in again. That is, MICRO-CONTROLLER uses the FONcmd to pull-in.
.FSPC : Automatic speed control bit at focus pull-in (This function reduces the search speed as the search comes closer to the pull-in point)
"0" : No automatic speed control (during search)
"1" : Automatic speed control (Reduces the search speed by half following the S-curve)
.PIL3, PIL2, PIL1, PIL0 : S-curve acceptance level : pull-in level

x	x	1	1	:	FEpk/2	:	FEpk/4
x	x	0	1	:	FEpk/2	:	FEpk/8
x	1	1	0	:	FEpk/4	:	FEpk/8
x	0	1	0	:	FEpk/4	:	FEpk/16
1	x	0	0	:	FEpk/8	:	FEpk/16
0	x	0	0	:	FEpk/8	:	FEpk/32



Register	Addr.	Function	Default	Value
FSpk	0055h	F-srch pull in output control coefficient (% full swing)	4000h	50%
FLoff	007Eh	FLKB (Focus lock) off time	0172h	4.4ms
FLon	007Fh	FLKB (Focus lock) on time	000Ah	113us
Fsrng	0091h	Focus re- pull-in search range	5000h	737mV

TONcmd (Address 03H)

TONcmd is the tracking pull-in command, which sets gains in the lens brake and track search mode.
There is no operation if tracking is already on when this command arrives.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
TONcmd	03								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
			SLSV		TOLB	MTLB	SFOG	STRG	

./SLSV : Sets sled servo on.
"0" : Turns on both tracking and sled servos on at the same time.
"1" : Does not turn on the sled servo (The sled command turns it on .)
.TOLB : Sets the lens brake when the tracking servo is turned on.
"0" : Does not turn on the Lens brake.
"1" : Turns on the lens brake until there is no MIRR signal.
.MTLB : Manual tracking lens brake
"0" : Does not turn on the Lens brake
"1" : Turns on the Lens brake(Turns on the lens brake when there is MIRR/TZC signal.)
.SFOG : Sets (kick+brk+GuT interval) focus gain during search
"0" : Does not change the gain.(manual)
"1" : Automatically changes the gain.(down: changes to temporary gain.)
.STRG : Sets the tracking gain when search ends (kick+brk+GuT+dlyTG interval).
"0" : Does not change the gain.(manual)
"1" : automatically changes the gain.(up: changes to temporary gain.)

Register	Addr.	Function	Default	Value
GuT	0077h	Track gain up time after jump (Track pull-in)	0400h	11.6ms
dlyTG	0079h	TGup delay time after Gut ends	0200h	5.5ms
TLoff	0080h	TLKB off delay time setting	0001h	11.3us
TLon	0081h	TLKB on delay time setting	0100h	2.9ms

SLDcmd (Address 04H)

This command controls the sled motor. The bit is checked from the HOMEIN bit. It moves the pickup in the both directions (from inside to outside and from outside to inside) and turns on and off the sled servo. The MICRO-CONTROLLER controls the sled movement during play. The sled can also be moved manually. It can also extract the home location.

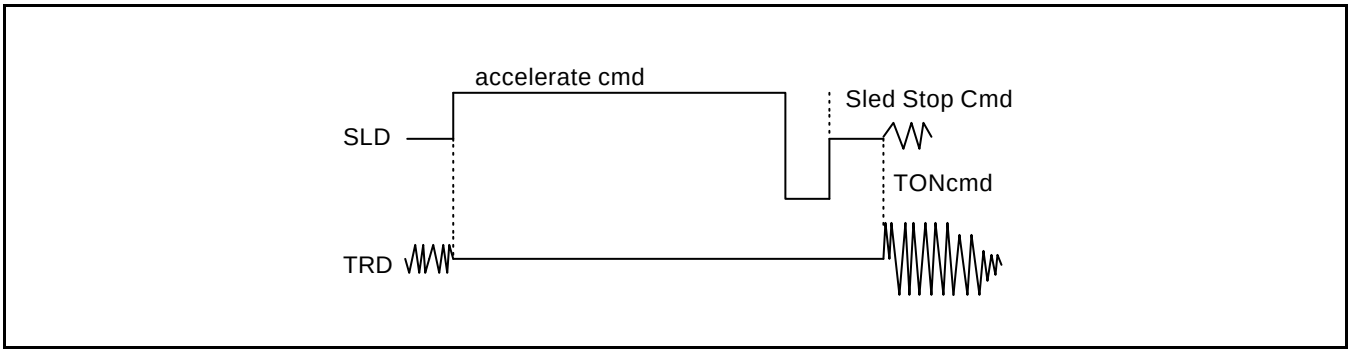
Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
SLDcmd	04								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
							SPLY	SMOV	HOMEIN

.HOMEIN : Set SLED HOMEIN MODE (priority Bit)
"0" : Off(Checks the upper bits.)
"1" : After returning to the home location, specified time: tHFwd, it moves to the outside.
SENSE = *BUSY*/READY

.SMOV, SPLY : Bit that controls the sled servo on/off and sled movement
0 0 : Sled servo off/ move off
0 1 : Sled servo on
1 0 : Sled forward move(in -> out). Sets the kick level to LEScmd's 'SKCKd'.
1 1 : Sled backward move(out -> in).Sets the kick level to LEScmd's 'SKCKd'.
Even after home in, kick more inwards during the specified time:tHBwd.
(only when the focus servo is off).

.DH4 — 0 : Don't care

It operates with SENSE = *BUSY*/READY when the focus servo is off. On the other hand, when the focus servo is on, SENSE becomes manual sled move. If OKScmd's Cout is "0", TZC signal is output through SENSE and, if not, (≠ 0=2n) track count busy signal is output through SENSE. Then, the MICRO-CONTROLLER counts these signals to move the sled. First OKScmd sets Cout; FONcmd turns off tracking; and then the SLDcmd accelerates the sled. When the number of SENSE signals nears the objective count, the SLDcmd brakes the sled. Then, when the interval between the SENSE signals are wide apart to consider the sled to have stopped, the SLMcmd turns off the brake pulse. After safe standby, it sends the track on command:TONcmd to turn on the tracking and sled servos to return to play.



Register	Addr.	Function	Default	Value
SKCKd	008Ch	SLED kick level(Vref reference)	7000h	1049ms
tHBwd	0056h	After home in, backward move time	1833h	70ms
tHFwd	007Bh	After home in, fwd move time	0F00h	43.3ms

JMPcmd (Address 05H)

The JMPcmd executes the track search. There are two types of search methods, track jump a sled move. With this command, repeated search is possible. The manual mode is available for track jump.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
JMPcmd	05	DIR	JPM1	JPM0	JIT2	JIT1	JIT0	JPD9	JPD8
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		JPD7	JPD6	JPD5	JPD4	JPD3	JPD2	JPD1	JPD0

.DIR : Sets the jump direction
"0" : Forward (outward) jump
"1" : Reverse (inward) jump

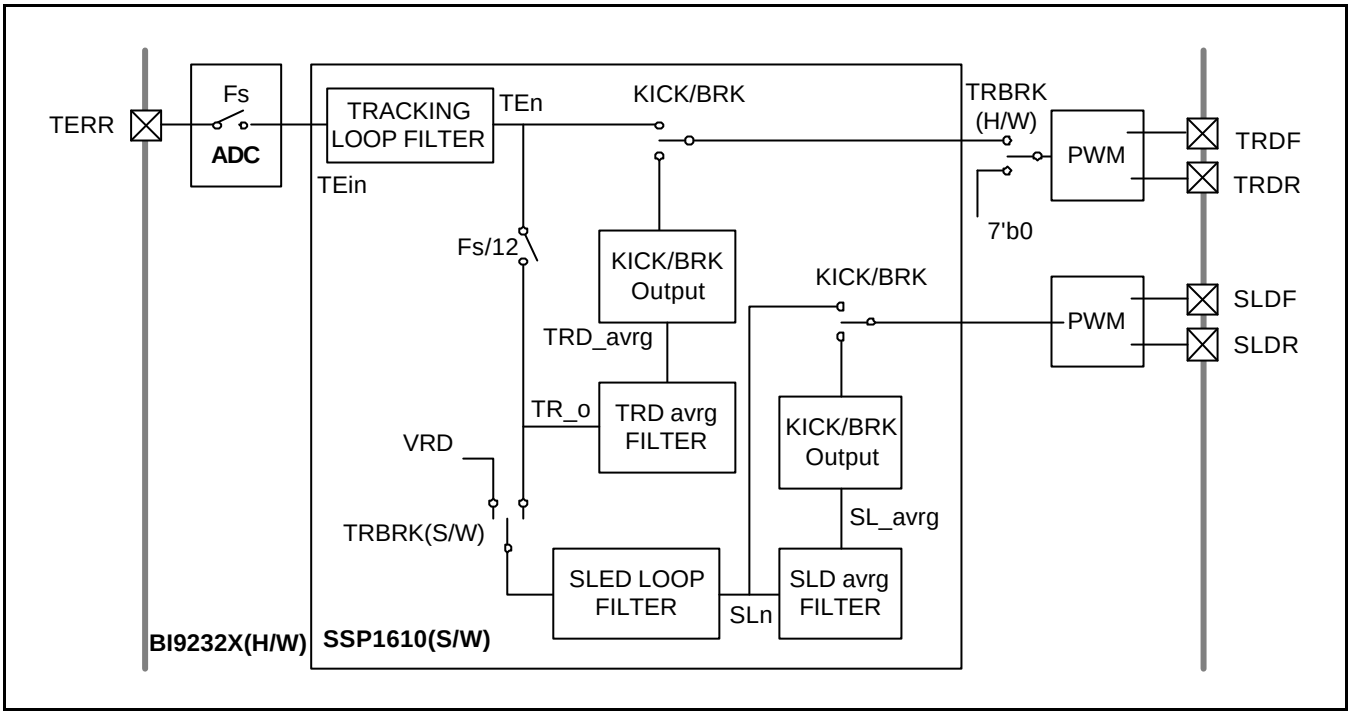
.JPM1 — 0 : Jump type assignment bit
"00" : Automatically determines whether to perform a track jump or sled jump depending on the number of jump tracks. The type of jump is determined by the boundary value:BOUND set by OKScmd.
"01" : Executes tracking jump
"10" : Executes sled move.
"11" : Repeats the track jump for every interval set in JIT_{2-0}(interval jump)

.JIT2 — 0 : Bit that sets the time interval of the repeated track jump. The period is the time from the initial jump time to the initial time of the next jump.

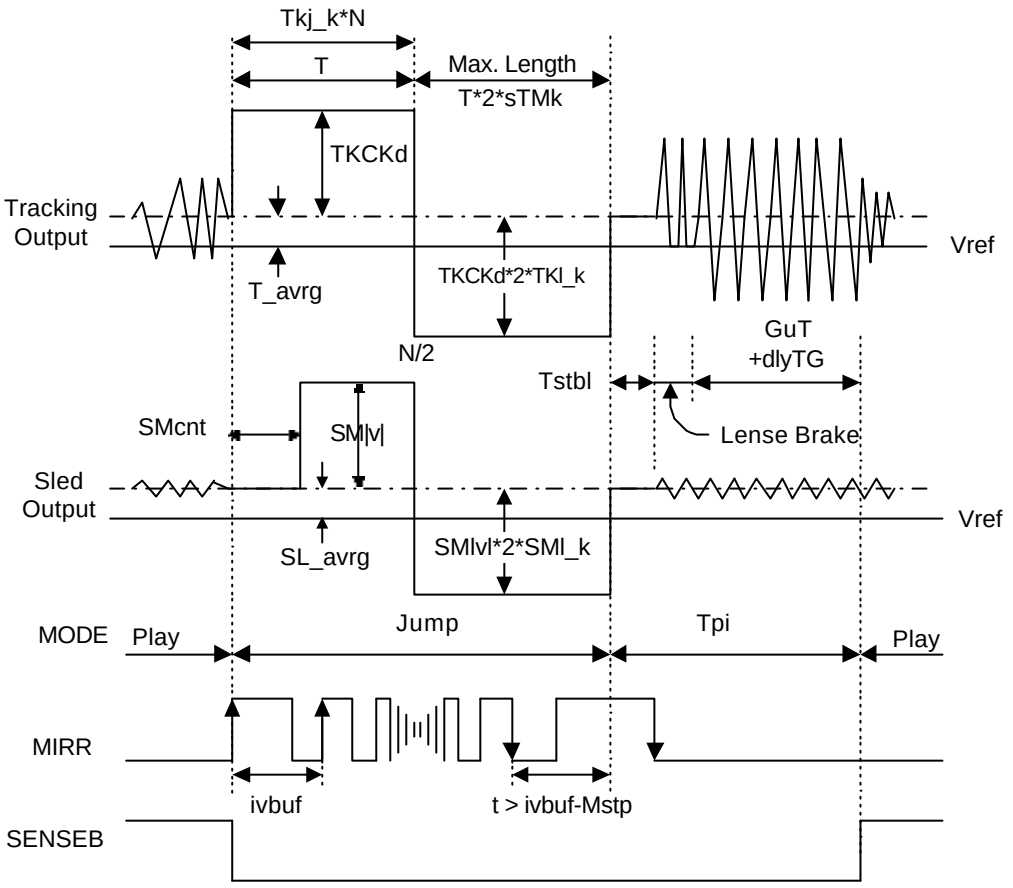
JIT2 ¾ 0	Time interval (repeat cycle)	Comment
0 0 0	Reserved	
0 0 1	2.7Hz	
0 1 0	5.4Hz	
0 1 1	8.1Hz	
1 0 0	13.5Hz	
1 0 1	21.6Hz	
1 1 0	29.7Hz	
1 1 1	40.5Hz	

.JPD12 — 0 : When the JPM1 — 0 bit is set to something besides "11" , JIT2 — 0 becomes JD12 — 10.
: When JPM1 — 0 bit is set to "10", the track number + 8 set by JD12 — 0 is the number of tracks to be jumped.

It reads in the lens brake on/off signal, which is created by the H/W, through the status register into SSP1611_CDP(Digital signal processor) to brake the sled output with the lens brake after a track jump. After it reads in the signal, then it substitutes the sled filter input (TR_o) data with '0' using software when the lens brake turns on. To do this, the 'SLbrk' bit must be set to '1' using the HDWcmd just after initializing the IC.



The kick level (TKCKd) was superposed onto the pre-jump average TRD output (TRD_avg) to generate the trk kick pulse, which was output through the TRD. If the track counter (H.CT) become half the count value (GSkbf) by jumping (N)*TKj_k trk, the brake turns on and this level becomes TKCKd*2*TKl_k times the original level. Jump direction is changed to the reverse direction if the level is less than the trk end condition at the MIRR reverse point during the brake interval. If this occurs, pickup can return to the location before the jump or pull-in can become unstable due to the sharp deceleration intervals. Therefore, the kick time (T)*2*sTMK is suggested for the maximum brake time to prevent sharp energy fluctuation between acceleration and deceleration.
If the number of tracks to move from the track kick reaches the sled move count (SMcnt), the sled move level (SMlvl) kick is superposed onto the pre-jump average sled output (SL_avrg) and the level becomes SMlvl*2*SMl_k as track kick and sled changes to brake. The kick/brake interval limit shares the tracking setting condition, except that SMcnt does not move the sled, but specifies the number of usable track range to jump only using the lens. The track pull-in (Tpi_int) routine actually starts to run after the stabilization time. After the Tstbl ends, the GuT is set to tracking gain up (when STRG=H); however, GuT continues to reload if lens brake (MIRR) exists. Therefore, after the period from the end of lens brake to the end of the GuT period ends, first of all, the focus gain down from the beginning of the jump is returned to normal. Then, after dlyTG time passes, tracking gain is also returned to normal, after which it returns to the normal play mode. Converting time of focus gain and that of tracking gain are different each other by dlyTG. The reason is for preventing the system from emergency situation such as tracking oscillation and focus drop which are resulted from the tracking gain conversion under the unstable focusing on converting or right after transition characteristics for focus gain. If the maximum deceleration period does not end at window(T*2*sTMk) : t < ivbuf-Mstp, it can return to over-acceleration (BRK) making it unstable. Therefore, the maximum brk time has been set.


Tkj_k*N
T
Max. Length
T*2*sTMk
TKCKd
Tracking
Output
Vref
T_avrg
TKCKd*2*TKl_k
N/2
GuT
+dlyTG
Tstbl
SMcnt
SMlvl
Lense Brake
Sled
Output
Vref
SL_avrg
SMlvl*2*SMl_k
MODE
Play
Jump
Tpi
Play
MIRR
ivbuf
t > ivbuf-Mstp
SENSEB

Register	Addr.	Function	Default	Value
TKCKd	008Bh	initial kick level	1800h	224.8mV
SMlvl	008Eh	Trk jump sled move level	7000h	1032mV
Tkj_k	0024h	Kick/brk duty setting coefficient	3D00h	47.70%
TKl_k	0026h	Trk brake level control coefficient	1000h	26.2%
SMl_k	0027h	Sled brake level control coefficient	C000h	-100%
SMbrkl	0028h	Brake level when sled move	0008h	0.00V
fsTjN	00BAh	Forced Brk control trk number	0003h	3trk
sTMk	00DAh	Trk brake interval detection window time Note1)	4000h	50.0%*2
LbT	0072h	Lens brake start time	0078h	1.35ms
Tstbl	0074h	Stabilization time after Trk jump	0000h	0us
Twin	0075h	MIRR/TZC blind time	000Ah	113us
Mstp	0076h	Jump stop time compensation time(stop=ivbuf-Mstp)	0003h	33.9us
GuT	0077h	Tgup delay time after jump end	0400h	11.6ms
Jstp	0078h	Stop when "Tracking jump stop timer<MIRR cycle"	0018h	271ms
dlyTG	0079h	Delay time after GuT end	0200h	5.5ms
tJap	007Ah	Jump assist procedure time(enMH=SLST=0)	024Ch	79.7ms
Cchg	0086h	Cout(up/dn) and TZC/MIRR(up) select track number	0080h	128trk
Bound	0087	Trk jump and sled move boundary trk number	0080h	128trk
SMcnt	0088h	Trk number from after trk kick to sled move	0001h	1trk
SScnt	0089h	Brake when the remaining track number becomes less than SScnt when the sled moves	0200h	512trk
Sbrk	005Bh	Sled move Brake max time	2380h	103ms

NOTE: the longest trk brk time = T * 2 * sTMk (T=kick time)

The finishing condition of jump is ivbuf-Mstp when INIcmd's BTS is 'L' and Jstp_Mstp when BTS is 'H'.
Before Twin, the TM1(Jump stop cycle (MIRR ↓ to ↓) detection down counter) is set to Jstp. After Twin, it is set to ivbuf or Jstp depending on the BTS.

EMEcmd (Address 07H)

The EMEcmd command directs the defect/shock emergency processing.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
EMEcmd	07								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		Test	SLST		upFv	dsAS	ASFO	ASTR	

.Test : Sets filter test mode (Set by FTSTcmd.)
"0" : Normal mode "1" : Filter test mode
.SLST : Bit that decides whether to stop the sled when the lock signal turns off.
"0" : No STOP "1" : STOP
.upFv : Specify whether or not to compensate the focus output offset: FSval when the focus pulls in.
"0" : No compensation (during the time measured in focus search)
"1" : Compensation
.dsAS : Specify whether or not to process the anti-shock.
"0" : Enable. Validates ASFO, ASTR and ASBR functions.
"1" : Disable. Leave it up to the servo.
.ASFO : Bit that decides on whether to down the focus gain in case of a shock
"0" : Maintains the focus gain to normal.
"1" : Downs the focus gain.
.ASTR : Bit that decides on whether to up the tracking gain in case of a shock
"0" : Maintains the tracking gain to normal.
"1" : Ups the tracking gain

When shock is detected, ATSCed is set by reading output flag from the RF into the status register. In play mode, both DFCT and ATSC are executed by one interrupt routine that has (88.1/16)kHz time period. After verifying that ATSCed had been set and ATSC process had been enabled (DSAS = L), tracking gain up and focus gain down start to be processed depending on the set mode. They were processed by the interrupt immediately after an emergency (maximum delay = 135.6us) and finished by the main loop because timing is not critical.

Register	Addr.	Function	Default	Value
tDFCT	0057h	TGup hold time for LOCK off in case of DFCT	0800h	23ms
DFCTpd	007Ch	Set DFCT handling time after DFCT	0040h	723us
ATSCd	007Dh	Set ATSC handling time after ATSC	0400h	11.6ms

HDWcmd (Address 08H)

The HDWcmd initializes the DSSP hardware settings. After the reset is released, this command is executed first. This command cannot be executed in any state except in the STBY state.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
HDWcmd	08								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
			SSTOP	LPDS	SPhold	PCUP		SLbrk	0

.SSTOP : The active H/L of limit switch can be selected according to the Mechanism.
"0" : High active (Limit Switch is High)
"1" : Low active (Limit Switch is Low)

.LPDS : Flag for low power digital servo operation(Play mode H/W enable)
"0" : PMHW(play mode hardware) disable
"1" : PMHW(play mode hardware) enable

.Sphold : Spindle hold select in FOKB = H & LOCK = L states
"0" : Hold
"1" : No Hold

.PCUP : Pick-up type
"0" : Vibration resistant pick-up
"1" : Vibration non-resistant pick-up (Hinge, plate-spring type)

.SLbrk : Decides on whether to process SLE as zero considering the TRD zero output at lens brake
"0" : Lens brake not considered.
"1" : Process SLE as zero at Lens brake

INIcmd (Address 09H)

The INIcmd command sets the initial values.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
INIcmd	09								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
			JPCK			BJJM	BTS	enJaP	SLref

.JPCK : Sets the signal used for track search /count when the sled moves
"0" : TZC
"1" : MIRR

.BJJM : Setting on whether to convert the remaining number of tracks to track jump after track search.
"0" : Continuous sled movement
"1" : Executes SLED MOVE + TRACK JUMP

♣ Convert to track jump if the number of tracks remaining after sled movement using TZC/MIRR is less than the bound set by OKScmd.

.BTS : TZC frequency that decides on the time when the track kick/jump is to stop.
"0" : Stops if the cycle becomes the same as the MIRR cycle when kick started.
"1" : Stops when it becomes the same as Jstp set by TMScmd (0CH).

.enJap : Mandatory enMH = 0, SLST = 0 for tJaP after track search
"0" : Execute.
"1" : Not execute.

.SLref : Select SLED kick reference
"L" : Vref
"H" : Sled average

SPDcmd (Address 0BH)

SPDcmd sets the playback speed. One of the two kinds of filter coefficients is supposed to be set by this command. This command is always available to change the speed.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
SPDcmd	0B								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
									SPD

.DH7—1 : Reserved. "Must set to L".
.SPD : Play speed (Speed X) setting bit
"0" : 1X(RAM address pointer = 8X — BX)
"1" : 2X(RAM address pointer = CX — FX)

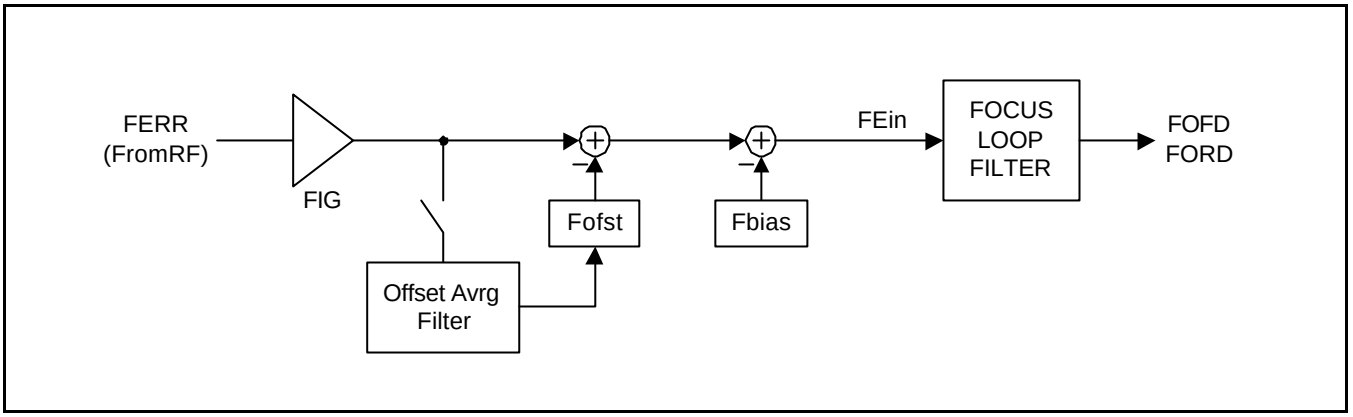
♣ This command only selects the actual usable filter coefficient set. The signal processing command selects the rotation speed.

OFAcmd (Address 11H)

The OFAcmd controls the focus/tracking offset. The focus must be off to receive this command. This command can be used to turn on or off the laser diode and to measure average t0Fa time of the focus error/tracking error that includes the electrical offset. Final error value is as each erroneous input minus t0Fa. Even when the control ends, the laser diode changes to STANDBY mode as long as it is on, if offset is controlled in the state of LD on. Because it takes time for the laser output to stabilize after being turned on, it is better to control the tracking offset first and then focus offset. Whereas tracking offset control is nearly all measurement of the electrical offset, the focus offset control almost precisely measures the off focus error level (this value used in the DDTcmd, the next command executed.)

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
OFAcmd	11								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
								LDoff	FTS

.FTS : Selects either the focus or tracking offset adjust.
"0" : Focus offset adjust "1" : Tracking offset adjust
.LDoff : LD on/off offset measurement select.
"0" : LD on "1" : LD off



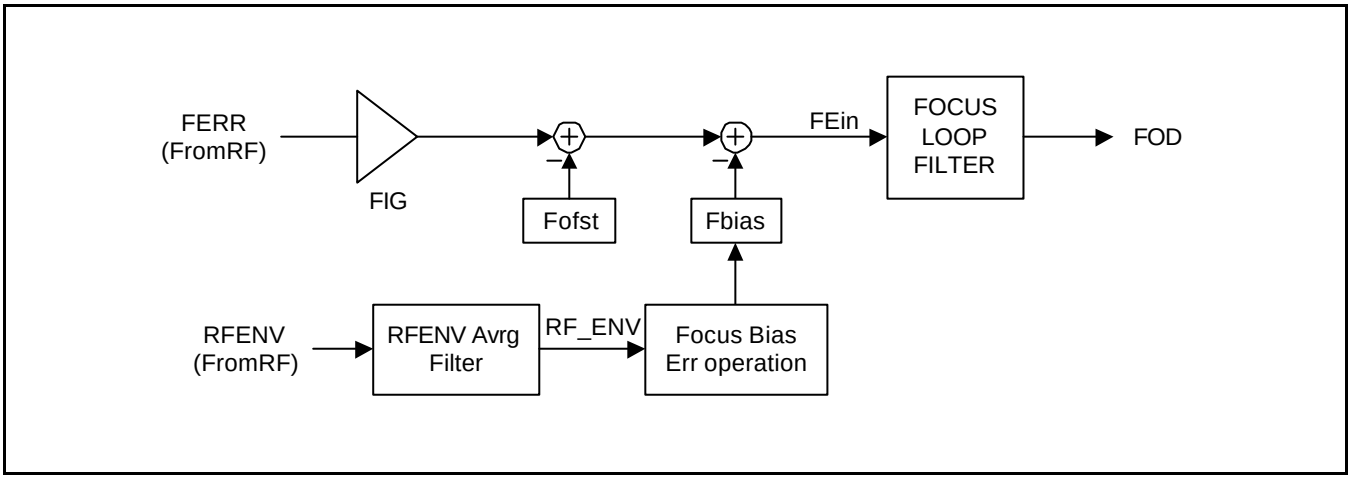
Register	Addr.	Function	Default	Value
ofst K0	003Ch	Offset average filter new data gain(K0=1-K)	0060h	-
ofst K	003Dh	Offset average filter old data gain	7FA0h	-
tOFa	0058h	Offset measurement time(average value measurement time)	0FF0h	46.2ms
Fofst	1003h	Focus offset controlled value	0000h	-
Tofst	1005h	Tracking offset controlled value	0000h	-

FBAcmd (Address 12H)

The FBAcmd command controls the focus balance during playback. It controls the focus bias to play with the best quality RF signal. The quality of the RF signal can be evaluated with the amount of jitter; however, an algorithm to find the minimum jitter in the IC is realistically impossible to create. The focus bias is controlled so that the RF envelope becomes maximum using the fact that jitter becomes minimum near the focus bias where the RF envelope maximizes. Disc detection: DDTcmd controls the balance so that the size of the peak and bottom is the same, but this command supports the following two control types to maximize the peak level of the RF signal envelope.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
FBAcmd	12								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0

Measurement cycle with respect for RF amplifier: The relationship between FBpd and cut-off frequency of RF envelope average filter must be reasonable. The following is a flow diagram of bias control.



Register	Addr.	Function	Default	Value
FBpd	0059h	Focus bias control RFENV measurement cycle	0172h	50ms
FBok	0082h	Focus bias OK level	0400h	± 36mV
dXbuf	0029h	initial dX setting level	0C00h	110mV
Fbias	0098	Focus bias controlled value	0000h	0V

TBAcmd (Address 13H)

The TBAcmd command controls the tracking balance when the focus is on. The followings are controlled to make the average nTbal cycle sizes of the peak and bottom equal within the specific frequency range of the tracking error signal derived from off track eccentricity.

Track balance: Tbal output control (repeat:RPTB=0)

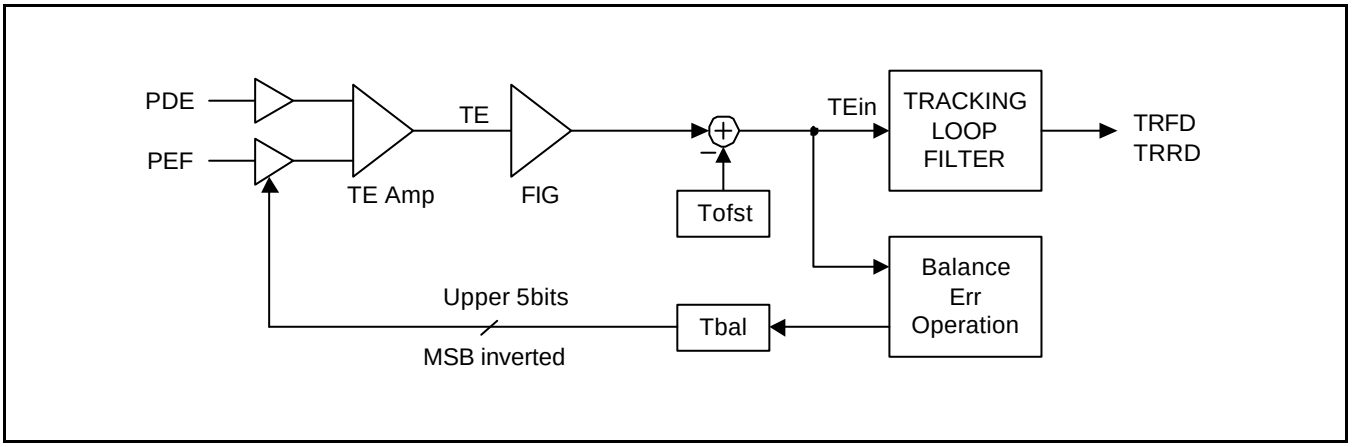
Track bias: Sets the Tbias and subtracts it from the TE input.(Tbmthd=1)

After changing the Track balance:Tbal output, a RF amp is absolutely required to control it. However, the bias subtraction method does not require the RF amp. The tracking balance method: Tbmthd bit of the flag command:FLGcmd specifies which method to use. In the bias method, control ends with one measurement.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
TBAcmd	13								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
								RPTB	TIGA

./TIGA : Control of tracking input gain according to the peak level of the tracking error(TE) signal.
"0" : Control "1" : No control.

./RPTB : Sets whether to repeat tracking balance control.
"0" : Continues to repeat after the standby for the stabilization time(TBwt) until the error becomes less than the allowable value(Tbok).
"1" : Does not repeat



Register	Addr.	Function	Default	Value
nTbal	0061h	The number of TZC cycle to extract the first balance err	000Ah	10trk
TBwt	005Ah	Wait time from the Tbal change to re-measurement	1000h	46.3ms
TBok	0083h	t_bal ok level(allowable error)	0400h	± 36mV
TBk	002Bh	Trk balance control sensitivity coefficient	0800h	100%
Tengh	0041h	TZC size maximum limit	3000h	450mV
fmin	104Bh	TZC detection minimum frequency	00F6h	359Hz
fmax	104Ch	TZC detection maximum frequency	0018h	3.68kHz
Tbias	0099h	Tracking bias controlled value	0000h	-
Tbal	0097h	Tracking balance controlled value	0000h	-

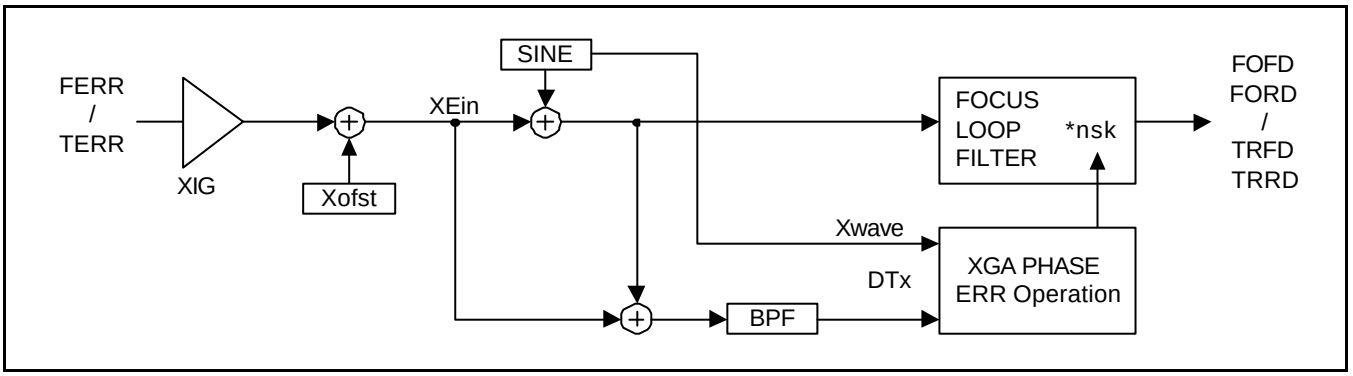
*nTbal must be a value applicable to 2n. In order to calculate Work0(Σ [TEmin+TEmax]/nTbal result register), nTbal must be the divisor when calculated internally, and, in embedded digital signal processor(SSP1611_CDP), it must equal to 2n because it must be divided by the bit shift. Essentially, it will be used in 0001h=20(0 bit shift) and 0080h=27(7 bit shift).

FGAcmd (Address 14H)

The FGAcmd is the command that adjusts the auto focus gain during playback.
The servo loop superposes the measured waveform of Kf(Kf*sin(Fwave)) where Kf is determined by Ffrq. After waiting for the FGwt cycle and stabilizing it, the detection signal phase difference is integrated for the interval of FGcnt cycle. The value multiplied by the feedback gain coefficient:Kcf of the phase difference is added to the output gain until the result of this integration becomes less than the allowable value:FGok to change the gain. This is repeated until the loop gain is controlled using Ffrq frequency so that it becomes 0db.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
FGAcmd	14								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0

The following diagram shows the loop gain control operation. (same as focus/tracking)



Register	Addr.	Function	Default	Value
xGcnt	0090h	measurement cycle	000Ah	10 times note1)
xGwt	008Fh	waiting time	0018h	24 times
Ffrq	0044h	Focus loop bandwidth(sine frequency)	000Ah	798.2Hz
Kf	0046h	F_gain (sine)disturbance level	1000h	300mVpp
Kcf	002Ch	F_gain control sensitivity coefficient	4000h	0.5X
FGok	0084h	F_gain control OK level	0080h	± 2.3mV
FGmax	005Ch	F_gain control upper limit	7000h	nsk
FGmin	005Dh	F_gain control lower limit	0800h	nsk
FGN1nsk	00B7h	Focus gain normal output gain (1X)	2000h	nsk
FGD1nsk	00A7h	Focus gain down output gain (1X)	1000h	nsk

NOTE: Repeat the cycle of sine table 10 times.

TGAcmd (Address 15H)

The TGAcmd is the command that adjusts the auto tracking gain during playback.
The servo loop superposes the measured waveform of Kt(Kt*sin(Twave)) where Kt is determined by Tfrq. After waiting for the TGwt cycle and stabilizing it, the detection signal phase difference is integrated for the interval of TGcnt cycle. The value multiplied by the return gain coefficient:Kcf of the phase difference is added to the output gain until the result of this integration becomes less than the allowable value:TGok to change the gain. This is repeated until the loop gain is controlled using Tfrq frequency so that it becomes 0db.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
TGAcmd	15								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0

For the operation of tracking gain adjustment, refer to the focus loop gain adjustment in the previous sections.

Register	Addr.	Function	Default	Value
xGcnt	0090h	measurement cycle	000Ah	10 times note1)
xGwt	008Fh	waiting time	0018h	24 times
Tfrq	0048h	Tracking loop bandwidth(sine frequency)	000Bh	1.1kHz
Kt	004Ah	T_gain (sine)disturbance level	1000h	300mVpp
Kct	002Dh	T_gain control sensitivity coefficient	4000h	0.5X
TGok	0085h	T_gain control OK level	0040h	2.34mV
TGmax	005Eh	T_gain control upper limit	7000h	nsk
TGmin	005Fh	T_gain control lower limit	0800h	nsk
TGN1nsk	00EFh	Tracking gain normal output gain (1X)	2BB2h	nsk
TGD1nsk	00E7h	Tracking gain down output gain (1X)	286Fh	nsk

NOTE: Repeat the cycle of sine table 10 times.

RFSNScmd (Address 17H)

The RFSNScmd is the command that selects the SENSE pin output signal. Because this command was made to test the RF, it can operate with only MCK, without XI input. Besides, this command can be operated without any test mode setting.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RFSNScmd	17								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
							SEN2	SEN1	SEN0

.SEN2 — 0 : SEN2 — 0 determine the SENSE output as follows:

SNS2 ¾ 0 (SNSsel)	SENSE Output
000	SENSE
001	ATSC
010	CPEAK
011	SSTOPO
100	TZCO
101	Reserved
110	Reserved
111	Reserved

SQDTcmd (Address 18H)

The SQDTcmd is the command that selects the SQDT pin output signal. This command can be used to select from SQDT, FOK, and LKFS signals etc. according to MICRO-CONTROLLER requirements.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
SQDTcmd	18								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
								SQDT1	SQDT0

.SQDT1 — 0 : SQDT1 — 0 determine the SQDT pin output as follows:

SQDT1 ¾ 0	SQDT output
00	SQDT
01	FOK
10	LKFS
11	SQDT

The FOKB and LKFS signals selected through this command can be monitored using 19h command. However, there are instances when the MICRO-CONTROLLER cannot use the SENSE pin because FOKB and LKFS etc. must be monitored at the same time the end of the jump is verified through continuous monitoring of SENSE after the jump command. Therefore, this command has also the additional ability to monitor the SQDT pin to verify focus drop and LOCK off etc. without using the FOKB and LKFS etc. ports during a jump.

SNScmd (Address 19H)

This SNScmd command selects the SENSE pin output signal. Therefore, Cout, FOKB, LKFS(GFS), SOS1, TLKB etc. signals can be monitored with this command as required by the MICRO-CONTROLLER.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
SNScmd	19								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
			SNS2	SNS1	SNS0			Ssel	

.SNS2 — 0, Ssel : SNS2 — 0(SNSsel[2:0])and Ssel combinations determine the SENSE output as follows

SNS2 ¾ 0 (SNSsel)	Ssel	SENSE output
000	0	ST5 Always H output
001	0	FLK
010	0	Cout
011	0	Sout It can be monitored with DDTcmd limit check & manual sled move
100	0	FOK
101	0	LKFS(GFS)
110	0	S0S1
111	0	TLKB
XXX	1	Serial

FLGcmd (Address 1AH)

The FLGcmd command refers and makes change to the flag in the DSSP system.

Command		DH								Comment
Name	code	D15	D14	D13	D12	D11	D10	D9	D8	Bold
FLGcmd	1A	**stp**	**Fptmg**	SSVon	HOME	itvJ	TSV	SSV	**enTJn**	Character
		DL								(Setting
		D7	D6	D5	D4	D3	D2	D1	D0	Cmd)
		DFCTed	ATSCed	**Tbmthd**			**FSend**		**enLOCK**	

.**Stp** : Stop reservation flag
"0" : No Stop
"1" : Stop reservation

.**Fptmg** : Focus re-pull-in timing select bit
"0" : Start re-pull-in after deviating FLK
"1" : Start re-pull-in after deviating FOK

♣ If the spindle motor is off (MON=L), each output is turned off and goes into STBY state.
Re-pull-in is prohibited at this time.

.SSVon : (Sled servo on & LOCK & not filter test mode) status flag
"0" : No
"1" : Yes

.HOME : Operation of HOME location flag
"0" : Operation of HOME location off.
"1" : Operation of HOME location on.

.itvj : Interval jump flag
"0" : Interval jumping off.
"1" : Interval jumping on.

.TSV : Track servo flag
"0" : Off
"1" : On

.SSV : Sled servo flag
"0" : Off
"1" : On

.enTJn : On completing specified number of track jump
"0" : No trk pull-in whatsoever.
"1" : trk pull-in

.DFCTed : Defect period flag
"0" : No Defect period
"1" : Defect period

.ATSCed : Anti-shock period flag
"0" : No Anti-shock period
"1" : Anti-shock period

.**Tbmthd** : Tracking balance control method
"0" : Controls the balance in the RF amp based on the tracking balance:Tbal output.
"1" : Compensate tracking error balance based on bias decrease

.**FSend** : Focus search end location select
"0" : Vref(operating current¡Ö0 position)
"1" : Pull-in range from the focus point (location below FSrng)

.**enLOCK** : tracking gain when the lock drops
"0" : Normal
"1" : Up

SNSCcmd (Address 1BH)

The SNSCcmd command selects the SENSE pin output signal and also monitors the DSSP internal data. Besides, after running JMPcmd, it returns the SENSE output to normal SENSE output from the SENSE output of JMPcmd for executing a non-DSSP command. Essentially, it has the ability to change it back to BUSY/READY regarding JMPcmd. Because the monitored data come out through PWM logic of the sled output pins (SLDF/SLDR), they can be observed in real time using an oscilloscope. In addition to the 16 bit upper data, the lower data can also be monitored by the monitor output gain command:TTKcmd(=57h). (If Gain=0040h, upper byte, but, if 4000h, the lower byte is output.)
Namely, if this command is used for monitoring, SLDF and SLDR are used as the monitor pins. Therefore, this command is used to make all BANK & MOD7-0 equal to "0" and RWB= "0" (select only SENSE output) to return to the original sled output. Therefore, the monitoring of address '000' is not available. 1B00H must be inserted after this command is used.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
SNSCcmd	1B	RWB		*NORM*	FTLK				BANK
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		MOD7	MOD6	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0

.RWB : Setting of input and output of the RAM address to be monitored
"0" : Write
"1" : Read
./NORM,FTLK : SENSE pin output control bit
"0 0" : Normal SENSE output (READY/*BUSY*)
"0 1" : Return SENSE to jump/BUSY after running a non-DSSP command after a jump
SENSE pin generates H state in the Play mode
"1 0" : FLKB output
"1 1" : TLKB output
.BANK : RAM bank that has the data to be monitored
.MOD7 — MOD0 : Address in the RAM bank that has the data to be monitored

♣ Only PAGE0 of the internal RAM can be monitored. PAGE1 does not need to be monitored since it contains unchanging coefficient data.

DPRWcmd (Address 1CH)

The DPRWcmd command directly reads from and writes to the DSSP input/output port.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
DPRWcmd	1C	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		DD3	DD2	DD1	DD0	ST6	DPS2	DPS1	DPS0

.ST6,DPS2 — 0 : Select output port
.DD11 — 0 : Data to be written (if DD[11:0] is FFFh, execute read operation)

♣ Data read method : Sets all DD11 - 0 data 12bits to 1. Unrelated to ST6.
DO[15:0] can be get by sending MCK after a Command is applied.
Example) After sending "1CFFF3", the external status input data are read.

.ST6, DPS2 — 0
"X000" : Read A/D converted digital data. (DO[15:8]is A/D Converted 8bit data)
"X001" : Read interrupt vector of free running counter. (DO[7:0]is interrupt vector)
"X010" : Read RFcnt (RF count). (DO[15:0])
"X011" : Read external status. (DO[15:0])

15	14	13	12	11	10	9	8
ATSC							S_sw
7	6	5	4	3	2	1	0
MON	TZC	MIRR	FOK		ADCok	TR_BRK	LOCK

.ATSC : Vibration(shock) detect bit
.S_sw : Sled limit switch (= SSTOP)
.MON : Spindle motor on
.TZC : Track zero cross
.MIRR : On-track signal
.FOK : RF_detect signal
.ADCok : ADC complete bit
.TR_BRK : Lens brake
.LOCK : Lock signal

"X100" : Read count value of hardware track counter HCT. (DO[15:0])
"X101" : Read data accepted from MICRO-CONTROLLER. (DO[15:0])
"X110" : Read command accepted from MICRO-CONTROLLER. (DO[7:0])
"X111" : Read ONTcnt(On Track Count). (DO[15:0])

* Data write method : Set data other than "1" to DD11—0 and select the output pins using ST6 and DPS2 — 0.

Example) Because "0100" is written to the DSSP control register when "1C100B" is sent, the laser turns on.

.ST6, DPS2-0

"0000" : Writes data(DD[11:4]) to DSSP and FOFD/FORD generate PWM output of the data.
"0001" : Writes data(DD[11:4]) to DSSP and TRFD/TRRD generate PWM output of the data.
"0010" : Writes data(DD[11:6]) to DSSP and SLFD/SLRD generate PWM output of the data.
"0011" : Writes data(DD[11:6]) to DSSP and SPD generates PWM output of the data.
"0100" : Write DD[11:4] and DD[9:7] to Fin_G of memory and FG[2:0] respectively.
"0101" : Write DD[11:4] and DD[9:7] to Tin_G of memory and TG[2:0] respectively.
"0110" : Write DD[11:4] to VRP(Vref+).
"X111" : Reset counter RFcnt.
"1000" : Write DD[2:0] to analog select register (Asel)

ASEL<2:0>			**Signal Selection**	
2	1	0	Active	Descriptions
0	0	0	TESEN	TES(Tracking Error Sum)
0	0	1	TEEN	TE(Tracking Error)
0	1	0	TESEN	TES(Tracking Error Sum)
0	1	1	SMEEN	SME(Spindle Motor Error)
1	0	0	TESEN	TES(Tracking Error Sum)
1	0	1	FEEN	FE(Focus Error)
1	1	0	TESEN	TES(Tracking Error Sum)
1	1	1	VREN	VREF(Voltage Reference)

"1001" : Write DD[7:0] to interrupt vector register (VCT).
"1010" : Reserved
"1011" : Write DD[11:0] to CNTbuf's lower 12 bits and put upper 4 bits "0".

15	14	13	12	11	10	9	8
Sout	DDTF	VRseL	SNSsel(2:0)			TM	LDON
7	6	5	4	3	2	1	0
BRKENB	JMPF	TLK	FLK	Ssel	Csel	LSWsel	"0"

.Sout : Sense out
.DDTF: Disc detect mode flag(1:DDT processing, 0:not DDT mode)
.VRsel: Select VR/VR+ by controlling VREF MUX input(1:VR+, 0:VR)
.SNSsel: Sense data information
.T/M : TZC/MIRR select
.LDON: Laser diode on/off
.BRKENB: Brake disable/enable
.JMPF: Track jump mode flag(1:jumping, 0:not jump mode)
.TLK : Tracking lock (-> /TLK at output pin)
.FLK : Focus lock (-> /FLK at output pin)
.Ssel : Sense output select
.Csel : Counter clock select
.LSWsel: Limit switch active high/low select

"1100" : Clears the hardware track counter H.CT to 0000H
"1101" : Writes DD[11:0] to the upper 12 bits of register sent to micro-controller , and '1101' to the lower 4 bits of the register.
"1110" : Writes DD[11:4] to the tracking balance output (TBAL).
"1111" : Reset ONTcnt.

FTSTcmd (Address 1DH)

The FTSTcmd command measures internal digital filter characteristics of DSSP. By forcing the internal mode to PLAY to run each filter and converting the filter input to normal, this command should not be applied while the pickup and motor are connected to the DSSP output. The SLED filter input shares the TE filter input.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
FTSTcmd	1D								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
					WTF				WFF

.WTF : Sets tracking filter measurement gain
"0" : Tracking filter normal test
"1" : Tracking filter up test

.WFF : Sets focus filter measurement gain
"0" : Focus filter normal test
"1" : Focus filter down test

RamRcmd (Address 1EH)

The RamRcmd command refers to the internal RAM contents of DSSP. Continuous outputs are possible.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RamRcmd	1E	NEXT	0	0	BANK	0	0	0	PAGE
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		RAM7	RAM6	RAM5	RAM4	RAM3	RAM2	RAM1	RAM0

.NEXT : Address setting method
"0" : Assigns the RAM address to BANK, PAGE and RAM7-RAM0.
"1" : Add 1 to the RAM address of the previous cycle and make it the RAM address of the present cycle. (Lower bits are not required)
.DH6—5,3—1 : Reserved. Must be set to "0".
.BANK : Set memory bank (0 or 1)
.PAGE : Set memory page (0 or 1)
.RAM7—RAM0 : Internal SRAM address assignment. SRAM is composed of total 1024 words , which is 512 words of BANK0 and 512 words of BANK1 according to pages 0 and 1.

RamWcmd (Address 1FH)

The RamWcmd command writes 16 bit data to the internal RAM of DSSP. Continuous writing is also available.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RamWcmd	1F	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

.RD15 — RD0 : Data to be written.
♣ Before writing data, the write addresses should set by RamRcmd. This command should be issued continuously to write to the consecutive address. If RamWcmd is issued just before the current cycle, DSSP adds 1 to the address of the previous cycle and makes this the address of the present cycle, to where it writes the present data. If address is added by 1 and become "00" for both RamRcmd and RamWcmd command, then the page is also increased by 1 automatically.

TTKcmd (Address 20H)

The TTKcmd command refers and makes changes to the output gain when SNSCcmd monitors the internal RAM.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
TTKcmd	20	LK15	LK14	LK13	LK12	LK11	LK10	LK9	LK8
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		LK7	LK6	LK5	LK4	LK3	LK2	LK1	LK0

.LK15 — 0 : Monitor output gain coefficient (nsk)

FTGcmd (Address 21H)

The FTGcmd command changes the focus/tracking gain manually.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
FTGcmd	21								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
						UP	Tchg	DWN	Fchg

.Fchg : Changes focus gain.
"0" : No change.
"1" : Change.(DWN valid)
.DWN : Focus gain
"0" : normal mode recovery (normal/down)
"1" : forced gain down (always gain down)
.Tchg : Changes tracking gain.
"0" : No change.
"1" : change (UP valid)
.UP : Tracking gain
"0" : normal mode recovery (normal/up)
"1" : forced gain up (always gain up)

PWMcmd (Address 30H)

The PWMcmd command sets PWM output mode.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
PWMcmd	30			SPM1	SPM0			SLM1	SLM0
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
			TRM2	TRM1	TRM0		FOM2	FOM1	FOM0

Address	Register	6-bit TRM, FOM	7-bit TRM, FOM
00d8	Pwm9	FC00	FE00
011d	bosang	0200	0100

.SPM[1:0] : Spindle PWM output format.

SPM[1:0]	Resolution	Expression	Clock
00	5bit	2's complement	88.2kHz
01	5bit	Signed Magnitude	88.2kHz
10	6bit	2's complement	176.4kHz
11	6bit	2's complement	176.4kHz

.SLM[1:0] : Sled PWM output format.

SLM[1:0]	Resolution	Expression	Clock
00	5bit	2's complement	88.2kHz
01	5bit	Signed Magnitude	88.2kHz
10	6bit	2's complement	176.4kHz
11	6bit	2's complement	176.4kHz

.TRM[2:0] : Over-sampled tracking PWM output format.

TRM[2:0]	Resolution	Expression	Clock
000	6bit	2's complement	5.6448MHz
001	6bit	Signed Magnitude	5.6448MHz
010	7bit	2's complement	11.2896MHz
011	7bit	Signed Magnitude	11.2896MHz
100	6bit	2's complement	5.6448MHz
101	6bit	Signed Magnitude	5.6448MHz
110	7bit	2's complement	11.2896MHz
111	7bit	Signed Magnitude	11.2896MHz

.FOM[2:0] : Over-sampled focus PWM output format.

FOM[2:0]	Resolution	Expression	Clock
000	6bit	2's complement	5.6448MHz
001	6bit	Signed Magnitude	5.6448MHz
010	7bit	2's complement	11.2896MHz
011	7bit	Signed Magnitude	11.2896MHz
100	6bit	2's complement	5.6448MHz
101	6bit	Signed Magnitude	5.6448MHz
110	7bit	2's complement	11.2896MHz
111	7bit	Signed Magnitude	11.2896MHz

RFMRcmd (Address 58H)

The RFMRcmd command is the RF Mirror control commands.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RFMRcmd	58								EQS
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0

.EQS : Selects EQO pin output signal
0: EQO 1: RFO
.MC0 : EQ input level selection
0: EQI/2 1: EQI
.MC1 : MIRROR bias setting bit
0: MIRROR BIAS OFF 1: MIRROR BIAS ON
.MC2 : RFN2 input selection
0: RFN2 1: MIRRB (Mirror Bias input)
.MC3 : MIRROR gain selection bit
0: 1.5X MIRROR Gain 1: 2X MIRROR Gain
.MC4 : MIRROR bottom frequency selection bit
0: MIRROR Bottom Frequency Normal.
1: MIRROR Bottom Frequency Up.
.MC5 : MIRROR peak frequency selection bit
0: MIRROR Peak Frequency Normal
1: MIRROR Peak Frequency Up
.MC6 : Defect gain selection bit
0: Defect 1.5X Gain 1: Defect 2X Gain
.MC7 : Defect offset setting bit
0: Defect Offset Off 1: Defect Offset On

ADCKcmd (Address 59H)

The ADCKcmd command selects the operating frequency of A/D converter.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
ADCKcmd	59								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		TZCSEL	APCGAIN						ADCKS

.TZCSEL : Selects TZC usage
0: Analog TZC
1: Digital TZC
.APCGAIN : Selects APC Gain
0: Normal
1: Gain Down
.ADCKS : Selects ADC operating z frequency
0: 16.9344MHz
1: 8.4672MHz

RFBALcmd (Address 5AH)

The RFBALcmd command is for manual setting of TE balance and TES gain. TBAL[4:0] is only valid under RF test mode. (TEST[5:0] = 110101)

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RFBALcmd	5A								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		STSL1	STSL0		TBAL4	TBAL3	TBAL2	TBAL1	TBAL0

.STSL[1:0] : TES gain control
00/11: Normal
01: -2.5dB
10: 2.0dB
.TBAL[4:0] : Tracking balance control

TBAL[4:0]	MICOM COMMAND		GAIN[dB]
	DPRWcmd	RFBALcmd	
00000	800E 1C	0010 5A	1.781dB
00001	880E 1C	0011 5A	1.690dB
00010	900E 1C	0012 5A	1.561dB
00011	980E 1C	0013 5A	1.468dB
00100	A00E 1C	0014 5A	1.316dB
00101	A80E 1C	0015 5A	1.239dB
00110	B00E 1C	0016 5A	1.104dB
00111	B80E 1C	0017 5A	1.005dB
01000	C00E 1C	0018 5A	0.886dB
01001	C80E 1C	0019 5A	0.744dB
01010	D00E 1C	001A 5A	0.642dB
01011	D80E 1C	001B 5A	0.517dB
01100	E00E 1C	001C 5A	0.390dB
01101	E80E 1C	001D 5A	0.262dB
01110	F00E 1C	001E 5A	0.132dB
01111	F80E 1C	001F 5A	0.000dB

TBAL[4:0]	MICOM COMMAND		GAIN[dB]
	DPRWcmd	RFBALcmd	
10000	000E 1C	0000 5A	-0.134dB
10001	080E 1C	0001 5A	-0.247dB
10010	100E 1C	0002 5A	-0.386dB
10011	180E 1C	0003 5A	-0.526dB
10100	200E 1C	0004 5A	-0.693dB
10101	280E 1C	0005 5A	-0.790dB
10110	300E 1C	0006 5A	-0.962dB
10111	380E 1C	0007 5A	-1.112dB
11000	400E 1C	0008 5A	-1.316dB
11001	480E 1C	0009 5A	-1.420dB
11010	500E 1C	000A 5A	-1.552dB
11011	580E 1C	000B 5A	-1.713dB
11100	600E 1C	000C 5A	-1.877dB
11101	680E 1C	000D 5A	-2.044dB
11110	700E 1C	000E 5A	-2.210dB
11111	780E 1C	000F 5A	-2.340dB

In RF test mode, RFBALcmd can change TBAL values without clock(XI), but 1Ch command (DPRWcmd) should be used to change TBAL value manually in normal mode.

RFSTcmd (Address 5BH)

The RFSTcmd sets RF related parameters. No system clock is required.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RFSTcmd	5B								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		VISEL	SF2	RFB1	RFB0	LDON	PSTZCB	EQL1	EQL0

.VISEL : Pickup type selection bit
0: Voltage type
1: Current type

.SF2 : Speed X status. (Use this command for manual setting. In normal operation, a flag indicated the speed change should be generated from digital signal processing part.)
0: 1X
1: 2X

.RFB[1:0] : RF bias control bits
00: 0mV
01: Reserved
10: Lower RF bias by 120mV.
11: Lower RF bias by 240mV.

.LDON : LD on/off selection bit (This bit is valid under RF test mode. For the same operation under normal mode, either STPcmd or DPRWcmd could be used.)
0: off
1: on

.PSTZCB : TZC block enable/disable select
0: on
1: off

.EQL[1:0] : AGC level control
00: 1V
01: 1.1V
10: 1.2V
11: 1.3V

EFMScmd (Address 5CH)

The EFMScmd command selects signals from either analog block or digital block. No system clock is required for executing this command.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
EFMScmd	5C								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		MODEC	SPEAK	ONOFF	DONOFF		FOKS	DFCTS	MIRRS

.MODEC : Function enable to improve EFM performance
0: disable (off) 1: enable
.SPEAK : CPEAK detect select
0: disable 1: mute enable
.ONOFF : CPEAK block enable
0: disable 1: enable
.DONOFF : Focus/Tracking mute(average hold) enable
0: disable 1: mute enable
.FOKS : Analog/digital FOK block usage select
0: analog 1: digital
.DFCTS : Analog/digital DFCT block usage select
0: analog 1: digital
.MIRRS : Analog/digital MIRR block usage select
0: analog 1: digital

RFRWcmd (Address 5DH)

The RFRWcmd controls the RF and TE block gains to support CD-RW disc. No system clock is required for executing this command.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RFRWcmd	5D								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		RW3	RW2	RW1	RW0		RWT2	RWT1	RWT0

.RW3 : Resistor between RFN and RFO On/Off selection bit
0 : No Resistor between RFN and RFO
1 : 22K Resistor On between RFN and RFO

.RW[2:0] : RF gain control

000: 0.07dB	001: 3.96dB	010: 6.44dB	011: 8.52dB
100: 8.52dB	101: 10.20dB	110: 11.53dB	111: 12.76dB

.RWT[2:0] : TE gain control

000: 0.00dB	001: 3.47dB	010: 6.06dB	011: 7.97dB
100: 7.97dB	101: 9.53dB	110: 10.92dB	111: 12.06dB

RFIGcmd (Address 5EH)

The RFIGcmd command sets the input gain of FE/TE block. No system clock is required, but RF test mode setting is required.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
RFIGcmd	5E								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
			FG2	FG1	FG0		TG2	TG1	TG0

.FG[2:0] : Focus input gain control (Although the focus input gain can be controlled automatically by embedded DSP, this command is used to set focus input gain manually for testing.)

Focus input gain control	
D [6:4]	Gain inc. [dB]
000	0.00 [dB]
001	1.51[dB]
010	2.79[dB]
011	3.91[dB]
100	4.90[dB]
010	5.77[dB]
110	6.60[dB]
111	7.34[dB]

.TG[2:0] : Tracking input gain control (Although the tracking input gain can be controlled automaically by embedded DSP, this command is used to set tracking input gain manually for testing)

Tracking input gain control	
D [2:0]	Gain inc. [dB]
000	0.00 [dB]
001	1.72[dB]
010	3.15[dB]
011	4.38[dB]
100	5.46[dB]
010	6.42[dB]
110	7.28[dB]
111	8.07[dB]

TPWMcmd (Address 5FH)

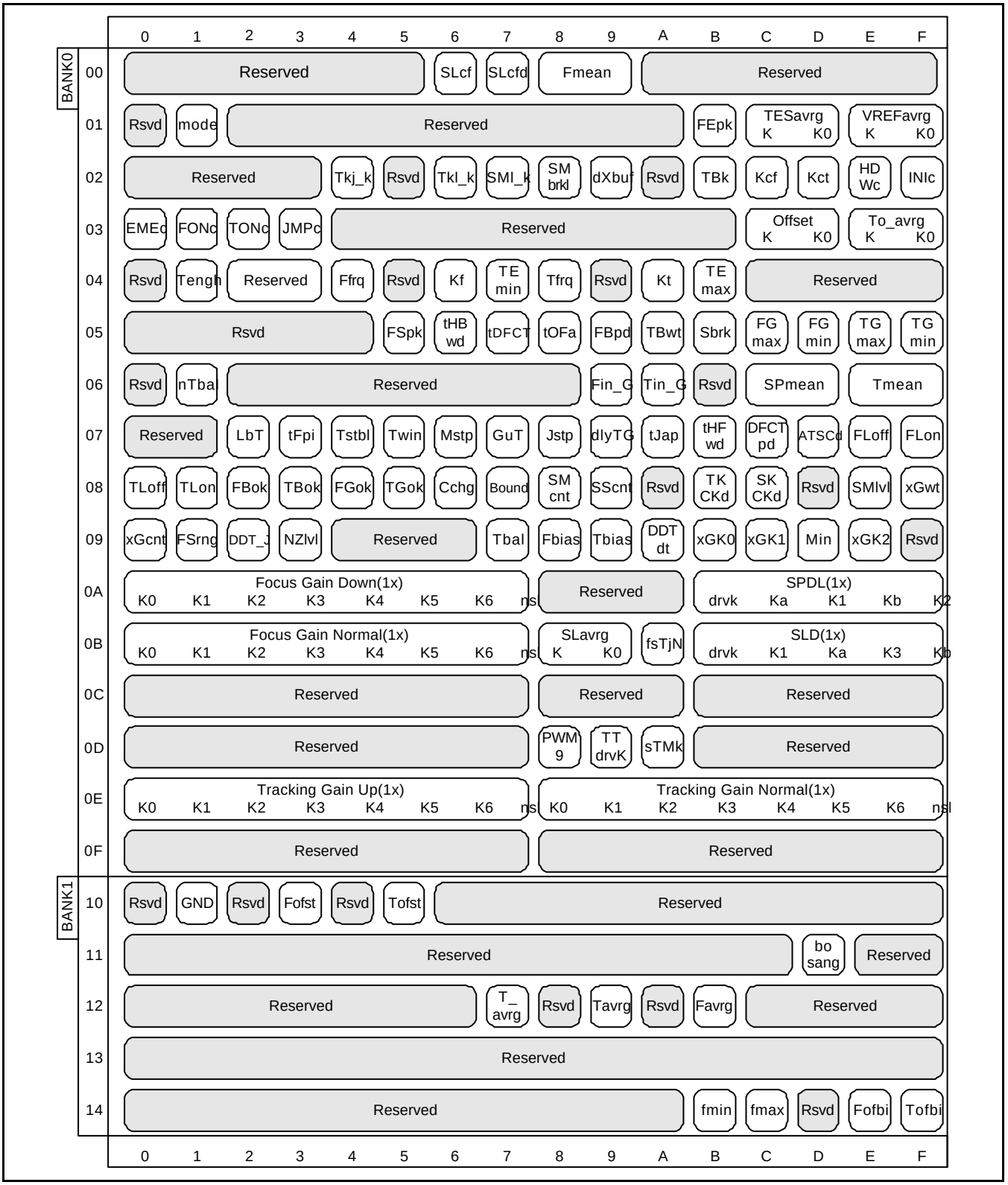
The TPWMcmd command tests the PWM part under the RF test mode. 8 bit digital input values can be set by this command.

Name	code	DH							
		D15	D14	D13	D12	D11	D10	D9	D8
TPWMcmd	5F								
		DL							
		D7	D6	D5	D4	D3	D2	D1	D0
		PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0

.PWM7 — PWM0 : 8bit input value setting bits

The set value of PWM[7:0] is sent to FODF/FODR, TRDF/TRDR, SLDF/SLDR and SPD, respectively. The PWM7 is inverted when it comes out via output pins.

Memory Map


0 1 2 3 4 5 6 7 8 9 A B C D E F
BANK0
00 Reserved SLcf SLcfd Fmean Reserved
01 Rsvd mode Reserved FEpk TESavrg K K0 VREFavrg K K0
02 Reserved Tkj_k Rsvd Tkl_k SMI_k SM brkl dXbuf Rsvd TBk Kcf Kct HD Wc INIc
03 EMEc FONc TONc JMPc Reserved Offset K K0 To_avrg K K0
04 Rsvd Tengn Reserved Ffrq Rsvd Kf TE min Tfrq Rsvd Kt TE max Reserved
05 Rsvd FSpk tHB wd tDFCT tOFa FBpd TBwt Sbrk FG max FG min TG max TG min
06 Rsvd nTbal Reserved Fin_G Tin_G Rsvd SPmean Tmean
07 Reserved LbT tFpi Tstbl Twin Mstp GuT Jstp dlyTG tJap tHF wd DFCT pd ATSCd FLoff FLon
08 TLoff TLon FBok TBok FGok TGok Cchg Bound SM cnt SScnt Rsvd TK CKd SK CKd Rsvd SMlvl xGwt
09 xGcnt FSrng DDT_J NZlvl Reserved Tbal Fbias Tbias DDT dt xGK0 xGK1 Min xGK2 Rsvd
0A Focus Gain Down(1x) K0 K1 K2 K3 K4 K5 K6 ns Reserved SPDL(1x) drvk Ka K1 Kb K2
0B Focus Gain Normal(1x) K0 K1 K2 K3 K4 K5 K6 ns SLavrg K K0 fsTjN SLD(1x) drvk K1 Ka K3 Kb
0C Reserved Reserved Reserved
0D Reserved PWM 9 TT drvK sTMk Reserved
0E Tracking Gain Up(1x) K0 K1 K2 K3 K4 K5 K6 ns Tracking Gain Normal(1x) K0 K1 K2 K3 K4 K5 K6 ns
0F Reserved Reserved
BANK1
10 Rsvd GND Rsvd Fofst Rsvd Tofst Reserved
11 Reserved bo sang Reserved
12 Reserved T_ avrg Rsvd Tavrg Rsvd Favrg Reserved
13 Reserved
14 Reserved fmin fmax Rsvd Fofbi Tofbi
0 1 2 3 4 5 6 7 8 9 A B C D E F

Memory Descriptions

* 8SB: 8th significant bit from LSB

Address	Parameter	Description	Default (HEX)	Value (value)	STEP/LSB (@2.4V)
0006	SLcf	Sled filter k1 coefficient pointer buffer	00BC	buff.	-
0007	SLcfd	Sled filter nsk coefficient pointer buffer	00BB	buff.	-
0008	Fmean-1	Focus average filter k0 coefficient	0060	coeff.	-
0009	Fmean	Focus average filter k1 coefficient	7FA0	coeff.	-
0011	Mode	Current operation mode	0000	buff.	-
001B	FEpk	Focus peak level	0000	0V	9.38mV/8SB*
001C	Emean-1	TES average filter k0 coefficient	0800	coeff.	-
001D	Emean	TES average filter k1 coefficient	7800	coeff.	-
001E	Rmean-1	Voltage reference average filter k0 coefficient	0800	coeff.	-
001F	Rmean	Voltage reference average filter k1 coefficient	7800	coeff.	-
0024	Tkj_k	K for accelerate in track jump	3D00	47.7%	0.78%/8SB*
0026	TKI_k	K for track brake level percentage of kick level	1000	26.2%	1.56%/8SB*
0027	SMI_k	K for sled move brake percentage of kick level	C000	-100%	0.78%/8SB*
0028	SMbrkl	Brake level when sled move	0008	0V	9.38mV/8SB*
0029	dXbuf	Initial delta X value for focus bias control	0C00	110mV	9.38mV/8SB*
002B	TBk	Track balance control feedback coefficient	0800	100%	12.5%/8SB*
002C	Kcf	Focus gain control feedback coefficient	4000	50%	0.78%/8SB*
002D	Kct	Track gain control feedback coefficient	4000	50%	0.78%/8SB*
002E	HDWc	Hardware flags command buffer	0008	flag	-
002F	INIc	Initialize flags command buffer	0041	flag	-
0030	EMEc	Emergency flags command buffer	004F	flag	-
0031	FONc	Focus on action and condition command buffer	0041	flag	-
0032	TONc	Tracking on action and condition command buffer	0032	flag	-
0033	JUMc	Jump action command buffer	0000	0trk	trk#1/LSB
003C	Ofst k0	Offset average filter new data gain (K0=1-K1)	0060	coeff.	-
003D	Ofst k1	Offset average filter old data gain	7FA0	coeff.	-
003E	Omean_1	TRD average filter k0 coefficient	0800	coeff.	-
003F	Omean	TRD average filter k1 coefficient	7800	coeff.	-
0041	Tehgh	Enough TE level at balance control	3000	450mV	9.38mV/8SB*
0044	Ffrq	Focus loop gain control target frequency (0dB)	0008	798.2Hz	(Ffrq/884) / 88.2kHz
0046	Kf	Ffrq+2 disturbance signal (sine wave) amplifier	0800	150mV	(2.4V*0.78%)/8SB*
0047	TEmin	TE minimum level buffer for balance control	0000	0V	9.38mV/8SB*

*8SB:8th significant bit from LSB (Continued)

Address	Parameter	Description	Default (HEX)	Value (value)	STEP/LSB (@2.4V)
0048	Tfrq	Tracking loop gain control target frequency (=0dB)	000B	1.1kHz	(Ffrq/884)*88.2kHz
004A	Kt	Tfrq+2 disturbance signal (sine wave) amplitude	1000	300mV	(2.4V*0.78%)/8LSB*
004B	Temax	TE maximum level buffer for balance control	0000	0V	9.38mV/8SB*
004F	unBal	Error unbalance judge level percentage	2003	25%	0.78%/8SB*
0055	FSpk	Focus search output level control (% of full swing)	4000	50%	0.78%/8SB*
0056	tHBwd	Sled backward move time after home in	1833	70ms	11.3us/LSB
0057	tDFCT	Tracking gain up protect proceeding time at lock off (after defect)	0800	23ms	11.3us/LSB
0058	tOFa	Offset accumulate time	0FF0	46.1ms	11.3us/LSB
0059	FBpd	TES measure period for focus bias control	0172	50ms	181.4ms/LSB
005A	TBwt	Setting time after tracking balance change	1000	46.3ms	11.3us/LSB
005B	Sbrk	Sled brake maximum time after sled move	2380	102.7ms	11.3us/LSB
005C	FGmax	Focus output gain (nsk) maximum limit	7000	coeff.	-
005D	FGmin	Focus output gain (nsk) minimum limit	0800	coeff.	-
005E	TGmax	Tracking output gain (nsk) maximum limit	7000	coeff.	-
005F	TGmin	Tracking output gain (nsk) minimum limit	0800	coeff.	-
0061	nTBal	TZC cycle number of tracking balance measuring	000A	10trk	trk#/LSB
0069	Fin_G	Focus input gain control	0000	0dB	refer to SPEC
006A	Tin_G	Tracking input gain control	0000	0dB	refer to SPEC
006C	SPmean_1	Spindle output average filter k0 coefficient	0060	coeff.	-
006D	SPmean	Spindle output average filter k1 coefficient	7FA0	coeff.	-
006E	Tmean_1	TE average filter k0 coefficient	0060	coeff.	-
006F	Tmean	TE average filter k1 coefficient	7FA0	coeff.	-
0072	LbT	Lense Brake time	0078	1.35ms	11.3us/LSB
0073	tFpi	Focus pull-in stable time	0014	226us	11.3us/LSB
0074	Tstbl	Track kick jump stable time	0000	0us	11.3us/LSB
0075	Twin	Track jump TZC balance time	000A	113us	11.3us/LSB
0076	Mstp	Interval stop margin time	0003	33.9us	11.3us/LSB
0077	GuT	Track gain up time	0400	11.6ms	11.3us/LSB
0078	Jstp	T_Kick stop detect interval time	0018	271us	11.3us/LSB
0079	dlyTG	TG_norm.dlay time from FG_norm.onto play	0200	5.5ms	11.3us/LSB
007A	tJaP	Jamp assist procedure time	024C	79.7ms	11.3us/LSB
007B	tHFwd	Sled backward move time after home in	0F00	43.3ms	11.3us/LSB

*8SB:8th significant bit from LSB (Continued)

Address	Parameter	Description	Default (HEX)	Value (value)	STEP/LSB (@2.4V)
007C	DFCTpd	DeFeCT recover delay time	0040	723us	11.3us/LSB
007D	ATSCd	AnTiShoCk recover delay time	0A52	29.8ms	11.3us/LSB
007E	FLoff	FLK off time	0172	4.4ms	11.3us/LSB
007F	FLon	FLK on time	000A	113us	11.3us/LSB
0080	TLoff	TLK off time	0001	11.3us	11.3us/LSB
0081	TLon	TLK on time	0100	2.9ms	11.3us/LSB
0082	FBok	FBa allowance	0400	± 36.0mV	9.38mV/8SB*
0083	TBok	TBa allowance	0400	± 36.0mV	9.38mV/8SB*
0084	FGok	FGa allowance	0080	± 4.68mV	36.6uV/LSB
0085	TGok	TGa allowance	0040	± 2.34mV	36.6uV/LSB
0086	Cchg	Track jump count select (Cout or TZC/MIRR)	0080	128trk	track#/LSB
0087	Bound	Boundary or sled move/track jump	0080	128trk	track#/LSB
0088	SMcnt	Sled move kick delay track # after track kick	0001	1trk	track#/LSB
0089	SScnt	Sled brake start count (left track # < SScnt)	0200	512trk	track#/LSB
008B	TKCKd	Track kick voltage level	1800	224.8mV	9.38mV/8SB*
008C	SKCKd	Sled kick voltage level	7000	1049mV	9.38mV/8SB*
008E	SMlvl	Sled move level on track kick jump	7000	1049mV	9.38mV/8SB*
008F	xGwt	Loop gain settling time	0018	24T	period#/LSB
0090	xGcnt	Accumulate times in loop gain adjustment	000A	10T	period#/LSB
0091	FSrng	Focus search range in focus drop	5000	737mV	9.38mV/8SB*
0092	DDT_J	Judge value for simple DDT	1000	225.1mV	9.38mV/8SB*
0093	NZlvl	Noise level for S-curve detection	0800	75.04mV	9.38mV/8SB*
0097	Tbal	Tracking balance data	0000	0V	36.6uV/LSB
0098	Fbias	Focus bias	0000	0V	36.6uV/LSB
0099	Tbias	Track bias	0000	0V	36.6uV/LSB
009A	DDTdt	DDT return data buffer	0000	0V	9.38mV/8SB*
009B	xGk0	BPF coefficient for loop gain control :k0	32CB	coeff.	-
009C	xGk1	BPF coefficient for loop gain control : k1	4D35	coeff.	-
009D	Min	BPF coefficient for loop gain control : min	8000	coeff.	-
009E	xGk2	BPF coefficient for loop gain control : k2	7E00	coeff.	-

*8SB:8th significant bit from LSB (Continued)

Address	Parameter	Description	Default (HEX)	Value (value)	STEP/LSB (@2.4V)
00A0	FEd0	Focus gain down filter coefficient k0 (x1)	0800	coeff.	-
00A1	FEd1	Focus gain down filter coefficient k1 (x1)	8000	coeff.	-
00A2	FEd2	Focus gain down filter coefficient k2 (x1)	4600	coeff.	-
00A3	FEd3	Focus gain down filter coefficient k3 (x1)	7EC6	coeff.	-
00A4	FEd4	Focus gain down filter coefficient k4 (x1)	7FEA	coeff.	-
00A5	FEd5	Focus gain down filter coefficient k5 (x1)	7E00	coeff.	-
00A6	FEd6	Focus gain down filter coefficient k6 (x1)	3B00	coeff.	-
00A7	FGdw	Focus gain down filter coefficient knsk (x1)	1000	coeff.	-
00AB	SPdrvk	Spindle filter coefficient knsk (x1)	2000	coeff.	-
00AC	SPca	Spindle filter coefficient ka (x1)	023B	coeff.	-
00AD	SPc1	Spindle filter coefficient k1 (x1)	7DC5	coeff.	-
00AE	SPcb	Spindle filter coefficient kb (x1)	17AF	coeff.	-
00AF	SPc2	Spindle filter coefficient k2 (x1)	6851	coeff.	-
00B0	FEn0	Focus gain normal filter coefficient k0 (x1)	0800	coeff.	-
00B1	FEn1	Focus gain normal filter coefficient k1 (x1)	8000	coeff.	-
00B2	FEn2	Focus gain normal filter coefficient k2 (x1)	4600	coeff.	-
00B3	FEn3	Focus gain normal filter coefficient k3 (x1)	7EE4	coeff.	-
00B4	FEn4	Focus gain normal filter coefficient k4 (x1)	7FD8	coeff.	-
00B5	FEn5	Focus gain normal filter coefficient k5 (x1)	7E00	coeff.	-
00B6	FEn6	Focus gain normal filter coefficient k6 (x1)	3B00	coeff.	-
00B7	FGn	Focus gain normal filter coefficient knsk (x1)	2000	coeff.	-
00B8	Lmean-1	Sled average filter coefficient k5 (x1)	0800	coeff.	-
00B9	Lmean	Sled average filter coefficient k1 (x1)	7800	coeff.	-
00BA	FsTjN	Forced brake control track number	0003	3trk	track#/LSB
00BB	SLdrvk	Sled filter coefficient knsk (x1)	3000	coeff.	-
00BC	SLc1	Sled filter coefficient k1 (x1)	7FFE	coeff.	-
00BD	SLca	Sled filter coefficient ka (x1)	0002	coeff.	-
00BE	SLc3	Sled filter coefficient k3 (x1)	77A4	coeff.	-
00BF	Slcb	Sled filter coefficient kb (x1)	010C	coeff.	-

*8SB:8th significant bit from LSB (Continued)

Address	Parameter	Description	Default (HEX)	Value (value)	STEP/LSB (@2.4V)
00D9	TTdrvk	SNSCcmd output filter gain coefficient	0000	coeff.	-
00DA	sTMk	Track brake interval detection window time	4000	50.0%*2	1.56%/8SB*
00DB	SLd2xk	Sled filter coefficient knsk (x1)	3000	coeff.	-
00DC	SLD2xc	Sled filter coefficient k1 (x1)	7FFE	coeff.	-
00DD	SL2xca	Sled filter coefficient ka (x1)	0002	coeff.	-
00DE	SL2xc3	Sled filter coefficient k3 (x1)	77A4	coeff.	-
00DF	SL2xcb	Sled filter coefficient kb (x1)	010C	coeff.	-
00E0	TEu0	Tracking gain up filter coefficient k0 (x1)	0800	coeff.	-
00E1	TEu1	Tracking gain up filter coefficient k1 (x1)	8000	coeff.	-
00E2	TEu2	Tracking gain up filter coefficient k2 (x1)	2996	coeff.	-
00E3	TEu3	Tracking gain up filter coefficient k3 (x1)	7FA0	coeff.	-
00E4	TEu4	Tracking gain up filter coefficient k4 (x1)	7FF2	coeff.	-
00E5	TEu5	Tracking gain up filter coefficient k5 (x1)	7BC0	coeff.	-
00E6	TEu6	Tracking gain up filter coefficient k6 (x1)	1782	coeff.	-
00E7	TGup	Tracking gain up filter coefficient knsk (x1)	44A2	coeff.	-
00E8	TEn0	Tracking gain normal filter coefficient k0 (x1)	0188	coeff.	-
00E9	TEn1	Tracking gain normal filter coefficient k1 (x1)	8000	coeff.	-
00EA	TEn2	Tracking gain normal filter coefficient k2 (x1)	54CB	coeff.	-
00EB	TEn3	Tracking gain normal filter coefficient k3 (x1)	7E76	coeff.	-
00EC	TEn4	Tracking gain normal filter coefficient k4 (x1)	7FF2	coeff.	-
00ED	TEn5	Tracking gain normal filter coefficient k5 (x1)	7DE0	coeff.	-
00EE	TEn6	Tracking gain normal filter coefficient k6 (x1)	430C	coeff.	-
00EF	TGn	Tracking gain normal filter coefficient knsk (x1)	3B00	coeff.	-

*8SB:8th significant bit from LSB (Continued)

Address	Parameter	Description	Default (HEX)	Value (value)	STEP/LSB (@2.4V)
1001	GND	Vref level offset average value	0000	0V	36.6uV/LSB
1003	Fofst	Focus offset average value	0000	0V	36.6uV/LSB
1005	Tofst	Focus offset average value	0000	0V	36.6uV/LSB
1027	T_avrg	Tracking output average data	0000	0V	36.6uV/LSB
1029	Tavrg	Tracking input average data	0000	0V	36.6uV/LSB
102B	Favrg	Focus input average data	0000	0V	36.6uV/LSB
104B	fmin	Minimum frequency for tracking balance control	00F6	358.5Hz	88.2kHz/fmin
104C	fmax	Maximum frequency for tracking balance control	0018	3.68kHz	88.2kHz/fmax
104E	Fofbi	Focus offset +bias value	0000	0V	36.6uV/LSB
104F	Tofbi	Tracking offset+bias value	0000	0V	36.6uV/LSB

CD-DSP/ESP/DBB MICRO-CONTROLLER COMMAND DESCRIPTIONS

60 Commands : DPLL setting commands(60h = 0110 0000)

Bit	Name	Function	Init.	Sense
D7	WIDE	Wide PLL mode selection 1 : Wide 0 : Normal	0	Z
D6	-		0	
D5	PGAIN	Phase Gain 1 : On 0 : Off	0	
D4	DLFGAIN	Digital loop filter gain 1 : 1/2^10 0 : 1/2^9	0	
D3	ROM1	ROM coefficient selection 1 : Accept ± 3T 0 : Ignore ± 3T	0	
D2	COAT	All T Correction 1 : All T 0 : Normal	0	
D1	-		0	
D0	RETREF	Reference when return to M1 = 98 1 : ± 2.28 % 0 : ± 1.14 %	0	

61 Commands : DPLL setting commands(62h = 0110 0001)

Bit	Name	Function	Init.	Sense
D[7:6]	REF98[1:0]	Outward reference when M1 = 98 00 : ± 1.71 % 01 : ± 2.28 % 10 : ± 3.41 % 11 : ± 4.55 %	11	Z
D[5:4]	REF[1:0]	Outward reference when M1 ≠ 98 00 : ± 1.71 % 01 : ± 2.28 % 10 : ± 3.41 % 11 : ± 4.55 %	11	
D[3:2]	MAXTGAIN[1:0]	MAX T accumulation gain 00 : 1 01 : 1/2 10 : 1/4 11 : 1/8	00	
D[1:0]	CAPRANGE[1:0]	Capture range selection 00 : 50% 01 : 40% 10 : 30% 11 :20%	00	

62 Commands : DPLL setting commands(62h = 0110 0010)

Bit	Name	Function	Init.	Sense
D[7:6]	DIVS1[1:0]	PLL1 post scaler 00 : ± 8 01 : ± 10 10 : ± 12 11 : ± 14	01	Z
D[5:0]	DIVP1[5:0]	PLL1 pre divider 0 — 63 (recommend range : 22 — 10)	010110	

64 Commands : DPLL setting commands(64h = 0110 0100)

Bit	Name	Function	Init.	Sense
D[7:0]	MITEST[7:0]	DPLL divider setting value	00000000	Z

65 Commands : DPLL setting commands(65h = 0110 0101)

Bit	Name	Function	Init.	Sense
D7	CMDSPLT	DPLL command setting method in case of speed change. 0 : Automatic setting when speed change command is performed. 1 : Manual DPLL setting required.	0	
D6	PONLY	Selects Phase Compensation Only 0 : Phase and Frequency Compensation 1 : Phase Compensation Only	0	
D[5:4]	MRANGE[1:0]	Setting Main Divider M value of PLL 00 : 50% 01 : 40% 10 : 30% 11 : 20%	00	Z
D3	FSREG	Confirm Frame sync (|Thigh-Tlow|<1) to calculate MAX T	0	
D2	PLLTEST	PLL Test mode 1 : Test (M1<=M2), 0 : Normal	0	
D1	PLLPWDN	PLL1 Power down mode 1 : Power down 0 : Normal	0	
D0	-		0	

70 Commands : DBB Related Commands (70h = 0111 0000)

Bit	Name	Function	Init.	Sense
D7	-	-	0	
D6	-	-	0	
D5	-	-	0	
D4	-	-	0	Z
D3	TST1	Test Flag 0 : Normal 1 : Test	0	
D2	-		0	
D[1:0]	MAX,DBB	DBB Mode Setting. 00 : DBB OFF 01 : MIN 10 : DBB OFF 11 : MAX	00	

80 Commands : Shock-proof memory system setting Commands (80h = 1000 0000)

Bit	Name	Function	Init.	Sense
D7	MSWREN	Encode sequence start On/Off 0 : Start OFF 1 : Start ON	0	
D6	MSWACL	Write Address Reset 0 : Reset release 1 : Reset	0	
D5	MSRDEN	Decode sequence start/stop 0 : Stop 1 : Start	0	
D4	MSRACL	Read address reset 0 : Reset release 1 : Reset	0	Z
D[3:2]	MSDCN[1:0]	11 : 3-pair comparison start 10 : 2-pair comparison start 01 : Direct connect start 00 : Connect operation stop	00	
D1	WAQV	Q Data valid. 0 : Not valid 1 : Valid	0	
D0	MSON	Memory system ON (When off, through mode, and attenuation is active) 0 : OFF 1 : ON	0	

83 Commands : Audio Control Related Commands 1(83h = 1000 0011)

Bit	Name	Function	Init.	Sense
D7	ATT	ESP Attenuate block On 1 : ON 0 : OFF	0	
D6	MUTE	Forced Mute 1 : ON 0 : OFF	0	
D5	SOFT	Soft Muting. Changes smoothly when On only. 1 : ON 0 : OFF	0	
D4	NS	Noise sharper function when encoding 1 : ON 0 : OFF	0	Z
D3	CMP12	12-bit comparison connect/16-bit comparison connect 1 : 12bit 0 : 15bit	0	
D2	-		0	
D1	-		0	
D0	-		0	

84 Commands : Digital attenuation level setting commands(84h = 1000 0100)

Bit	Name	Function	Init.	Sense
D7	K7	MSB 2^{-1}	0	Z
D6	K6	2^{-2}	1	
D5	K5	2^{-3}	0	
D4	K4	2^{-4}	0	
D3	K3	2^{-5}	0	
D2	K2	2^{-6}	0	
D1	K1	2^{-7}	0	
D0	K0	LSB 2^{-8}	0	

85 Commands : Option setting commands(85h = 1000 0101)

Bit	Name	Function	Init.	Sense
D[7:6]	RAMS[1:0]	DRAM type setting 00 : 1MDRAM(256kx4bit) x single 10 : 4MDRAM(1Mx4bit) x single 01 : 4MDRAM(1Mx4bit) x double 11 : 16MDRAM(4Mx4bit) x single	00	Z
D5	-		0	
D4	-		0	
D3	COMPFB	Full bit compression mode (High enable)	0	
D2	COMP6B	6bit compression mode (High enable)	1	
D1	COMP5B	5bit compression mode (High enable)	0	
D0	COMP4B	4bit compression mode (High enable)	0	

86 Commands : Digital Audio interface setting commands(86h = 1000 0110)

Bit	Name	Function	Init.	Sense
D[7:6]	CP[1:0]	Channel status and clock accuracy setting 00 : Level 2 (max ± 300 ppm) 01 : Level 3 (max ± 10%) 10 : Level 1 (max ± 50 ppm) 11 : Not supported	00	Z
D5	LBIT	Digital audio signal generation logic 0 : post recording software 1 : Unassigned	0	
D4	DIT	Digital audio interface(DIT) enable 0 : DIT output LOW 1 : H = DIT ON	0	
D3	-		0	
D2	-		0	
D1	-		0	
D0	-		0	

87 Commands : Subcode Q Data setting commands(87h = 1000 0111)

Bit	Name	Function	Init.	Sense
D11	QAD3	Q data setting and word address specification. QAD3(MSB) to QAD0(LSB) specify one of 10 valid addresses in the range 0000 to 1001 (If an address in the	1	
D10	QAD2	range 1010 to 1111 is specified, the data on QD7 to QD0	1	
D9	QAD1	is ignored. Note that writing to address 1001 also	1	
D8	QAD0	functions as the write stop command.)	1	
D7	QD7	MSB Q data setting word data	0	
D6	QD6	Q data setting word data	0	Z
D5	QD5	Q data setting word data	0	
D4	QD4	Q data setting word data	0	
D3	QD3	Q data setting word data	0	
D2	QD2	Q data setting word data	0	
D1	QD1	Q data setting word data	0	
D0	QD0	LSB Q data setting word data	0	

Address map for Q data setting buffer

QAD3	QAD2	QAD1	QAD0	QD7	QD6	QD5	QD4	QD3	QD2	QD1	QD0
0	0	0	0	CTL0	CTL1	CTL2	CTL3	ADR3	ADR2	ADR1	ADR0
0	0	0	1	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8
0	0	1	0	DQ9	DQ10	DQ11	DQ12	DQ13	DQ14	DQ15	DQ16
0	0	1	1	DQ17	DQ18	DQ19	DQ20	DQ21	DQ22	DQ23	DQ24
0	1	0	0	DQ25	DQ26	DQ27	DQ28	DQ29	DQ30	DQ31	DQ32
0	1	0	1	DQ33	DQ34	DQ35	DQ36	DQ37	DQ38	DQ39	DQ40
0	1	1	0	DQ41	DQ42	DQ43	DQ44	DQ45	DQ46	DQ47	DQ48
0	1	1	1	DQ49	DQ50	DQ51	DQ52	DQ53	DQ54	DQ55	DQ56
1	0	0	0	DQ57	DQ58	DQ59	DQ60	DQ61	DQ62	DQ63	DQ64
1	0	0	1	DQ65	DQ66	DQ67	DQ68	DQ69	DQ70	DQ71	DQ72

90 Commands (MICRO-CONTROLLER read): Shock-proof memory status(1) (90h = 1001 0000)

Bit	Name	Function	Init.	Sense
S7	FLAG6	Signal processor IC jitter margin exceeded 1 : Exceeded 0 : Not exceeded	0	
S6	MSOVF	Write overflow (Read once only when RA exceeds WA) 1 : DRAM overflow 0 : Not overflow	0	
S5	BOVF	Input buffer memory overflow because sampling rate of input data is too fast 1 : Input buffer memory overflow	0	
S4	-		0	
S3	DCOMP	Data compare-connect sequence operating 1 : Compare-connect sequence operating	0	
S2	MSWIH	Encode sequence stop due to internal factors 1 : Encoding stopped	0	
S1	MSRIH	Decode sequence stop due to internal factors 1 : Decoding stopped	0	
S0	-		0	

*S7 — S0 DATA ARE MSB FIRST

91 Commands (MICRO-CONTROLLER read): Shock-proof memory status(2) (91h = 1001 0001)

Bit	Name	Function	Init.	Sense
S7	MSEMP	Valid data empty state (Always HIGH when RA exceeds VWA) 1 : No valid data	0	
S6	OVFL	Write overflow state (Always HIGH when WA exceeds RA) 1 : Memory Full	0	
S5	ENCOD	Encode sequence operating state 1 : Encoding 0 : No operation	0	
S4	DECOD	Decode sequence operating state 1 : Decoding 0 : No operation	0	
S3	QRDY	Subcode Q data write-buffer write enable 1 : Write enable 0 : Write disable	0	
S2	-		0	
S1	-		0	
S0	-		0	

92 Commands (MICRO-CONTROLLER read): Shock-proof memory valid data residual(92h = 1001 0010)

Bit	Name	Function	Init.	Sense
S7	AM21	Valid data accumulated VWA-RA (MSB) 8M bits	0	
S6	AM20	4M bits	0	
S5	AM19	2M bits	0	
S4	AM18	1M bits	0	
S3	AM17	512k bits	0	
S2	AM16	256k bits	0	
S1	AM15	128k bits	0	
S0	AM14	64k bits	0	
M1	AM13	32k bits	0	
M2	AM12	16k bits	0	
M3	AM11	8k bits	0	
M4	AM10	4k bits	0	
M5	AM09	2k bits	0	
M6	AM08	1k bits	0	
M7	AM07	512 bits	0	
M8	AM06	256 bits	0	

93 Commands (MICRO-CONTROLLER read): Reserved for read commands (93h = 1001 0011)

Reserved for later use.

A0 Commands : CDDSP Function control(A0h = 1010 0000)

Bit	Name	Function	Init.	Sense
D7	CDROM	CDROM mode ON/OFF 1 : CDROM mode 0 : CDP mode	0	Z
D6	ESPEN	ESP enable 1 : ESP enable 0 : ESP disable	0	
D5	DEEM	De-emphasis ON/OFF 1 : De-emphasis ON 0 : De-emphasis OFF	1	
D4	ERAOFF	Erasure correction ON/OFF 1 : Erasure OFF 0 : Erasure ON	0	
D3	C1PNT	C1 pointer Set/Reset control when C1 2 Error correction 1 : C1PNT reset 0 : C1PNT set	0	
D2	DBBON	DBB module ON/OFF 1 : ON 0 : OFF	0	
D1	EMPHSEL	EMPH source selection 1 : External EMPH 0 : Internal EMPH	0	
D0	JITM	Copy RBC (Read Base Counter) value to WBC (Write Base Counter) value if JITM is high and AMUTE is On.	0	

A1 Commands : Frame sync related function control(A1h = 1010 0001)

Bit	Name	Function	Init.	Sense
D[7:6]	FSEL[1:0]	Sync Frame control selection for Frame sync protection /insertion 00 : 2 frames 01 : 4 frames 10 : 8 frames 11 : 13 frames	00	GFS
D[5:4]	WSEL[1:0]	Window width selection for Frame sync protection / insertion 00 : ± 3 01 : ± 7 10 : ± 13 11 : ± 26	00	
D[3:2]	FSMD	Frame sync detection method setting 00 : Pattern detection method 01 : Frequency compensation detection method 10 : Period 1 11 : Period 2	0	
D1	-		0	
D0	-		0	

A2 Commands : CDDSP Mode control (A2h = 1010 0010)

Bit	Name	Function	Init.	Sense
D7	PWRDNL	FULL LSI Power down. Change to power save mode when STOP 1 : Power down OFF 0 : Power down ON	1	
D6	ESPDN	ESP only power down 1 : ESP power down ON 0 : ESP power down OFF	0	
D5	SVOPDL	Servo part power down (Low active) 1 : Power down OFF 0 : Power down ON	1	
D4			0	Z
D3	CLVEMERG	ECLV ON/OFF 1 : ON 0 : OFF	0	
D2	EMERGP	ECLV_PD ON/OFF 1 : ON 0 : OFF	0	
D1	NCLV	1 : CLV phase servo activated by frame sync 0 : CLV phase servo activated by base counter	0	
D0	CRCQ	Q data CRC result(SQOK) included ON/OFF 0 : SQDT does not include SQOK 1 : SQDT is SQOK when S0S1 = H	1	

A3 Commands : CDDSP Mode control (A3h = 1010 0011)

Bit	Name	Function	Init.	Sense
D7	EFMSEL	EFM source selection 1 : External EFM source 0 : EFM from RF block	0	
D6	-			
D5	-		0	
D4	-		0	Z
D3	-		0	
D2	-		0	
D1	YFLAG	YFLAG source selection 1 : Jitter and Anti-shock 0 : Jitter only	0	
D0	JTFRV	Use VCO1 clock for processing data	0	

A8 Commands : Output ON/OFF Control(1) (A8h = 1010 1000)

Bit	Name	Function	Init.	Sense
D7	-		0	
D6	PLCKMUTE	PLCK output 1 : OFF 0 : ON	0	
D5	-		0	
D4	WFCKMUTE	WFCK output 1 : OFF 0 : ON	0	
D3	-		0	Z
D2	DAOMUTE	Digital Output 1 : OFF 0 : ON	0	
D1	SBDTMUTE	Subcode data output 1 : OFF 0 : ON	0	
D0	C4MMUTE	MICRO-CONTROLLER clock(C4M) output 1 : OFF 0 : ON	0	

A9 Commands : Output ON/OFF Control(2) (A9h = 1010 1001)

Bit	Name	Function	Init.	Sense
D7	-		0	
D[6:4]	MNTSEL[2:0]	Monitoring signal selection (Refer below table)	000	
D3	-		0	
D2	-		0	Z
D1	SC[1:0]	Calibration Range Scale Control Inputs 00 : Normal 01 : 2X Range	0	
D0		10 : 4X Range 11 : 0.5X Range	0	

MNTSEL table

Bit Name	Output Description					
MNTSEL[2:0]	SADT	LRCK	BCK	C2PO	RFCK	JITB
000	SADT	LRCK	BCK	C2PO	RFCK	YFLAG
001	FSYNC	FSDW	ECFL3	ECFL2	ECFL1	ECFL0
010	FSYNC	FSDW	ULKFS	EMPH	SQOK	TIM2
011	ESP_SADT	ESP_LRCK	ESP_BCK	DSP_BCK	DSP_LRCK	DSP_SADT
100	Fchange	DIVM98	DIVNFAST	AT2T	EFMIN	EFMOUT
101	DIVM1[5]	DIVM1[4]	DIVM1[3]	DIVM1[2]	DIVM1[1]	DIVM1[0]
110	DBB_SADT	DBB_LRCK	DBB_BCK	DAC_BCK	DAC_LRCK	DAC_SADT
111	0	0	0	0	0	0

AA Commands : Output ON/OFF Control(3) (AAh = 1010 1010)

Bit	Name	Function	Init.	Sense
D7	-	No Operation	0	Z
D6	-	No Operation	0	
D5	-	No Operation	0	
D4	-	No Operation	0	
D3	FREQS[3:0]	Sampling Frequency Information for digital out 0000 : 44.1 kHz	0	
D2		0100 : 48 kHz	0	
D1		1100 : 32 kHz	0	
D0		10XX, 00XX, 01XX, 11XX : Reserved	0	

AB Commands : Audio Control Related Commands 2 (ABh = 1010 1011)

Bit	Name	Function	Init.	Sense
D7	AMUTE	Audio mute 1 : ON 0 : OFF	1	S0S1
D6	ZCMT	Zero cross muting (valid when AMUTE = 1) 1 : ON 0 : OFF	0	
D5	-	-	0	
D4	ATTN	Audio 1/4 attenuation 1 : ON 0 : OFF	0	
D3	-	-	0	
D2	-	-	0	
D1	DATXMUTE	Force input data to DIGOUT block as all zero. 1 : ON 0 : OFF	0	
D0	DACMUTE	Sigma-Delta DAC audio input data mute 1 : ON 0 : OFF	1	

B0 Commands : Reserved for Test Mode Selection(1) (B0h = 1011 0000)
Caution ! : No Operation for Current Use. Use Pin to set Test Modes.

Bit	Name	Function	Init.	Sense
D7	DION	External Data input on/off 1 : ON 0 : OFF	0	
D6			0	
D5	TMODE5	TEST MODE selection (See below table)	0	
D4	TMODE4	TEST MODE selection (See below table)	0	Z
D3	TMODE3	TEST MODE selection (See below table)	0	
D2	TMODE2	TEST MODE selection (See below table)	0	
D1	TMODE1	TEST MODE selection (See below table)	0	
D0	TMODE0	TEST MODE selection (See below table)	0	

TMODE5	TMODE4	TMODE3	TMODE2	TMODE1	TMODE0	Test Mode
1	0	1	0	0	0/1	Full chip logic scan test mode
1	0	1	0	1	0	SSP boundary scan mode
1	0	1	0	1	1	NAND Tree test mode
1	0	1	1	0	0	BIST mode
1	0	1	1	0	1	-
1	0	1	1	1	0	Audio DAC vector test (+ BIST)
1	0	1	1	1	1	Audio DAC analog test
1	1	0	0	0	0	VCO test
1	1	0	0	0	1	DPLL test
1	1	0	0	1	0	DC Test
1	1	0	0	1	1	CDDSP function test mode
1	1	0	1	0	0	-
1	1	0	1	0	1	RF Test Mode
1	1	0	1	1	0	ADC Test Mode
1	1	0	1	1	1	NPC ESP Test mode 0
1	1	1	0	0	0	NPC ESP Test mode 1
1	1	1	0	0	1	NPC ESP Test mode 2
1	1	1	0	1	0	NPC ESP Test mode 3
1	1	1	0	1	1	NPC ESP Test mode 4
1	1	1	1	0	0	NPC ESP Test mode 5
1	1	1	1	0	1	NPC ESP Test mode 6
1	1	1	1	1	0	DBB Audio Out Test
1	1	1	1	1	1	DBB core coefficient monitoring
Otherwise						Normal Play Mode

C0 Commands : Audio DAC Digital Attenuation (C0h = 1100 0000)

Bit	Name	Function	Init.	Sense
D7			0	
D6			0	
D5	DATTN5	Digital Attenuation control MICRO-CONTROLLER data : M5	0	
D4	DATTN4	Digital Attenuation control MICRO-CONTROLLER data : M4	0	Z
D3	DATTN3	Digital Attenuation control MICRO-CONTROLLER data : M3	0	
D2	DATTN2	Digital Attenuation control MICRO-CONTROLLER data : M2	0	
D1	DATTN1	Digital Attenuation control MICRO-CONTROLLER data : M1	0	
D0	DATTN0	Digital Attenuation control MICRO-CONTROLLER data : M0	0	

Caution : Please be careful on choosing MICRO-CONTROLLER Data, because the data are not sorted by ascending order.

MDATA	Attenuation Level (dB)	MDATA	Attenuation Level (dB)
MSB — LSB LSB — MSB ID7 — ID0 M0 M1 M2 M3 M4 M5		MSB — LSB LSB — MSB ID7 — ID0 M0 M1 M2 M3 M4 M5	
IDNUM<7:0> 0 0 0 0 0 0	0	IDNUN<7:0> 1 0 0 0 0 0	-6.30
IDNUM<7:0> 0 0 0 0 0 1	-0.28	IDNUN<7:0> 1 0 0 0 0 1	-6.58
IDNUM<7:0> 0 0 0 0 1 0	-0.42	IDNUN<7:0> 1 0 0 0 1 0	-6.88
IDNUM<7:0> 0 0 0 0 1 1	-0.56	IDNUN<7:0> 1 0 0 0 1 1	-7.18
IDNUN<7:0> 0 0 0 1 0 0	-0.71	IDNUN<7:0> 1 0 0 1 0 0	-7.50
IDNUN<7:0> 0 0 0 1 0 1	-0.86	IDNUN<7:0> 1 0 0 1 0 1	-7.82
IDNUN<7:0> 0 0 0 1 1 0	-1.01	IDNUN<7:0> 1 0 0 1 1 0	-8.16
IDNUN<7:0> 0 0 0 1 1 1	-1.16	IDNUN<7:0> 1 0 0 1 1 1	-8.52
IDNUN<7:0> 0 0 1 0 0 0	-1.32	IDNUN<7:0> 1 0 1 0 0 0	-8.89
IDNUN<7:0> 0 0 1 0 0 1	-1.48	IDNUN<7:0> 1 0 1 0 0 1	-9.28
IDNUN<7:0> 0 0 1 0 1 0	-1.64	IDNUN<7:0> 1 0 1 0 1 0	-9.68
IDNUN<7:0> 0 0 1 0 1 1	-1.80	IDNUN<7:0> 1 0 1 0 1 1	-10.10
IDNUN<7:0> 0 0 1 1 0 0	-1.97	IDNUN<7:0> 1 0 1 1 0 0	-10.55
IDNUN<7:0> 0 0 1 1 0 1	-2.14	IDNUN<7:0> 1 0 1 1 0 1	-11.02
IDNUN<7:0> 0 0 1 1 1 0	-2.32	IDNUN<7:0> 1 0 1 1 1 0	-11.51
IDNUN<7:0> 0 0 1 1 1 1	-2.50	IDNUN<7:0> 1 0 1 1 1 1	-12.04
IDNUN<7:0> 0 1 0 0 0 0	-2.68	IDNUN<7:0> 1 1 0 0 0 0	-12.60
IDNUN<7:0> 0 1 0 0 0 1	-2.87	IDNUN<7:0> 1 1 0 0 0 1	-13.20
IDNUN<7:0> 0 1 0 0 1 0	-3.06	IDNUN<7:0> 1 1 0 0 1 0	-13.84
IDNUN<7:0> 0 1 0 0 1 1	-3.25	IDNUN<7:0> 1 1 0 0 1 1	-14.54
IDNUN<7:0> 0 1 0 1 0 0	-3.45	IDNUN<7:0> 1 1 0 1 0 0	-15.30
IDNUN<7:0> 0 1 0 1 0 1	-3.66	IDNUN<7:0> 1 1 0 1 0 1	-16.12
IDNUN<7:0> 0 1 0 1 1 0	-3.87	IDNUN<7:0> 1 1 0 1 1 0	-17.04
IDNUN<7:0> 0 1 0 1 1 1	-4.08	IDNUN<7:0> 1 1 0 1 1 1	-18.06
IDNUN<7:0> 0 1 1 0 0 0	-4.30	IDNUN<7:0> 1 1 1 0 0 0	-19.22
IDNUN<7:0> 0 1 1 0 0 1	-4.53	IDNUN<7:0> 1 1 1 0 0 1	-20.56
IDNUN<7:0> 0 1 1 0 1 0	-4.76	IDNUN<7:0> 1 1 1 0 1 0	-22.14
IDNUN<7:0> 0 1 1 0 1 1	-5.00	IDNUN<7:0> 1 1 1 0 1 1	-24.08
IDNUN<7:0> 0 1 1 1 0 0	-5.24	IDNUN<7:0> 1 1 1 1 0 0	-26.58
IDNUN<7:0> 0 1 1 1 0 1	-5.49	IDNUN<7:0> 1 1 1 1 0 1	-30.10
IDNUN<7:0> 0 1 1 1 1 0	-5.75	IDNUN<7:0> 1 1 1 1 1 0	-36.12
IDNUN<7:0> 0 1 1 1 1 1	-6.02	IDNUN<7:0> 1 1 1 1 1 1	- ∞

C1 Commands : Audio DAC Control (C1h = 1100 0001)

Bit	Name	Function	Init.	Sense
D7	ZDENL	Zero input detection enables. 0 : Enable 1 : Disable	0	Z
D6	-		0	
D5	FSSEL1	De-emphasis sampling frequency mode selects. FSSEL<1:0>	0	
D4	FSSEL0	00 : 44.1kHz 01 : 48kHz 10 : 32kHz 11 : 48kHz	0	
D3	DACCLK	Audio DAC system clock selection 0 : internal 1 : external	0	
D2	-		0	
D1	BISTONP	Audio DAC Memory BIST test mode	0	
D0	TSEL	Test Pin for analog post-filter input enable (H)	0	

E0 Commands : CLV Gain (E0h = 1110 0000)

Bit	Name	Function	Init.	Sense
D7	-		0	Z
D6	WBN	Controls bottom hold period at CLV speed mode 0 : Change depends on WB 1 : RFCK/64	0	
D5	WPN	Controls peak hold period at CLV speed mode 0 : Change depends on WP 1 : RFCK/8	0	
D4	RFCKSEL	Selects RFCK source (always use X'tal clock) 0 : Normal 1 : Jitter free mode	0	
D3	-		0	
D2	WB	Bottom Hold frequency Setting at CLV speed mode 1 : RFCK/16 0 : RFCK/32	1	
D1	WP	Peak Hold frequency Setting at CLV speed mode 1 : RFCK/2 0 : RFCK/4	1	
D0	GAIN	Output Gain of SMDS setting at CLV speed mode 1 : 0 dB 0 : -12 dB	1	

E1 Commands : CLV Mode (E1h = 1110 0001)

Bit	Name	Function	Init.	Sense
D[7:6]	UNLOCK	Selects low period of LKFS (change LOCK high to low) 00 : GFS is LOW for 128 frames, then LOCK goes to LOW 01 : GFS is LOW for 112 frames, then LOCK goes to LOW 10 : GFS is LOW for 96 frames, then LOCK goes to LOW 11 : GFS is LOW for 80 frames, then LOCK goes to LOW	0	
D5	CLVIDLE	Make CLV idle. 0 : Normal 1 : IDLE	0	
D4	PCEN	SMDS Phase control enable 1 : Enable 0 : Disable	0	/CLVST
D3	CM3	Refer to the CLV mode table below	0	
D2	CM2		0	
D1	CM1		0	
D0	CM0		0	

CLV Mode Table

Mode		D3¾D0	SMDP	SMDS	SMEF	SMON	Function
KICK	Forward	1 0 0 0	H	Hi-Z	L	H	spindle motor forward mode
BRAKE	Reverse	1 0 1 0	L	Hi-Z	L	H	spindle motor reverse mode
CLV-S	Speed	1 1 1 0	Speed	Hi-Z	L	H	rough servo mode at start up
CLV-P	Phase	1 1 1 1	Phase	Phase	Hi-Z	H	PLL servo mode
CLV-A	XPHSP	0 1 1 0	Speed Phase	Hi-Z Phase	L Hi-Z	H	normal play mode (If LOCK='H', CLV-P, otherwise CLV-S)
CLV-A'	VPHSP	0 1 0 1	Speed Phase	Hi-Z Phase	L Hi-Z	H	automatic servo mode (If LOCK= 'H' or GFS= 'H', CLV-P, otherwise CLV-S')
STOP	Stop	0 0 0 0	L	Hi-Z	L	L	spindle motor stop mode

E2 Commands : CLV Control (E2h = 1110 0010)

Bit	Name	Function	Init.	Sense
D7	STRIO	Tri-state out enable in phase mode 1 : Tri-state 0 : PWM	0	Z
D6	SMM	SMDS mask limit manual setting enable 1 : Manual setting 0 : Auto setting	0	
D5	PME	SMDP mask enable 1 : Enable 0 : Disable	0	
D4	SME	SMDS mask enable (dead zone enable) 1 : Enable 0 : Disable	0	
D[3:2]	PCKSEL[1:0]	MDP resolution clock selection 00 : CLK4M_CLV/2 01 : CLK4M_CLV/4 10 : CLK4M_CLV/8 11 : CLK4M_CLV/16	00	
D[1:0]	PGAIN[1:0]	SMDP gain setting 00 : 1 01 : 1/2 10 : 1/4 11 : 1/8	00	

E3 Commands : CLV Control (E3h = 1110 0011)

Bit	Name	Function	Init.	Sense
D7	LC	Lock control 1 : 1x -> 2x or 2x -> 1x then LOCK is forced to 0 0 : Normal LOCK control	0	Z
D6	PML	MDP mask limit 1 : SMDP mask for SMDS error center value ¡¾50% 0 : SMDP mask for SMDS error center value ±25%	0	
D[5:4]	SML[1:0]	MDS mask limit (dead zone area) at MDS error center value 00 : ± 0% 01 : ± 6.25% 10 : ± 12.25% 11 : ± 25%	00	
D3	POS	MDP output selection 1 : Gain controlled SMDP 0 : Normal SMDP	0	
D[2:0]	SGAIN[2:0]	SMDS Gain setting 000 : 1 001 : 2 010 : 4 011 : 8 100 : 16 101 : 32 110 : 64 111 : 128	000	

E4 Commands : CLV Control (E4h = 1110 0100)

Bit	Name	Function	Init.	Sense
D[7:0]	POFFSET[7:0]	POFFSET[7] : SMDP offset sign 1 : minus (-) 0 : plus (+) POFFSET[6:0] : SMDP offset absolute value	7b'0	Z

E5 Commands : CLV Control (E0h = 1110 0101)

Bit	Name	Function	Init.	Sense
D7	SPLUS	SMDS offset plus enable 1 : Enable 0 : Disable	0	Z
D6	SDD	SMDS speed down control disable 1 : Disable ON 0 : Disable OFF(Enable)	0	
D[5:4]	PHASEDIV[1:0]	Phase comparator period setting 00 : RFCK/2 01 : RFCK/4 10 : RFCK/8 11 : RFCK/16	00	
D[3:0]	SMOFFSET[3:0]	SMDS mask limit value 0000 — 1111	0000	

E6 Commands : CLV Control (E6h = 1110 0110)

Bit	Name	Function	Init.	Sense
D[7:0]	SOFFSET[7:0]	SMDS Offset value If SPLUS = 1, SMDS output = SMDS error + SOFFSET where SPLUS is D7 of E5h command	7'b0	Z

F0 Commands : PLAY Control Setting (E0h = 1111 0000)

Bit	Name	Function	Init.	Sense
D7	-	-	0	Z
D6	-	-	0	Z
D5	-	-	0	Z
D4	-	-	0	Z
D3	-	-	0	Z
D2	DASPEED	Sigma-Delta DAC speed control 1 : Double speed 0 : Normal speed	0	Z
D[1:0]	DS[1:0]	Speed Setting 00 : Normal speed 11 : Double speed 01/10 : Double speed if ESPEN = 1, otherwise normal speed.	00	Z

SUPPLEMENTARY INFORMATION FOR ESP AND DBB PART

Caution : It is only the case of FUNCNTL($A0) ESPEN=1 that this command section is effective.

Write command supplementary information

80 : Shock-proof memory system setting Commands(80h = 1000 0000)

Name	Code	DL7	DL6	DL5	DL4	Init
ESPMS	80	MSWREN	MSWACL	MSRDEN	MSRACL	00h
		DL3	DL2	DL1	DL0	
		MSDCN1	MSDCN0	WAQV	MSON	

.MSWREN :
"0": Encode sequence stops
"1": Encode sequence starts
Invalid when MSON is not 1 within the same 80H command
Invalid when FLAG6=1
Invalid when OVFL=1
Invalid when a compare-connect start command (MSDCN2=1 or MSDCN1=1) occurs simultaneously
Direct connect if a compare-connect sequence is already operating

.MSWACL :
"0": No operation
"1": Initializes the write address (WA)

.MSRDEN :
"0" : Decode sequence stops
"1" : Decode sequence starts
Does not perform decode sequence if MSON=1.If there is no valid data, decode sequence temporarily stops. But, because the MSRDEN flag setting is maintained as is, the sequence automatically re-starts when valid data appears.

.MSRACL :
"0" : No operation
"1" : Initializes the read address (RA)

.MSDCN2 .MSDCN1 :
0 0 : Compare-connect sequence stops. No operation if a compare-connect sequence is not operating.
0 1 : Direct connect sequence starts
1 0 : 2-pair compare-connect sequence starts
1 1 : 3-pair compare-connect sequence starts

.WAQV :
"0" : No operation
"1" : The immediately preceding YBLKCK falling-edge timing WA (write address) becomes the VWA (valid write address).

.MSON :
"0" : Memory system turns OFF and through-mode playback starts. (In this mode, the attenuator is still active.)
"1" : Memory system turns ON and shock-proof operation starts

83 : Audio control related 1 Commands(83h = 1000 0011)

Name	Code	DL7	DL6	DL5	DL4	INIT
AUDCNTL1	83	ATT	MUTE	SOFT	NS	00h
		DL3	DL2	DL1	DL0	
		CMP12				

.ATT (attenuator enable) :

"0" : Attenuator settings become inactive, and output continues without attenuation

"1" : Attenuator settings become active (84H command)

.MUTE (forced muting) :

"0" : No muting(note 1)

"1" : Outputs are instantaneously muted to 0.

Effective at the start of left-channel output data.

.SOFT (soft muting) :

"0" : No muting.

Soft mute release occurs instantaneously to either the value set by the 84H command (When ATT=1) or 0dB (When ATT=0)

"1" : Outputs are smoothly muted to 0.

MUTE, SOFT relationship

When all mute inputs are 0, mute is released.

.NS (noise shaper enable) :

"0" : Performs comparison connection using all 16 bits of input data.

"1" : Includes noise shaper function in compression-mode shockproof operation.

.CMP12 (12-bit comparison connection) :

"0" : Performs comparison connection using all 16 bits of input data.

"1" : Performs comparison connection using only the most significant 12 bits of input data.

84 : Attenuation level setting Commands(84h = 1000 0100)

Name	Code	DL7	DL6	DL5	DL4	INIT
ATTLEVEL	84	K7	K6	K5	K4	40h
		DL3	DL2	DL1	DL0	
		K3	K2	K1	K0	

.K7(MSB) to .K0(LSB) (Attenuation coefficient bits)

The gain (dB) is given from the set value (Datt) by the following equation.
Gain = 20 x log(Datt/256) [dB]; left and right channels
For the maximum attenuation register set value (Datt = 255), the corresponding gain is -0.03 dB. But when the ATT flag is 0 (Datt = 256), there is no attenuation.

After a system reset initialization, the attenuation register is set to 64 (-12 dB). However, because the ATT flag is reset to 0, there is no attenuation.

When the attenuation register setting changes or when the ATT flag changes, the gain changes smoothly from the previous set gain towards the new set value. If a new value for the attenuation level is set before the previously set level is reached, the gain changes smoothly towards the latest setting.

The gain changes at a rate of 4 x (1/fs) per step. A full-scale change (255 steps) takes approximately 23.3 ms .

85 : Option setting Commands(85h = 1000 0101)

Name	Code	DL7	DL6	DL5	DL4	INIT
OPTIONSET1	85	RAMS1	RAMS2			04h
		DL3	DL2	DL1	DL0	
		COMPFB	COMP6B	COMP5B	COMP4B	

.RAMS1 .RAMS2 :

0 0 : 1M DRAMs (256k x 4 bits)x single
0 1 : 4M DRAMs (1M x4 bits)x double
1 0 : 4M DRAMs (1M x4 bits)x single
1 1 : 16M DRAMs (4M x4 bits)x single

.COMPFB .COMP6B .COMP5B .COMP4B:

0 0 0 1: Selects 4-bit compression mode
0 0 1 0: Selects 5-bit compression mode
0 1 0 0: Selects 6-bit compression mode
1 0 0 0: Selects full-bit compression mode

In all other cases: Selects 6-bit compression mode
Changing mode without initializing during operation is possible.

86 : ESP block digital audio interface setting Commands(86h = 1000 0110)

Name	Code	DL7	DL6	DL5	DL4	INIT
DAUDIF	86	CP1	CP2	LBIT	DIT	00h
		DL3	DL2	DL1	DL0	

.CP1 .CP2 (channel status and clock accuracy setting)

0 0 : Level 2 (max ± 300 ppm)
0 1 : Level 3 (max ± 10%)
1 0 : Level 1 (max ± 50 ppm)
1 1 : Not supported

.LBIT (digital audio signal generation logic)

"0" : Post-recording software
"1" : Not assigned

.DIT (digital audio interface enable)

"0" : DIT LOW-level output
"1" : DIT output enable

87 : Subcode Q data setting Commands(87h = 1000 0111)

Name	Code	DH7	DH6	DH5	DH4	INIT
SUBQDAT	87					X0XXh
		DH3	DH2	DH1	DH0	
		QAD3	QAD2	QAD1	QAD0	
		DL7	DL6	DL5	DL4	
		QD7	QD6	QD5	QD4	
		DL3	DL2	DL1	DL0	
		QD3	QD2	QD1	QD0	

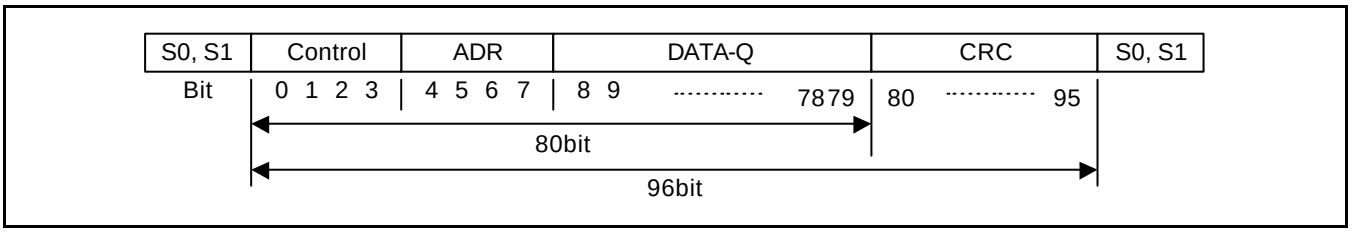
.QAD3 to .QAD0 (Q data setting and word address specification)

QAD3 (MSB) to QAD0 (LSB) specify one of 10 valid addresses in the range 0000 to 1001.
If an address in the range 1010 to 1111 is specified, the data on QD7 to QD0 is ignored.

NOTE: 3 That writing to address 1001 also functions as the write stop command.

.QD7 to .QD0 (Q data setting and word data)

The CD Q-channel has the general data format shown below.
The write data required to fully specify the Q data is the 80 bits comprising CONTROL, ADR, and DATA-Q.
The CRC write data is not required because it is generated by recalculation.



Address map for Q data setting buffer

QAD3	QAD2	QAD1	QAD0	QD7	QD6	QD5	QD4	QD3	QD2	QD1	QD0
0	0	0	0	CTL0	CTL1	CTL2	CTL3	ADR3	ADR2	ADR1	ADR0
0	0	0	1	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8
0	0	1	0	DQ9	DQ10	DQ11	DQ12	DQ13	DQ14	DQ15	DQ16
0	0	1	1	DQ17	DQ18	DQ19	DQ20	DQ21	DQ22	DQ23	DQ24
0	1	0	0	DQ25	DQ26	DQ27	DQ28	DQ29	DQ30	DQ31	DQ32
0	1	0	1	DQ33	DQ34	DQ35	DQ36	DQ37	DQ38	DQ39	DQ40
0	1	1	0	DQ41	DQ42	DQ43	DQ44	DQ45	DQ46	DQ47	DQ48
0	1	1	1	DQ49	DQ50	DQ51	DQ52	DQ53	DQ54	DQ55	DQ56
1	0	0	0	DQ57	DQ58	DQ59	DQ60	DQ61	DQ62	DQ63	DQ64
1	0	0	1	DQ65	DQ66	DQ67	DQ68	DQ69	DQ70	DQ71	DQ72

Subcode Q data setting process

Initially, data is written to word address range 0000 to 1000, and then data is written to address 1001. Next, only data that needs to be changed is written if the 91H command QRDY bit is 1, and then address 1001 is written again. Note that when shockproof mode is ON, the Q data is specified according to the data output from the SM5910AF.

Status flag operation summary

Flag name	Read method		
FLAG6	READ $90 S15	Meaning	-YFLAG detection. -The meaning of YFLAG varies according to the setup of "$A3 DL1 : YFLAG ".
		Set	-Set according to the YFLAG.
		Reset	-By $90 status read. -By $80h command when MSON=ON. -After external reset.
MSOVF	READ $90 S14	Meaning	-Indicates once only that a write to external DRAM has caused an overflow. (When reset by $90 status read command, this flag is reset even if the overflow condition continues.)
		Set	-When the write address (WA) exceeds the read address (RA).
		Reset	-By $90 status read. -When a read address clear (MSRACL) or write address clear (MSWACL) command is issued. -After external reset.
BOVF	READ $90 S13	Meaning	-Indicates input data rate too fast causing buffer overflow and loss of data.
		Set	-When inputs a data during a buffer memory overflow.
		Reset	-By $90 status read. -When a read address clear (MSRACL) or write address clear (MSWACL) command is issued. -After external reset.
DCOMP	READ $90 S11	Meaning	-Indicates that a compare-connect sequence is operating.
		Set	-When a (3-pair or 2-pair) compare-connect start command is receved (MSDCN2=1). -When a direct connect command is receved (MSDCN2=0,MSDCN1=1).
		Reset	-When a (3-pair or 2-pair) comparison detects conforming data. -When the connect has been perfprmed after receiving a direct connect command. -When a compare-connect stop command (MSDCN2=0,MSDCN1=0) is received. -When a MSWREN=1 command is received. (However, if a compare-connect command is received at the same time, the compare-connect command has priority.) -After external reset.

Status flag operation summary (Continued)

Flag name	Read method		
MSWIH	READ $90 S10	Meaning	-Indicates that the encode sequence has stopped due to internal factors. (not MICOM commands)
		Set	-When FLAG6 (above) is set. -When MSOVF (above) is set. -When BOVF (above) is set.
		Reset	-When conforming data is detected after receiving a compare-connect start command. -When the connect has been perfprmed after receiving a direct connect command. -When a read address clear (MSRACL) or write address clear (MSWACL) command is received. -After external reset.
MSRIH	READ $90 S9	Meaning	-Indicates that the decode sequence has stopped due to internal factors. (not MICOM commands)
		Set	-When the valid data residual becomes 0.
		Reset	-By $90 status read. -When a read address clear (MSRACL) or write address clear (MSWACL) command is issued. -After external reset.
MSEMP	READ $91 S15	Meaning	-Indicates that the valid data residual has become 0.
		Set	-When the VWA (final valid data's next address) = RA (address from which the next read would take place).
		Reset	-Whenever the above does not apply.
OVFL	READ $91 S14	Meaning	-Indicates a write to external DRAM overflow state.
		Set	-When the write address (WA) exceeds the read address (RA). (Note: This flag is not set when WA = RA through an address initialize or reset operation.)
		Reset	-When the read address (RA) is advanced by the decode sequence. -When a read address clear (MSRACL) or write address clear (MSWACL) command is issued. -After external reset.
MSEMP	READ $91 S15	Meaning	-Indicates that the valid data residual has become 0.
		Set	-When the VWA (final valid data's next address) = RA (address from which the next read would take place).
		Reset	-Whenever the above does not apply.
OVFL	READ $91 S14	Meaning	-Indicates a write to external DRAM overflow state.
		Set	-When the write address (WA) exceeds the read address (RA). (Note: This flag is not set when WA = RA through an address initialize or reset operation.)
		Reset	-When the read address (RA) is advanced by the decode sequence. -When a read address clear (MSRACL) or write address clear (MSWACL) command is issued. -After external reset.

Status flag operation summary (Continued)

Flag name	Read method		
ENCOD	READ $91 S13	Meaning	-Indicates that the encode sequence (input data entry, encoding, DRAM write) is operating.
		Set	-By the $80 command when MSWREN=1. -When conforming data is detected during compare-connect operation. -When the connect has been performed after receiving a direct connect command.
		Reset	-When FLAG6 (above) is set. -When OVFL (above) is set. -By the $80 command when MSWREN=0. -By the $80 command when MSDCN1=1 or MSDCN2=1 (compare-connect start command). -By the $80 command when MSON=0. -After external reset. (Note: Reset conditions have priority over set conditions. For example, if the $80 command has MSWREN=1 and MSDCN1=1,the ENCOD flag is reset and compare-connect operation starts.)
DECOD	READ $91 S12	Meaning	-Indicates that the decode sequence (read from DRAM, decoding, attenuation, data output) is operating.
		Set	-By the new $80 command when MSRDEN=1 and the MSEMP flag=0 (above).
		Reset	-Whenever the above dose not apply.
QRDY	READ $91 S11	Meaning	-Subcode Q data write-buffer write enable indicator.
		Set	-After internal subcode Q data write-buffer contents are read out.
		Reset	-When data is written to address 1001 using the $87 command.

Shock-proof operation overview

Shock-proof mode is the mode that realizes shock-proof operation using external DRAM. Shock-proof mode is invoked by setting MSON=H in MICOM command $80.
This mode comprises the following 3 sequences.

— Encode sequence

1. Input data is stored in internal buffers.
2. Encoder starts after a fixed number of data have been received.
3. The encoder, after the most suitable predicting filter type and quantization steps have been determined, performs ADPCM encoding and then writes to external DRAM.

— Decode sequence

1. Reads compressed data stored in external buffer RAM at rate fs.
2. Decoder starts, using the predicting filter type and quantization levels used when encoded.
3. Performs attenuation operation (including muting operation)
4. Outputs the result.

— Compare-connect sequence

1. Encoding immediately stops when either external buffer RAM overflows or when a CD read error occurs due to shock vibrations.
2. Then, using MICOM command $80, the compare-connect start command is executed and compare-connect sequence starts.
3. Compares data re-read from the CD with the processed final valid data stored in RAM (confirms its correctness).
4. As soon as the comparison detects conforming data, compare-connect sequence stops and encoding sequence re-starts, connecting the data directly behind previous valid data.

RAM addresses

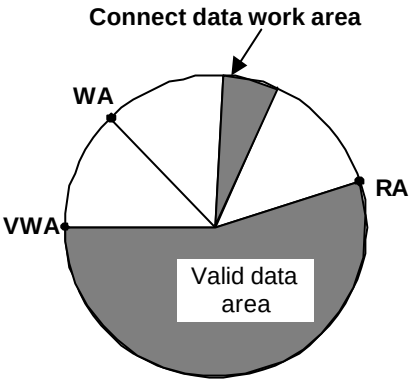
Three kinds of addresses are used for external RAM control.

WA (write address)
RA (read address)
VWA (valid write address)

Among these, VWA is the write address for conforming data whose validity has been confirmed. Determination of the correctness of data read from the CD is delayed relative to the encoding write processing, so VWA is always delayed relative to WA.
The region available for valid data is the area between VWA-RA.

— Connect data work area

This is an area of memory reserved for connect data. This area is 2k bits if using 1M DRAMs, 4k bits if using 4M DRAMs, or 8k bits if using 16M DRAMs.



RAM addresses

VWA (valid write address)

The VWA is determined according to the S0S1 and WAQV command. Refer to the timing chart below.

1. S0S1 is a 75Hz clock when used for normal read mode and it is a 150Hz clock when used for double-speed read mode, synchronized to the CD format block start timing.
   When this clock goes LOW, WA which is the write address of internal encode sequence, is stored (see note 2).
2. The MICOM checks the subcode and, if confirmed to be correct, generates a WAQV command ($80).
3. When the WAQV command is received, the previously latched WA is stored as the VWA.

NOTES 2: Actually, there is a small time difference, or gap, between the input data and YBLKCK. This gap serves to preserves the preceding WA to protect against incorrect operation.

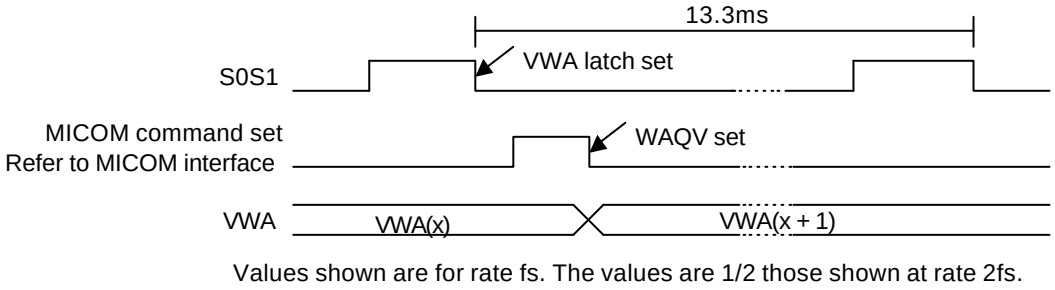


Figure 3. YBLKCK and VWA relationship

YFLAG, FLAG6

Correct data demodulation becomes impossible for the CD-DSP when a disturbance exceeding the RAM jitter margin occurs. The YFLAG signal input pin is used to indicate when such a condition has occurred.

The IC checks the YFLAG input and stops the encode sequence when such a disturbance has occurred, and then makes FLAG6 active.

Compare-connect sequence

The SM5910 supports three kinds of connect modes; 3-pair compare-connect, 2-pair compare-connect and direct connect.

Note that the SM5910 can also operate in 12-bit comparison connect mode using only the most significant 12 bits of data for connection operation.

In 3-pair compare-connect mode, the final 6 valid data (3 pairs of left- and right-channel data input before encode processing) and the most recently input data are compared until three continuous data pairs all conform. At this point, the encode sequence is re-started and data is written to VWA.

In 2-pair compare-connect mode, comparison occurs just as for 3-pair comparison except that only 2 pairs from the three compared need to conform with the valid data. At this point, the encode sequence is re-started and data is written to VWA.

In direct-connect mode, comparison is not performed at all, and encode sequence starts and data is written to the VWA. This mode is for systems that cannot perform compare-connect operation.

— Compare-connect preparation time

1. Comparison data preparation time

   Internally, when the compare-connect start command is issued, a sequence starts to restore the data for comparison. The time required for this preparation after receiving the command is approximately 2.5 x (1/fs). (approximately 60 ms when fs = 44.1kHz)

2. After the above preparation is finished, data is input beginning from the left-channel data and comparison starts.
3. If the compare-connect command is issued again, the preparation time above is not necessary and operation starts from step 2.
4. The same sequence takes place in direct-connect mode also. However, at the point when 3 words have been input, all data is directly connected as if comparison and conformance had taken place.

— Compare-connect sequence stop

If a compare-connect stop command (80H with MSDCN1= 1, MSDCN2= 0) is input from the microcontroller, compare-connect sequence stops.

If compare-connect sequence was not operating, the compare-connect stop command performs no operation. However, make sure that the other bit settings within the same 80H command are valid.

Encode sequence temporary stop

— When RAM becomes full, MSWREN is set LOW using the 80H command and encode sequence stops. (For details of the stop conditions, refer to the description of the ENCOD flag.)

— Then, if MSWREN is set HIGH without issuing a compare-connect start command, the encode sequence re-starts. At this time, new input data is written not to VWA, but to WA. In this way, the data already written to the region between VWA and WA is not lost.

— But if the MSWREN is set HIGH (80H command) after using the compare-connect start command even only once, data is written to VWA. If data is input before comparison and conformance is detected, the same operation as direct-connect mode takes place when the command is issued. After comparison and conformance are detected, no operation is performed because the encode sequence has already been started. However, make sure that the other bit settings within the same 80H command are valid.

DRAM refresh

— DRAM initialization refresh
A 15-cycle RAS-only refresh is carried out for DRAM initialization under the following conditions.
When MSON changes from 0 to 1 using command 80H.
When from MSON=1, MSRDEN=0 and MSWREN=0 states only MSWREN changes to 1. In this case, encode sequence immediately starts and initial data is written (at 2fs rate input) after a delay of 0.7ms.

— Refresh during Shock-proof mode operation
In this IC, a data access operation to any address also serves as a data refresh. Accordingly, there are no specific refresh cycles other than the initialization refresh cycle (described above).
This has the resulting effect of saving on DRAM power dissipation.

A data access to DRAM can occur in an encode sequence write operation or in a decode sequence read operation. Write sequence write operation stops during a connect operation whereas a read sequence read operation always continues while data is output to the D/A. The refresh rate for each DRAM during decode sequence is shown in the table below.

The decode sequence, set by MSON=1 and MSRDEN=1, operates when valid data is in DRAM (when MSEMP=0).

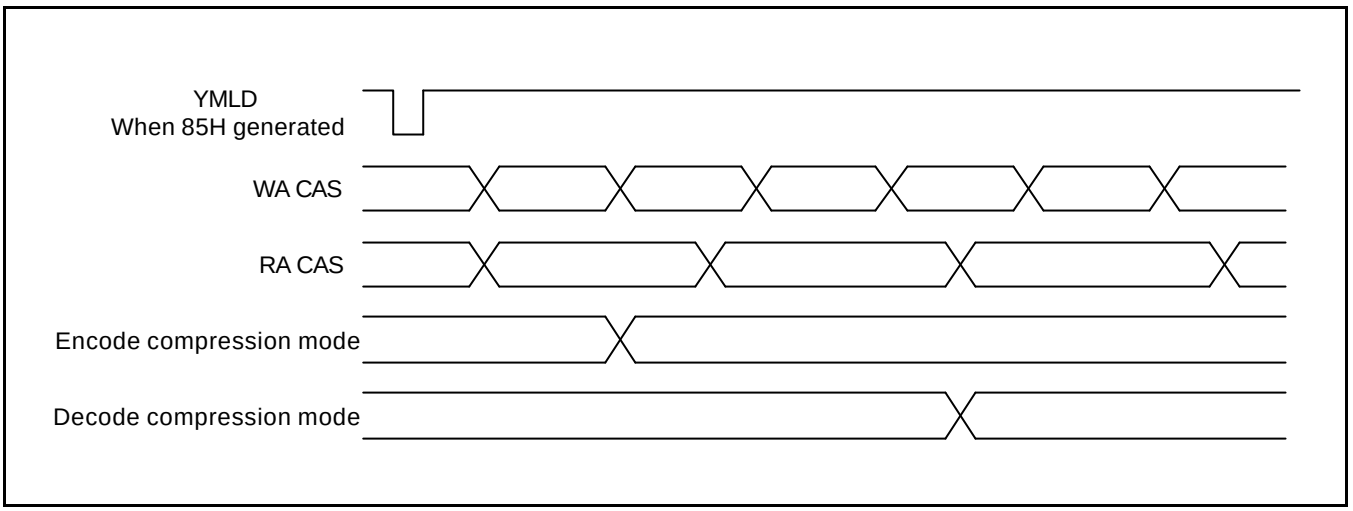
— When MSON=0, DRAM is not refreshed because no data is being accessed. Although MSON=1, DRAM is not refreshed if ENCOD=0 and DECOD=0 (both encode and decode sequence are stopped).

Table 4. Decode sequence refresh rate

Data compression mode	DRAM used(same for 1 or 2 DRAMs)		
	1M(256k x 4 bit)	4M(1M x 4 bit)	16M(4M x 4 bit)
4 bit	5.44ms	10.88ms	21.77ms
5 bit	4.35ms	8.71ms	17.42ms
6 bit	3.63ms	7.26ms	14.52ms
Full bit	1.36ms	2.72ms	5.81ms

Selecting compression mode

Even when the compression mode in selected with the 85H command during shock-proof operation, no malfunction occurs.
The compression mode change is not performed immediately after input of the 85H command, but it is performed at the following timing.



NOTE: CAS-000 is connect data.

Through-mode operation

If MSON is set LOW (80H command), an operating mode that does not perform shock-proof functions becomes active. In this case, input data is passed as-is (after attenuator and mute operations) to the output. External DRAM is not accessed.

— In this case, input data needs to be at a rate fs and the input word clock must be synchronized to the CLK input (384fs). However, short range jitter can be tolerated (jitter-free system).

— Jitter-free system timing starts from the first YLRCK rising edge after either (A) a reset (NRESET= 0) release by taking the reset input from LOW to HIGH or (B) by taking MSON from HIGH to LOW. Accordingly, to provide for the largest possible jitter margin, it is necessary that the YLRCK clock be at rate fs by the time jitter-free timing starts.
The jitter margin is 0.2/ fs (80 clock cycles).
This jitter margin is the allowable difference between the system clock (CLK) divided by 384 (fs rate clock) and the YLRCK input clock.
If the timing difference exceeds the jitter margin, irregular operation like data being output twice or, conversely, incomplete data output may occur. In the worst case, a click noise may also be generated.
When switching from shock-proof mode to through mode, an output noise may be generated, and it is therefore recommended to use the YDMUTE setting to mute ZSRDATA until just before data output.

Attenuation

— The attenuation register is set by the 84H command.

— The attenuation register set value becomes active when the 83H command sets the ATT flag to 1. When the ATT flag is 0, the attenuation register value is considered to be the equivalent of 256 for a maximum gain of 0 dB.

— The gain (dB) is given from the set value (Datt) by the following equation. Gain = 20 ?a log(Datt/256) [dB]; left and right channels

— For the maximum attenuation register set value (Datt = 255), the corresponding gain is -0.03 dB. But when the ATT flag is 0 (Datt = 256), there is no attenuation.

— After a system reset initialization, the attenuation register is set to 64 (-12 dB). However, because the ATT flag is reset to 0, there is no attenuation.

— When the attenuation register setting changes or when the ATT flag changes, the gain changes smoothly from the previous set gain towards the new set value. If a new value for the attenuation level is set before the previously set level is reached, the gain changes smoothly towards the latest setting.

The gain changes at a rate of 4 ?h (1/fs) per step. A full-scale change (255 steps) takes approximately 23.3 ms (when fs = 44.1 kHz). See figure 3.

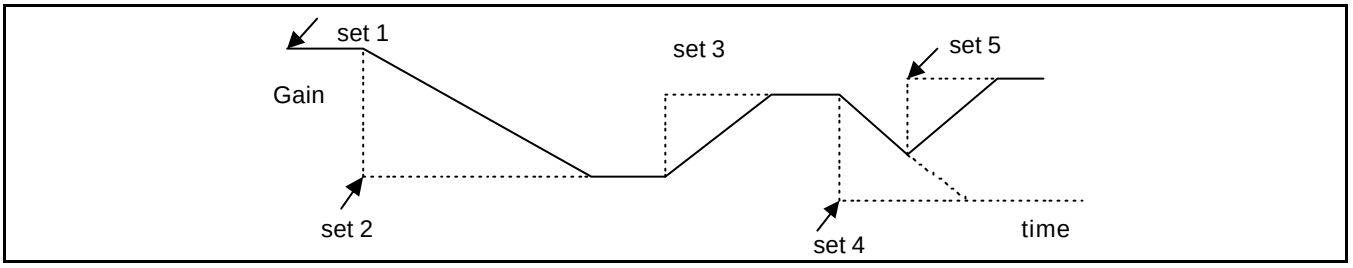


Figure 5. Attenuation operation example

Soft mute

Soft mute operation is controlled by the SOFT flag using a built-in attenuation counter.
Mute is ON when the SOFT flag is 1. When ON, the attenuation counter output decrement by 1 step at a time, thereby reducing the gain. Complete mute takes 1024/fs (or approximately 23.2 ms for fs = 44.1kHz).
Conversely, mute is released when the SOFT flag is 0. In this case, the attenuation counter instantaneously increases. The attenuation register takes on the value when the ATT flag was 1. If the ATT flag was 0, the new set value is 256 (0 dB).

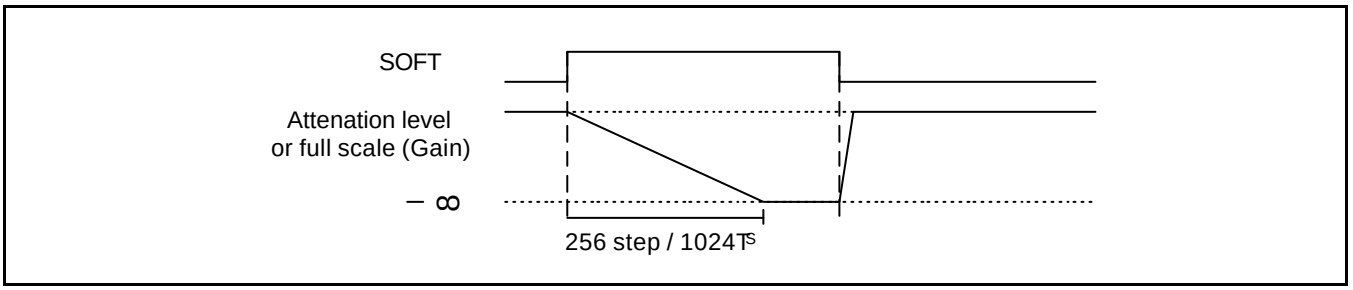


Figure 6. Soft mute operation example

Force mute

Serial output data is muted by setting the YDMUTE pin input HIGH or by setting the MUTE flag to 1. Mute starts and finishes on the leading left-channel bit.
When MSON is HIGH and valid data is empty (MSEMP=H), the output is automatically forced into the mute state.

12-bit comparison connection

When the CMP12 flag is set to 1, the least significant 4 bits of the 16-bit comparison connection input data are discarded and comparison connection is performed using the remaining 12 bits.
Note that if the CMP12 flag is set to 1 during a comparison connection operation, only the most significant 12 bits are used for comparison connection from that point on.

Digital audio interface

When the DIT flag is set to 1, the digital audio interface output from pin DIT is enabled. The output data structure is modulated using a preamble and biphase mark encoding.

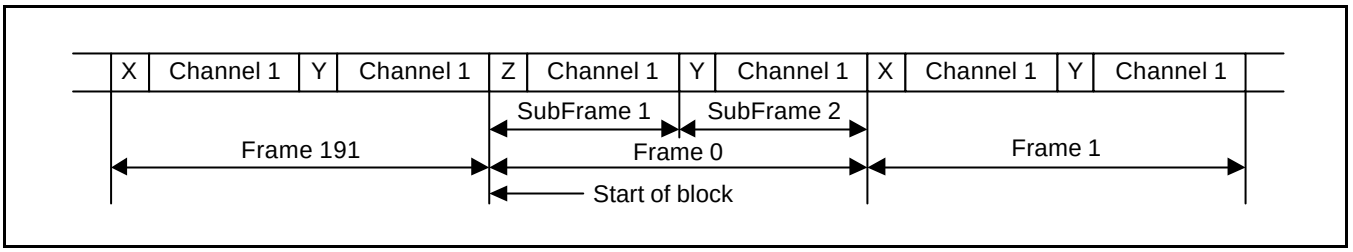


Figure 7. Frame format

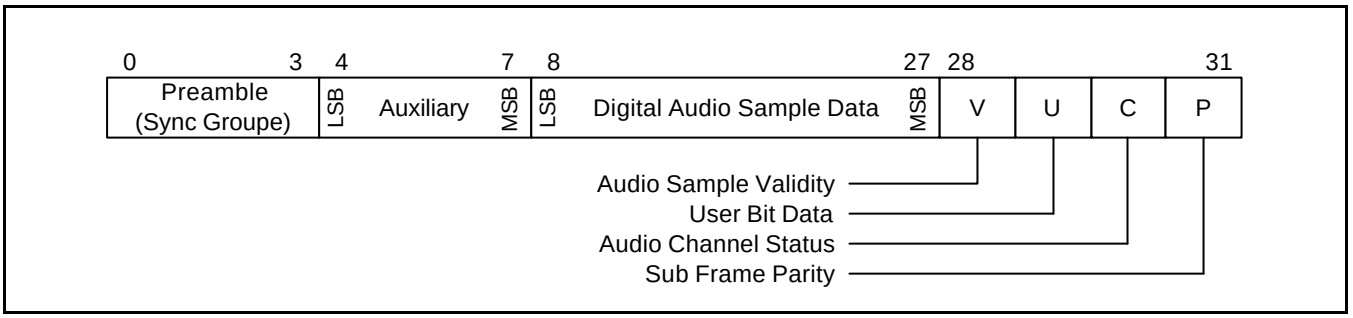


Figure 8. Subframe format

Preamble

The preamble is a particular bit pattern used to perform subframe and block synchronization and discrimination, assigned to one of 4 time slot divisions (0 to 3), comprising 8 continuous biphase modulated transfer rate status indicators.
There are 3 types of preamble. The leading preamble pattern of all blocks is preamble pattern B, which is then followed by preamble pattern M for channel 1, and preamble pattern W for channel 2.

preamble	Channel coding	
	Leading symbol = 0	Leading symbol = 1
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

Digital audio sample data and auxiliary audio

The digital audio sample data is a 20-bit digitized audio signal. Auxiliary audio data, on the other hand, can be audio sample data of varying length. The SM5910AF uses a 16-bit audio data structure internally with audio data output bits 4 to 11 set to 0 and bits 12 to 27 output in LSB first format.

Audio sample validity

The validity flag is set to 0 when the digital audio sample data is output correctly, or it is set to 1 if the output is incorrect. It is also set to 1 if encoding does not start when the device is operating in forced mute, microcontroller forced mute, and shockproof mode.

User bit data

User bit data is data specified by the user. The data is output, after the Q data has been specified, in the following sequence.

	0	1	2	3	4	5	6	7	8	9	10	11
0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0
24	1	Q_1	0	0	0	0	0	0	0	0	0	0
36	1	Q_2	0	0	0	0	0	0	0	0	0	0
: :	: :	: :	: :	: :	: :	: :	: :	: :	: :	: :	: :	: :
1164	1	Q96	0	0	0	0	0	0	0	0	0	0

— Using Q data

Initially, Q1 to Q80 are set using the 87H command, the DIT flag is set using the 86H command, and then data is output from DIT according to the digital audio interface format. Q81 to Q96 data are not required as these are set internally by CRC calculation.
There are 2 Q data buffers; a data output buffer and a data storage buffer. As a result, after all data has been specified in the first data write, only that data that has changed needs to be written during the 2nd and subsequent data write operations. Note that address 1001 is the write stop command and is, therefore, required after every data write operation.
When space becomes available in the data output buffer, QRDY is set to 1 (91H command status bit S3) to indicate available space and then the contents of the data storage buffer are transferred to the data output buffer. After data is transferred, a data write to address 1001 (write stop command) resets the QRDY flag to 0.
The Q data buffer read access time for a complete data cycle is approximately 13.3 ms.

Audio channel status

The channel status are information bits transferred to indicate the audio sample data length, preemphasis, sampling frequency, time code, source number, destination code, and other information. Seven bits comprising CP1, CP2, LBIT, and CTL0 to CTL3 can be set. All other bits are fixed.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	CTL0	CTL1	CTL2	CTL3	0	0	0	0	0	0	0	0	0	0	0	LBIT
16	0	0	0	0	L=1	R=1	0	0	0	0	0	0	CP1	CP2	0	0
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
48	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
80	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
96	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
112	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
128	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
144	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
160	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
176	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Subframe parity

The parity bit is used to indicate the detection of an odd number of bit errors. It is set to 1 if the number of 1s in the digital audio interface 27-bit data is odd, and is set to 0 if the number of 1s is even. The 27-bit data plus parity bit form 28-bit data that always has an even number of 1s.

DBB

Caution : It is only the case of FUNCNTL($A0) DBBON=1 that this commands is effective.

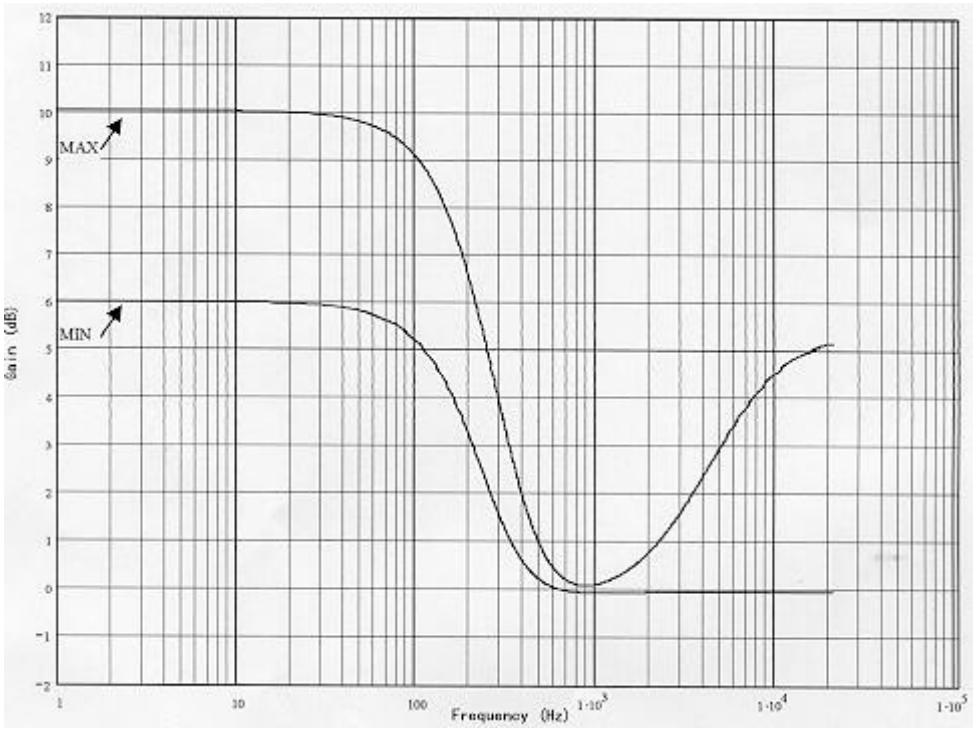
$70 : DBB Related Commands(70h = 0111 0000)

Name	Code	DL7	DL6	DL5	DL4	INIT
DBB	70					00h
		DL3	DL2	DL1	DL0	
		TST1	0	MAX	DBB	

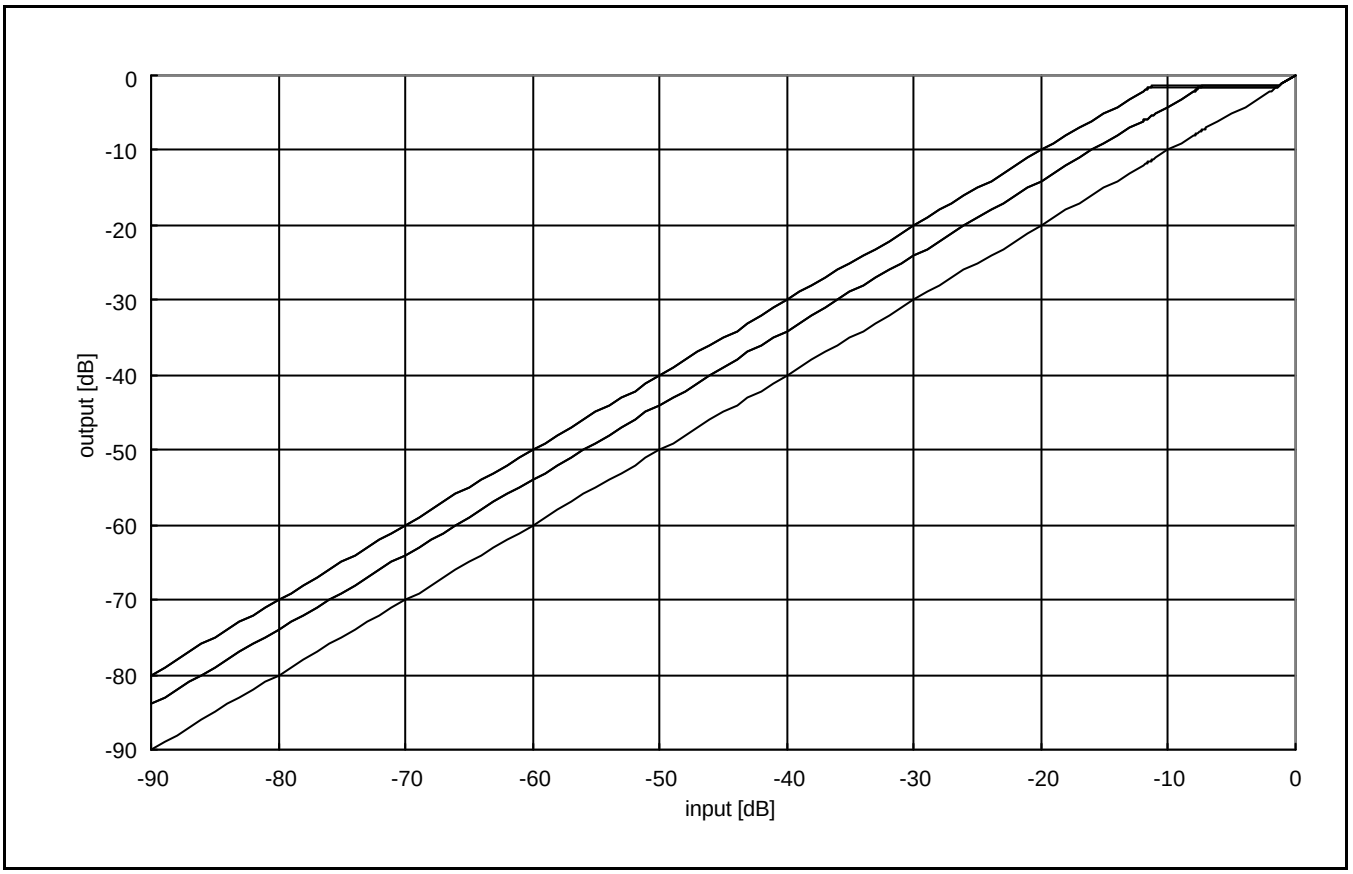
.TST1 :
"0" : Normal mode
"1" : DBB test mode
.MAX .DBB :
0 0 : DBB off (through)
0 1 : DBB on, minimum boost setting
1 0 : DBB off (through)
1 1 : DBB on, maximum boost setting

The DBB (Dynamic Bass Boost) function emphasizes the spectrum by changing gain of the specific frequency of the input signal.

DBB Frequency characteristic



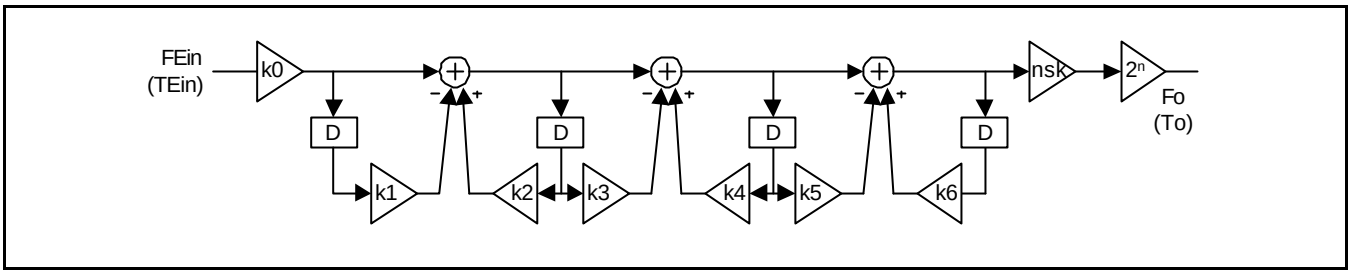
DBB gain response



DIGITAL SERVO

Digital Servo

The architecture of Focus/Tracking Loop Filter is as following. They have 3 poles and 3 zeros.



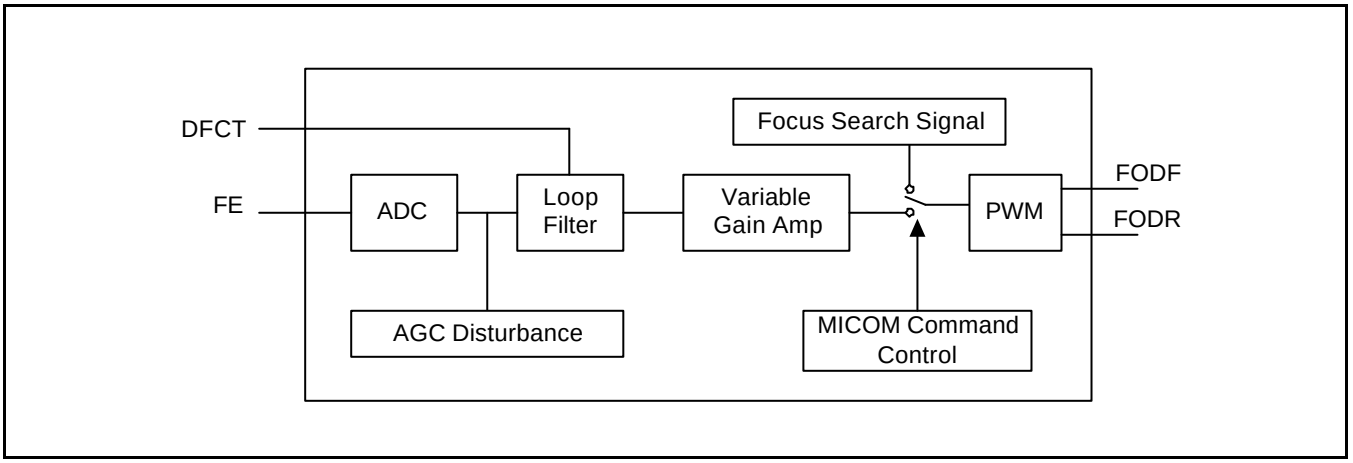
Therefore, transfer function is as below.

$$H(Z) = \frac{K0 * (1-K1*Z^{-1}) * (1-K3 * Z^{-1}) * (1-K5* Z^{-1}) * (NSK*2^{n})}{(1-K2*Z^{-1}) * (1-K4 * Z^{-1}) * (1-K6* Z^{-1})}$$

Each Coefficient could be changed variously depending on the characteristics of pick-up by micro-controller command. The filter coefficients can be designed using the provided simulator. Using the simulator, users can monitor the closed loop characteristics of the full system, which includes actuator, RF, digital servo, and driver. If user selects only the frequencies of pole and zero, and the DC gain, simulator generates hexadecimal value of each coefficient automatically.

Focus Servo

The below figure is the functional block diagram of the Focus Servo.

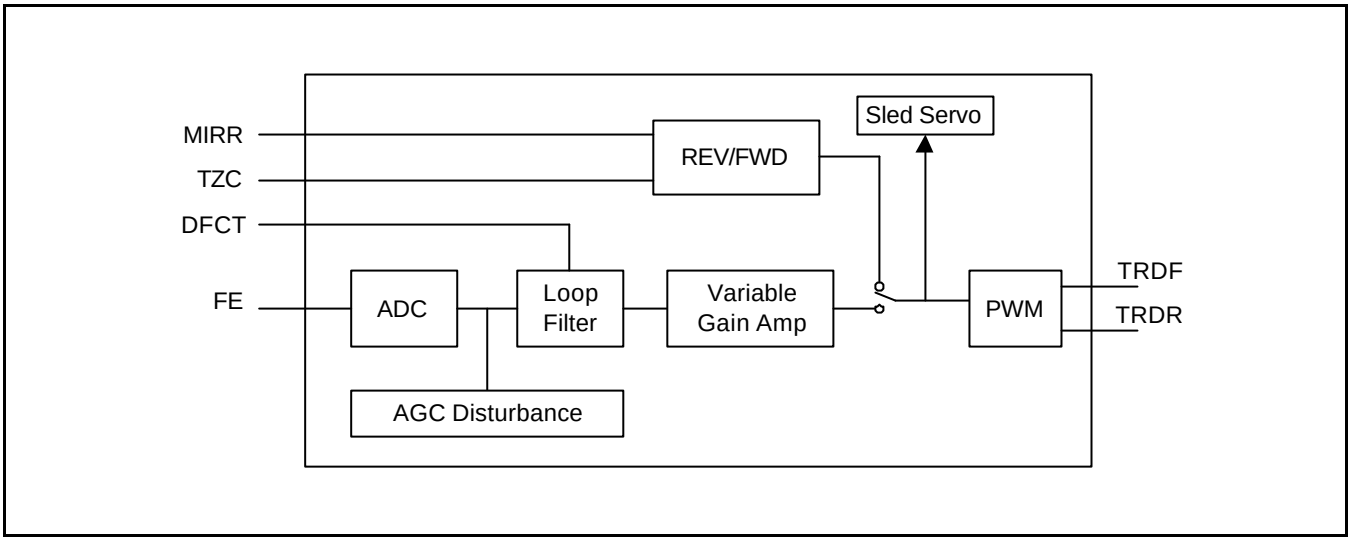


The focus error signal input into the FE pin goes through the input gain adjustment amplifier to achieve a regular level. The signal passes through the ADC, Loop filter, and output gain control block, then is output to the FODF/FODR pin through the PWM. It activates the focus coil through the drive amplifier. For Drop out solution, it holds the loop filters input if DFCT signal is generated by the RF. If it receives the disc detect command (DDT) or focus on command (FON), it generates delta waves from inside the digital servo, which activates the focus coil to move the pick-up perpendicular to the disc. The output always passes through the noise-shaping filter to improve output resolutions.

When **FONcmd** is asserted from micro-controller, FODF/FODR generates focus actuator drive voltage to monitor the FE signal, which carries out focus pull-in.
Focus-related jobs are divided into disc detection and focus pull-in. These are activated by DDTcmd and FON cmd command routines.

TRACKING SERVO

The below figure is the block diagram of tracking servo.



After A/D, the TE signal goes through the compensation filter and variable gain control block. It is then converted to PWM signal, then output to the driver IC (Variable gain is automatically selected during auto gain adjustment). As Drop out solution, it holds the loop filter input for DFCT signal.
When TONcmd is input from micro-controller, the digital servo activates tracking filter, monitors MIRR and TZC signals, and carries out pull-in of the closest track. Like the Focus Servo, the Tracking Servo signals also come out through the noise-shaping filter.

Automatic Adjustment

The following adjustments are included in the automatic adjustments, which are offset adjustment by OFAcmd, focus bias adjustment by FBAcmd, tracking bias/balance adjustment by TBAcmd, and loop gain adjustment by FGAcmd and TGAcmd. Please refer to the micro-controller command specification for detail. The automatically adjusted features in order are as follows.

1) Input Gain Adjustment

This function is to measure the input error signal's peak level, then to adjust the input amplifier's gain to make the peak level about 80% of the A/D s maximum input.

The input gain's automatic adjustment has the ability to absorb the deviation of the focus and tracking error's signal level from the RF for each set. Also, there is no gain switching feature for different disc types within the RF, it corrects the focus and tracking error's signal level difference. For focus, the S_curve size measured during focus search is used as the input gain amp's input. For tracking, the TE's track zero cross size when the disc is spinning in off track status is used as the input gain amp's input. Automatic adjustment is carried out so that it is approximately 80% of the maximum input no matter what the input gain amplifier's output level is. This has the advantage of using the ADC's input range to its fullest, and improving the decomposition ability in quantization. Manual setting can set the input gain to a fixed value at an appropriate level

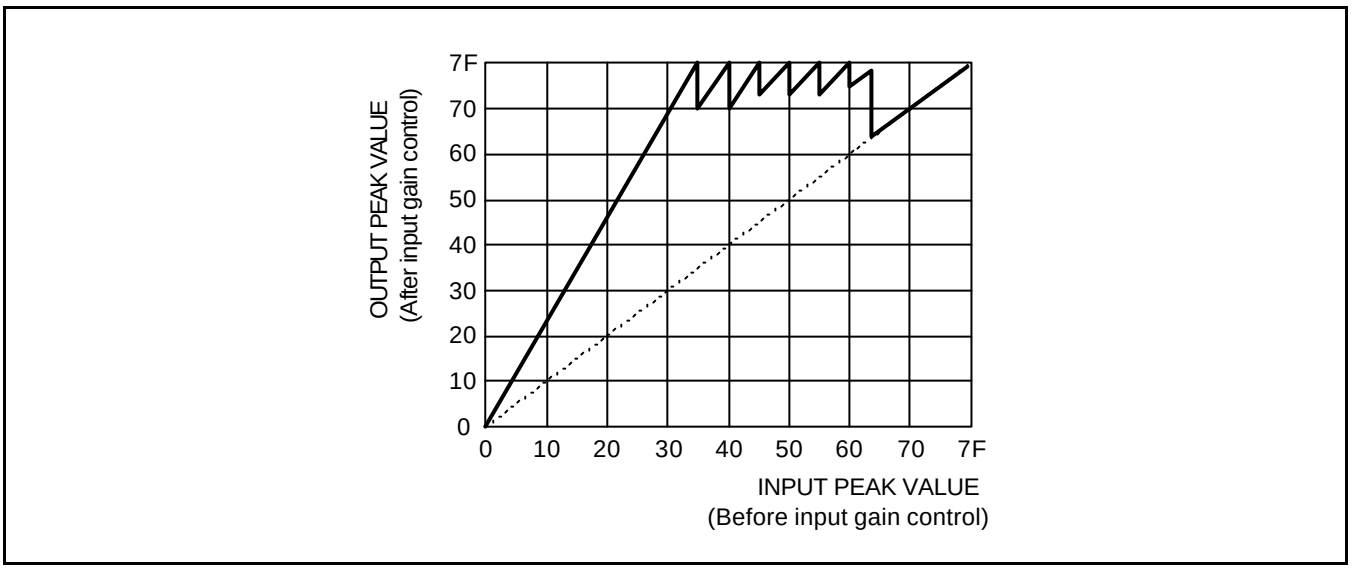


Figure 9. Input Gain Adjustment amplifier's gain characteristics (for automatic adjustment)

2) Offset Adjustment

The focus/tracking offset is electrical offset, which signifies the error level during defocus.
The offsets can be explained as the error signals when there is no input (FE/TE's electrical offset). The offset measurement can be carried out during laser diode On/Off status by micro-controller command, so it is appropriate to issue the system select command after reset release at the end.
When OFAcmd is received, the focus and tracking error offset are measured/averaged and stored in the register. This is to use the values during later filter operations in order to eliminate remaining error offset.

3) Bias/Balance Adjustment

Two algorithms are used for adjustment of focus bias in this digital servo. One of them is making peak and bottom of the S-curve's amplitude same using the Disc Detect Command (DDTcmd), which is the one already mentioned. The other algorithm is the method in which the TE sum(TES) level becomes peak, which is supported by FBA cmd.
The former is a rather simplified method that adjusts the bias as well as the DDTcmd search. The latter is a more active method that uses the following characteristic. If the balance is bad, the focus does not match exactly in the pit, and the TES level becomes lower, whereas when the focus is exact, the TES level goes to peak.

4) Tracking Balance Adjustment

Balance error value can be measured by integrating peak value of TE (min/max) in the off-track state. There are two methods for adjustment. The first one is that saving balance error value to Tbias. The value of Tbias is subtracted from TE, thus bias adjusted error signal can be generated. The other one is hardware oriented balance adjustment which makes error value feed back to TE block. The adjustment method can be selected by FLGcmd.

5) Focus Bias Adjustment

Focus bias adjustment is carried out so that playback is executed when the RF signal quality is at its best. The quality of the RF signal is shown by the jitter amount, but it is difficult to have an algorithm that can measure jitter on the IC and find the minimum point. Therefore, you use the characteristic where the jitter is always at its minimum near the focus bias point with the largest TES size. The focus bias is adjusted so that the TES is at its maximum size.

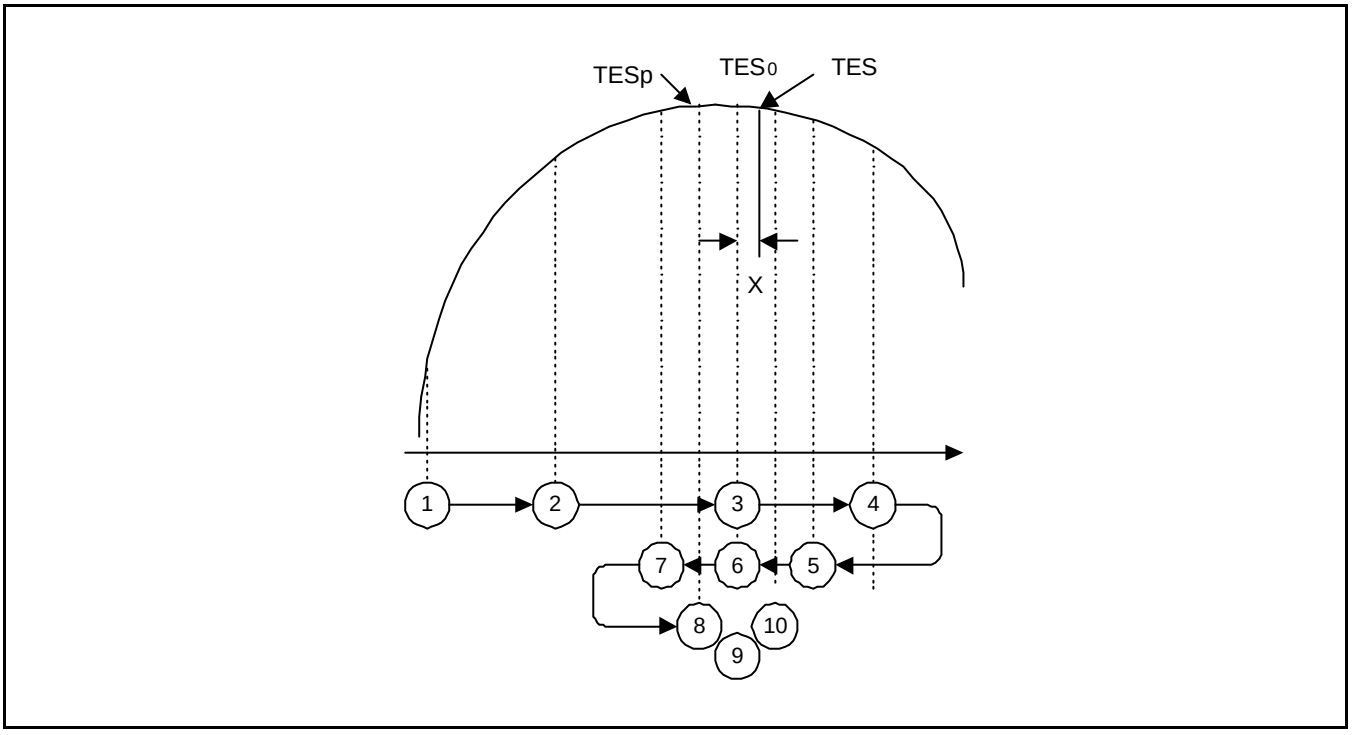
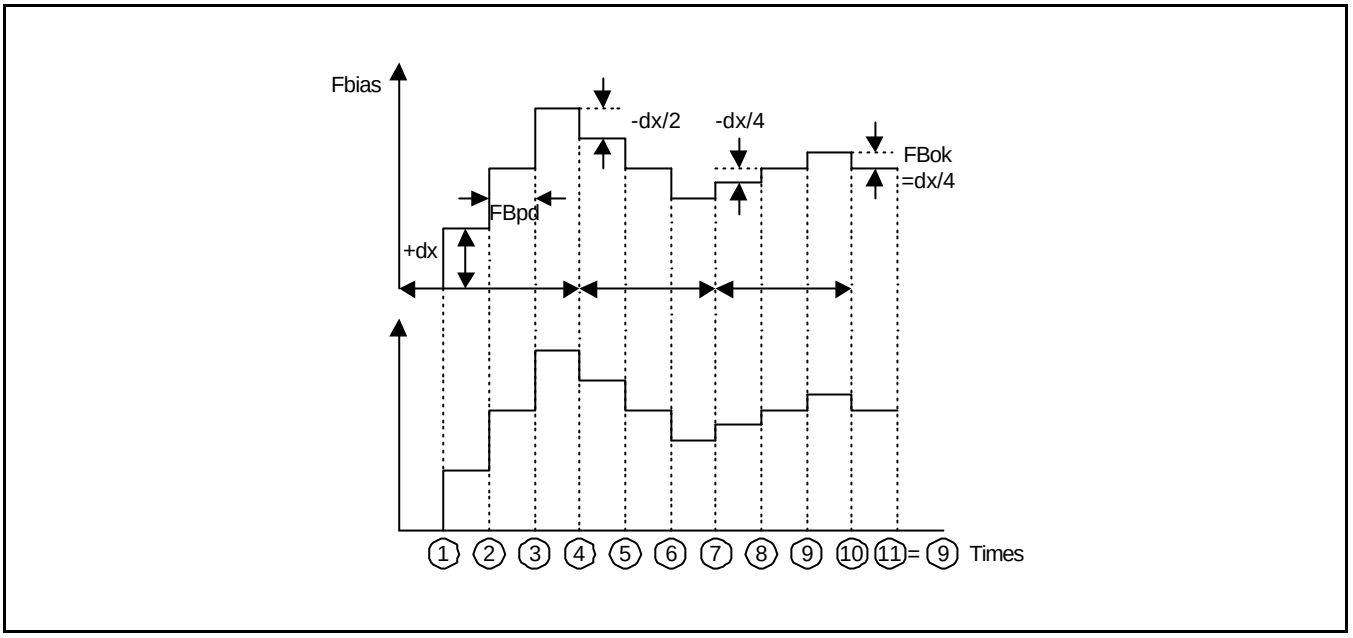


Figure 10. The algorithm of Focus bias adjustment through TES

TES' signal difference is minimized by the FE signal carrying the disturbance. The disturbance uses the FE as reference and is used after selecting +/-dX. The disturbance level value is given to the first + direction, the TES value is stored, and +/- is repeated so that the dxbuf amount of the largest TES level is added/subtracted from the Fbias amount to find the final Fbias.



6) Loop Gain Adjustment

The goal of this function is to make the gain of an entire Loop at a specific frequency f0 to 0 dB. Gain adjustment is accomplished by overlapping the measurement signal X within the Servo loop during Servo On status, and measuring the phase difference between X and Y, the detected signal. If you overlap the measurement signal with the sinusoidal wave of the frequency, the loop gain you want is 0 dB, and you can use the following characteristic. When the phase difference between the detected signal and the measurement signal is 90 degrees, the loop gain at that frequency is 0dB.

Track Jump Using Kick/Brake

This method jumps tracks by outputting an acceleration/deceleration pulse to the TRDF/TRDR output to carry out kick/brake. The algorithm consists of 3 steps (kick+brake+stabilizing area), and the track count is executed using mirror or COUT(TZC without noise).

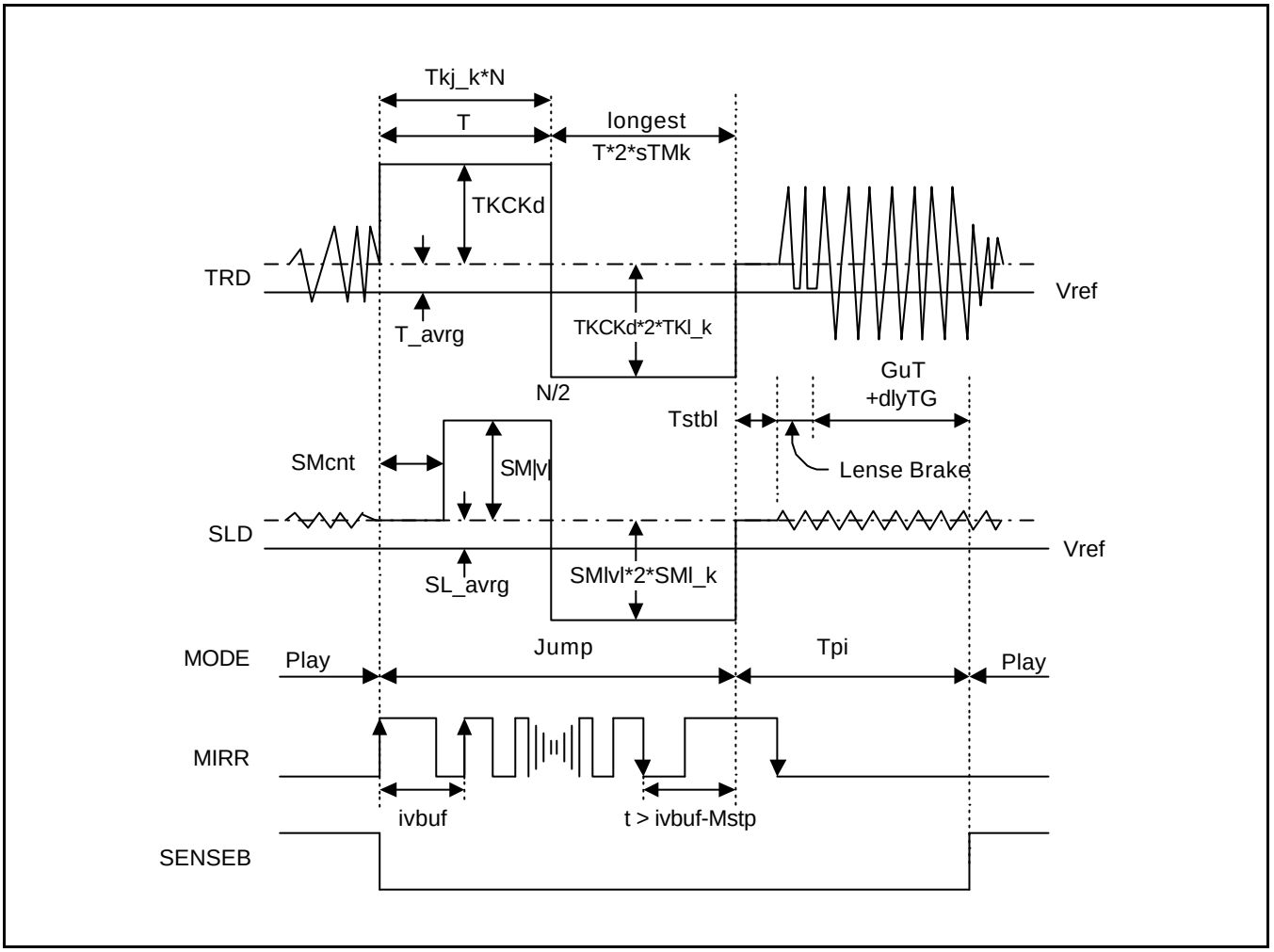


Figure 11. x. Tracking Kick/Brake Timing Diagram

The track kick pulse is the TRDF/TRDR output average value(TRD_avrg) before jump, overlapped with the kick level(TKCKd). The track kick pulse reverts to brake when the track counter(H.CT) becomes larger than the jump track # (N)*TKj_k, and the level is TKCKd*2*TKl_k.

If the MIRR period within the kick area becomes larger than ivbuf(Jstp)+Kwdt(according to BTS select conditions), it is a long-term error of the MIRR, and there is a change to brake for safety.

When the jump trk # generated by the track kick reaches the sled movement count(SMcnt), the sled output average value before the jump(SL_avrg) and the sled move level(SMlvl) kick are overlapped. Sled reverts to brake along with the trk kick's reversion to brake, and the level is SMlvl*2*SMl_k

DRIVE INTERFACE

The digitally handled Focus, Tracking, Sled, and Spindle Servo output go through PWM. Here, the Focus and Tracking drive output uses the 8-bit resolution, and the Sled and Spindle, the 6-bit resolution

PWM

	Main Clock, Number Notation, Resolution		
Mode	**FOD, TRD**	**SLD**	**SPD**
000	Half-bit resolution (Clk5M) 2's complement (default)	Half-bit resolution (Clk88K), 2's complement (default)	Half-bit resolution (Clk88K), 2's complement (default)
001	Half-bit resolution (Clk5M) Signed magnitude	Half-bit resolution (Clk88K), Signed magnitude	Half-bit resolution (Clk88K), Signed magnitude
010	Full-bit resolution (Clk1M), 2's complement	Full-bit resolution (Clk176K)	Full-bit resolution (Clk176K)
011	Full-bit resolution (Clk1M) Signed magnitude		
100	Half-bit resolution (Clk5M) 2's complement, +1 resolution		
101	Half-bit resolution (Clk5M) Signed magnitude, +1 resolution		
110	Full-bit resolution (Clk1M), 2's complement, +1 resolution		
111	Full-bit resolution (Clk1M) Signed magnitude, +1 resolution		

CD-DSP

EFM DEMODULATOR

This block demodulates EFM signals read from the CD. EFM demodulator block-related command registers and data are shown in below Table.

Table 5. EFM related MICRO-CONTROLLER command

Comments	Address D15~D08	Data								SENSE
		D7	D6	D5	D4	D3	D2	D1	D0	
Frame SYNC Protection, Attenuation Control	A1	FSEL[1:0]		WSEL[1:0		FSMD[1:0]		-	-	LKFS

EFM Phase Detection (Phase Comparison)

The NRZ format EFM input signal from the CD is made into a syn_efm_nrz signal, whose phase is synchronized with 4.3218MHz (2x: 8.6436 MHz) pll generated clock and NRZI format syn_efm_nrzi signal. As shown in figure below, the syn_efm_nrzi signal generates "H" at the transition edge of syn_efm_nrz signal and "L" for the rest.

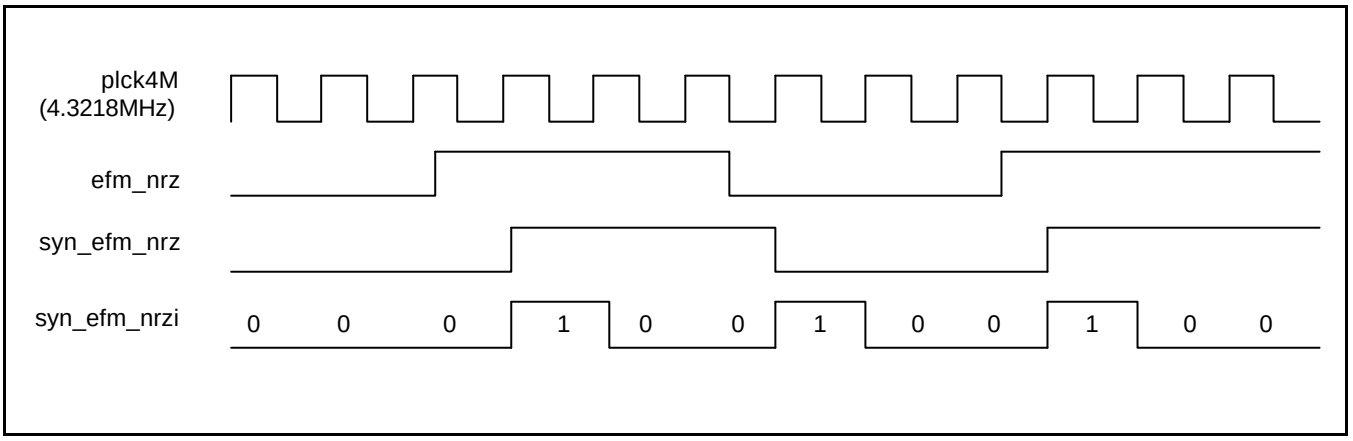


Figure 12. Timing diagram for EFM phase detection

SUBCODE S0S1 Generation

The synchronization patterns of SUBCODE, S0 (00100000000001) and S1 (00000000010010) are detected by EFM block. If either one of S0 or S1 is detected, S0S1 signal is set to H.

SUBCODE BLOCK

The SUBCODE block receives 8-bit subcode data with the cycle of 7.35kHz from the EFM block (synchronized with the write frame clock), and transmits to digital audio out block from the EFM block. Out of the 8-bit data (channel P ~ channel W), P and Q data are handled, then sent to micro-controller. The subcode data is data for CDP control or display, (one subcode block is composed of 98 symbols (8-bit)). Channel P data bit shows the start of the track. If it is "0", it is in the middle of a track, and if "1", it shows the starting of a track. Channel Q data is mainly timing data information, and each frame has 16 bits of CRC data. If the CRC result is "0", this data is transmitted to micro-controller, and if "1", "L" is output. The other channel R, S, T, U, V, W data are not used in S5L9232.

CLKGEN

The CLKGEN block makes all the clocks used in the CD-DSP and reset-related signals for each block. All clocks used in the CD-DSP are made using crystal-generated 16.9344 MHz or embedded PLL.

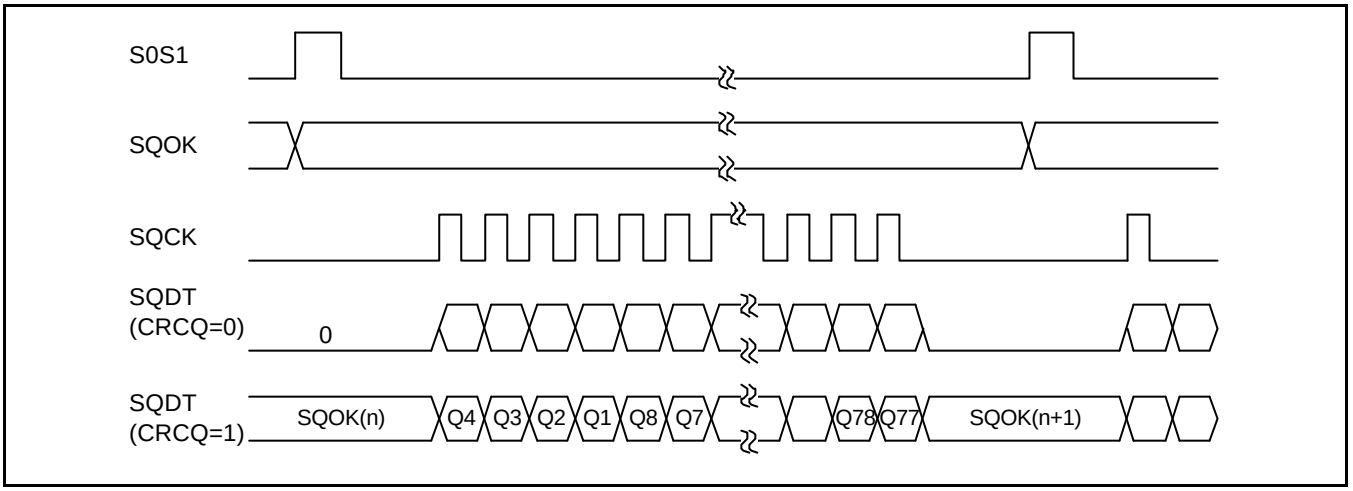


Figure 13. Subcode block Signal Timing Diagram

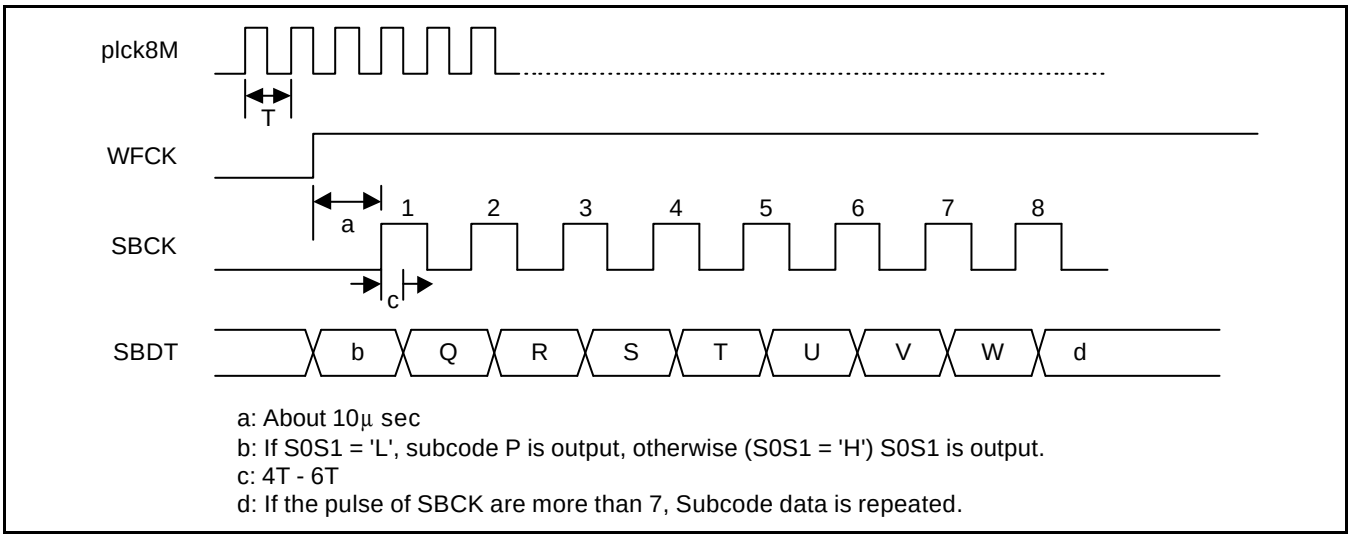


Figure 14. plck8M, WFCK, SBCK, SBDT Timing Diagram

ECU / MMU

ECU (Error Correction Unit)

The ECU block is a microprocessor specifically for error correction(ECC), and thus makes error corrections during decoding according to the proper error correction code (ECC) algorithm.

MMU (Memory Management Unit)

The MMU block manages the 16Kbit memory that is used within S5L9232 for EFM data storage, and read/writes memory according to EFM data priority.

INTERPOLATION

The Interpolation block interpolates the audio data that may still have errors even after error correction is done. Whether the audio data has the potential to have errors or not is decided when the C2PO data from the ECU block is decoded. If it is decided that there are errors in the audio data, a new audio data value is found using the most recent error-less data before the current one, and the error-less data which follows. The handling of audio data with possibility of errors brings the error concealment effect. This is under the assumption that the continuing audio data value is similar to nearby values. If there are no errors in the audio data, the said data is output as is.

The interpolation algorithm used in CDP is linear interpolation. In other words, when carrying out interpolation, the average of the error-less previous and following two values are used for calculating the output value, and if erroneous data come in sequentially as input of interpolation block, the most recent error-less audio data value is maintained.

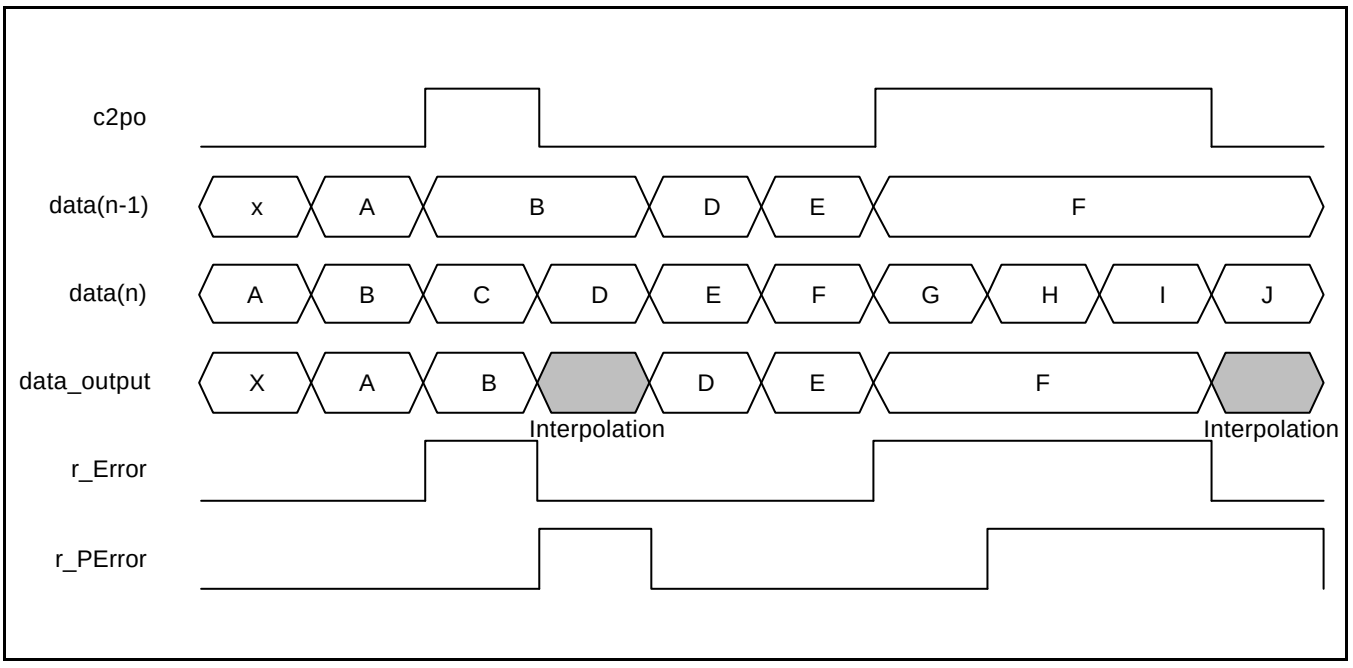


Figure 15. Interpolation

AUDOUT

The AUDOUT block transforms the 16-bit parallel data input from the INTERPOLATION block according to audio mode format. The audio format supported by S5L9232 is shown in Figure below.

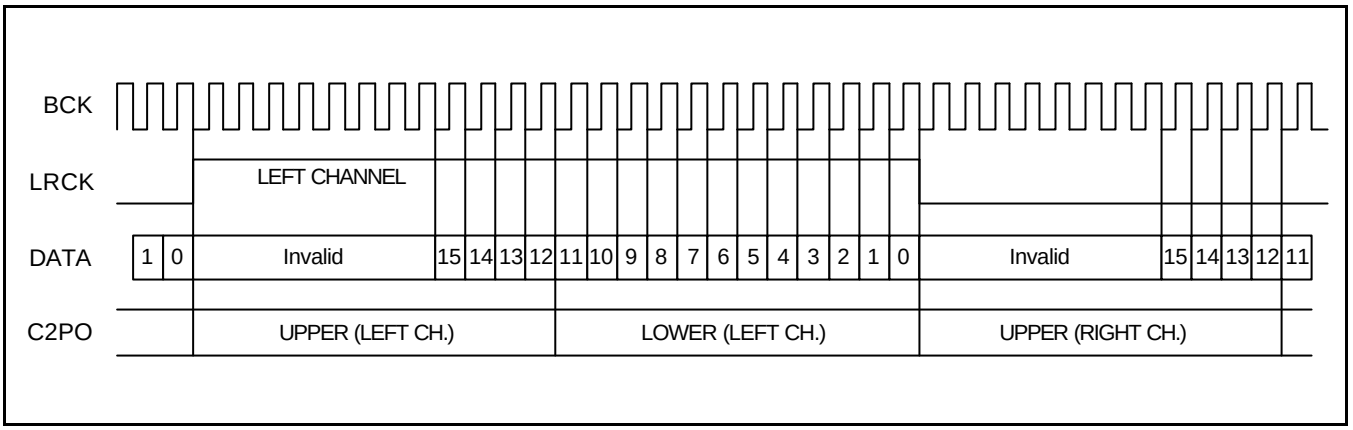


Figure 16. Audio output protocol for CD-DSP (24-bit bit clock, MSB first, right channel low, c2po MSB first, data latch timing negative edge)

DIGITAL AUDIO OUT

The Digital Audio Interface block serially transmits the information recorded in the CD to nearby parts. This interface method has the advantage of communicating using only one pin, and does not need other pins such as clocks. Because of this advantage, it is used not only in audio systems designed for home use, but also those for professional use. This interface is used only in normal speed.

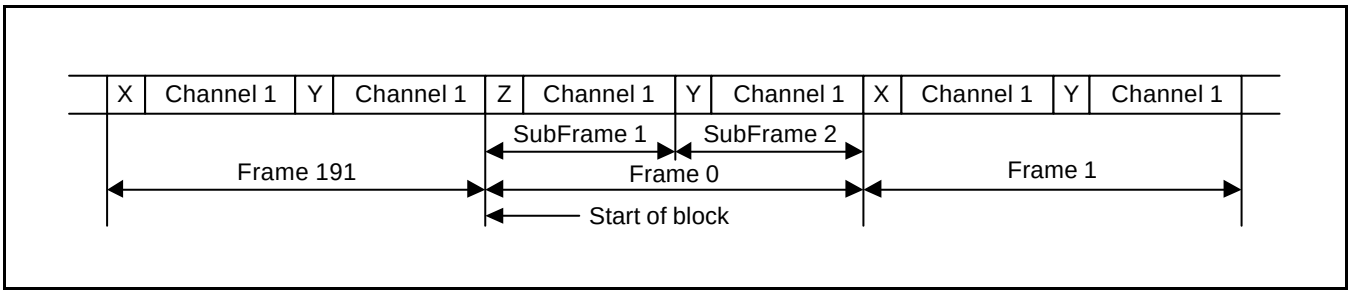


Figure 17. Digital Audio Out

SPDIF (Sony-Philips Digital audio Interface)

Because the Digital Audio Interface method for CD was originally suggested by Sony and Philips, it is called SPDIF, and its stipulations are listed in the AES (Audio Engineering Society). Data is transmitted serially and is sensitive to background noise. To overcome this, the digital out data is transmitted after being demodulated to bi-phase condition. This is accomplished as follows: Phase0 is set as a different value from the previous data's phase1 value, and if the source data of phase1 is "0", the same value as that of phase0 is set. If the source data is "1", a different value from phase 0 is set.

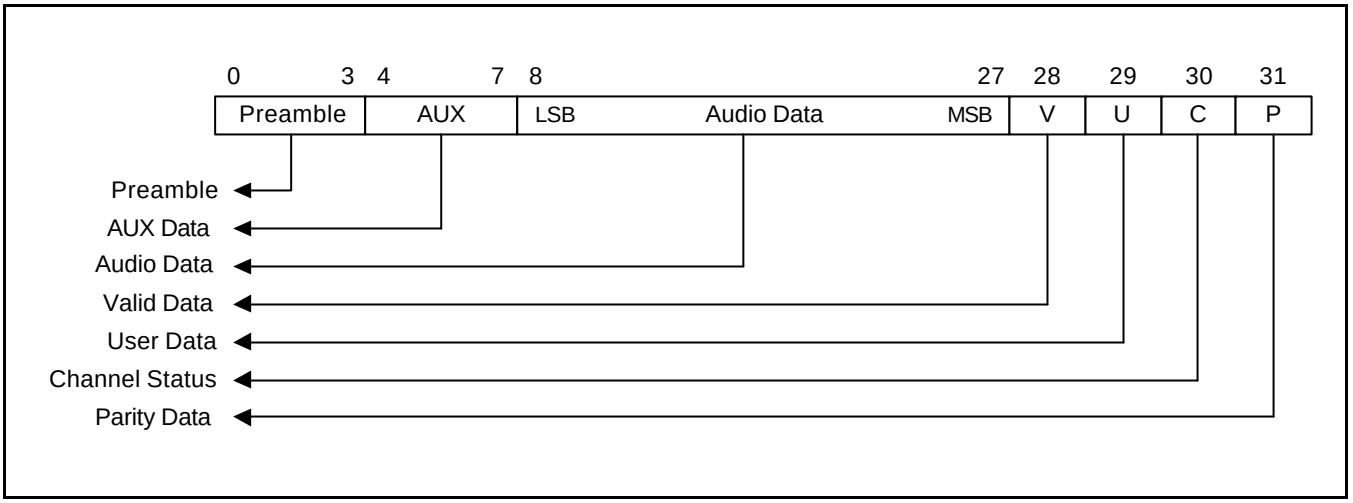


Figure 18. SPDIF

Structure of Format

Each sub-frame is made of 32 time slots, and the sub-frame includes audio data. Two sub-frames make one frame, and it has Left and Right stereo signal components. 192 frames make 1 block, which is the information unit of a control bit.

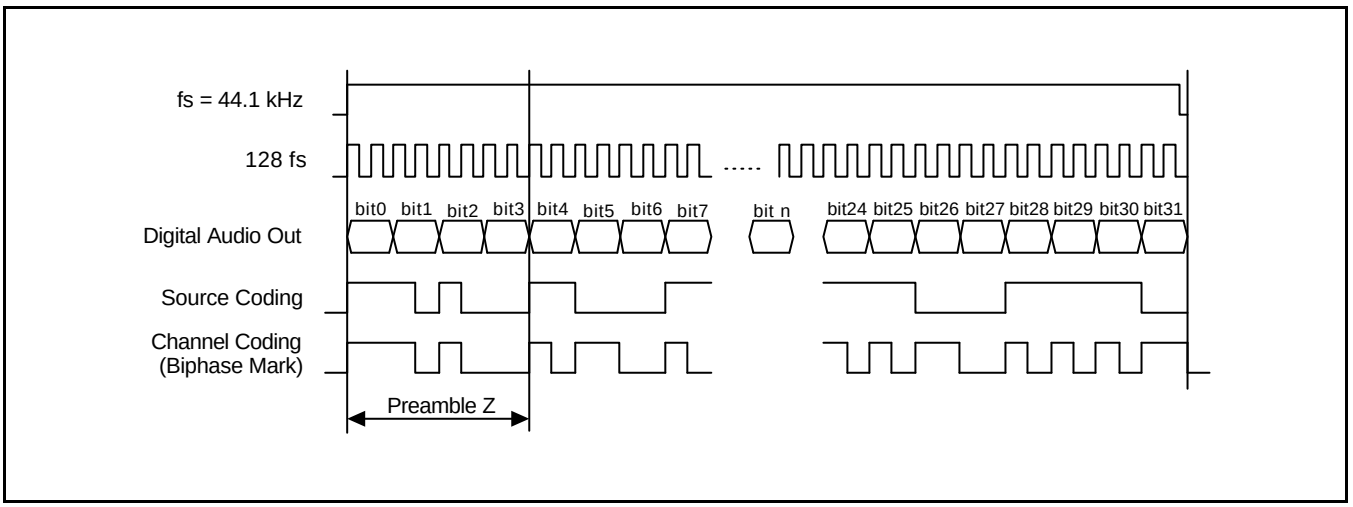


Figure 19. Sub-frame Format

Sub-frame Format

Preamble (4-bit): The preamble has the sync information of each sub-frame and block, and to maintain the original characteristics of sync data, the preamble data is not changed into bi-phase signal. But it is started as the opposite value from the previous symbol phase1 value. The preamble needs three patterns to distinguish left and right, and to show the start of the block. The patterns are as follows.

Preceding State	0	1	
	Channel Coding		
"X"	11100010	00011101	Sub-frame 1
"Y"	11100100	00011011	Sub-frame 2
"Z"	11101000	00010111	Sub-frame 1 and Block Start

Preamble X is channel 1's sync, and preamble Y is channel 2's sync. To show the start sync of a block, preamble Z is used. The reason why there are two sync patterns for each preamble is that the value is reversed according to the previous data's phase.

AUX (4-bit) : Auxiliary data area
Audio Data (20-bit) : The resolution of the audio data transmitted to digital out is basically 16-bit for CD, but you can expand to 20-bit, or even 24-bit by expanding the audio data area to the AUX area. This area is LSB first.
Validity Bit (1-bit) : If the audio sample word can be changed into analog audio signal, the validity bit is set to "1", and if not, set to "0". For CDs, it is set to "0". User data (1-bit) : For CDs, subcode data is transmitted using this area.
Control Status Data (1-bit) : Information is input for each sub-frame, and you need 192 sub-frames to make one control status data. This area has the consumer mode and professional mode, and the S5L9232 supports the consumer mode. For CDs, the control status data has the following meaning.

Bit	Control status data
0	0 : Consumer use, 1 : Professional use
1	0 : Normal Audio, 1 : Non audio Mode
2	0 : Copy Prohibit, 1 : Copy Permit
3	0 : No Pre-emphasis, 1 : Pre-emphasis
4	Reserved (= 0)
5	0 : 2 channel, 1 : 4 channel
6 — 7	00 : mode 0, reserved
8 — 15	10000000 : 2 channel CD player User bit channel = CD Subcode V bit optional
16 — 19	Source number (= 0000)
20 — 23	Channel number (= 0000)
24 — 27	Sampling frequency : 44.1kHz =0000
28 — 29	Clock accuracy 00 : Normal accuracy 10 : High accuracy 01 : Variable speed
30 — 191	Don't care (all zero)

DATAOUT

The DATAOUT block handles the interface between the embedded ESP controller and CDDSP. The ESPEN command is an embedded ESP controller enable signal. If the ESPEN signal is "L", the embedded ESP controller is not used, and the serial data input from the AUDOUT block goes through the serial to parallel register, and is output to the DIGOUT block and DSP core as parallel 16-bit. If the ESPEN signal is "H", the audio data output from the DATAOUT block is input to the embedded ESP controller at a 2x data rate, and the data input to the DATAOUT block from the ESP controller is input in normal speed. So, the parts excepting the DPLL and DIGOUT blocks are designed to operate at 2x if the ESPEN signal is "H". In the DATAOUT block, the output part to the DIGOUT block and the DSP core uses for parallel output, a 16-bit serial to parallel converter.
The operation carried out next in the DATAOUT block is the audio data mute control. The mute control functions supported in S5L9232 are zero-cross muting, muting, and attenuation.
Attenuation of audio signal can be executed by the ATTN and AMUTE of $AB micro-controller command as each signal is set as the table below.

Table 6. Attenuation

ATTN	AMUTE	DEGREE OF ATTENUATION
0	0	0dB
0	1	- ∞ dB
1	0	-12dB
1	1	-12dB

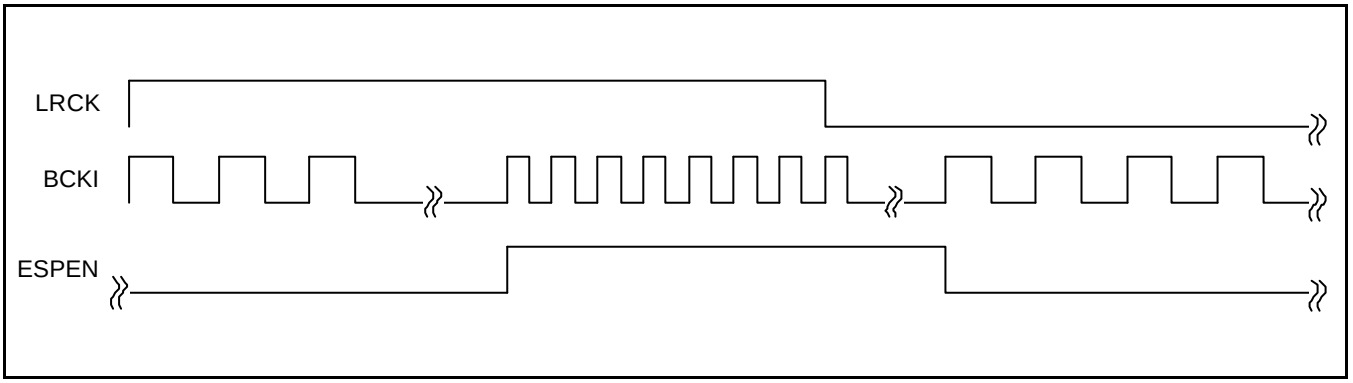


Figure 20. DATAOUT Timing Diagram

The interfacing signal formats between the ESP controller and DATAOUT are limited to the above figure.

CLV SERVO

The command registers and data related to the CLV block are shown in below table.

Table 7. CLV related MICRO-CONTROLLER command

Comments	Address D15 ¾ D08	Data								SENSE
		D7	D6	D5	D4	D3	D2	D1	D0	
CLV Gain control	E0	-	WBN	WPN	RFCK SEL	-	WB	WP	GAIN	Z
CLV mode selection	E1	UNLOCK		CLVID LE	PCEN	CM3	CM2	CM1	CM0	/CLVST
CLV control commands 1	E2	STRIO	SMM	PME	SME	PCKSEL[1:0]		PGAIN[1:0]		Z
CLV control commands 2	E3	LC	PML	SML[1:0]		POS	SGAIN[2:0]			Z
CLV control commands 3	E4	POFFSET[7:0]								Z
CLV control commands 4	E5	SPLUS	SDD	PHASEDIV[1:0]		SMOFFSET[3:0]				Z
CLV control commands 5	E6	SOFFSET[7:0]								Z

CLV Servo Mode

¾ KICK Mode (Forward Mode): The outputs of SMDP, SMDS, SMEF, and SMON are "H"(accelerate), "Hi-Z", "L", and "H" respectively.

— BRAKE Mode (Reverse Mode): The outputs of SMDP, SMDS, SMEF, and SMON are "L" (decelerate), "Hi-Z", "L", and "H" respectively.

— CLV-S Mode (Speed Mode): When track jump of EFM phase is unlocked, the speed mode roughly controls the spindle motor. The pulse width of NRZ format frame sync signal from EFM signal is exactly 22T (assuming the period of plck8M is T). But because of noise, it can exceed 22T, and in that case, the correct frame sync cannot be detected. If the maximum pulse width of the NRZ format EFM signal is smaller than 21T, SMDP becomes "L". If the pulse is 22T, it becomes "Hi-Z", and if larger than 23T, it becomes "H". If the CNTL-W register's gain is "L", SMDP's output is sent after attenuation (-12 dB), and if "H", it is output without attenuation. The outputs of SMDS, SMEF, and SMON are "Hi-Z", "L", and "H" respectively.

Table 8. Peak hold clock and Bottom hold clock's frequency

Peak hold clock frequency		Bottom hold clock frequency	
WP = 0	WP = 1	WB = 0	WB = 1
RFCK/4	RFCK/2	RFCK/32	RFCK/16

Table 9. SMDP output

Max. pulse width of Frame Sync	SMDP	
≤ 21T = 22T ≥ 23T	L Hi-Z H	⇒ if GAIN of $E0 command is 'L', SMDP output is attenuated as -12dB, otherwise('H') no attenuation is performed.

¾ **CLV-P Mode (Phase Mode):** This mode is for controlling the EFM phase. When $A2's NCLV bit is "L", the phase difference between P2WFCK/4 and RBFCK(P2RFCK/4) is detected and comes out via SMDP. When it is "H", the phase difference between RBFCK (Read Base Counter/4, P2RFCK/4) and WBFCK (Write Base Counter/4) is detected and comes out via SMDP. At this mode, SMEF output is "Hi-Z" and SMON output is "H".

where P2RFCK (= 7.35kHz) : Crystal-generated Read Frame Clocks output
P2WFCK (— 7.35kHz) : EFM-generated Write Frame Clocks output

In normal speed, if the period of 4.2336 MHz is T, and the width where WFCK is "H" is tHW, the output of SMDS is "H" for (tHW-278T)*32 at WFCKs falling edge, and then outputs "L" until the next falling edge.

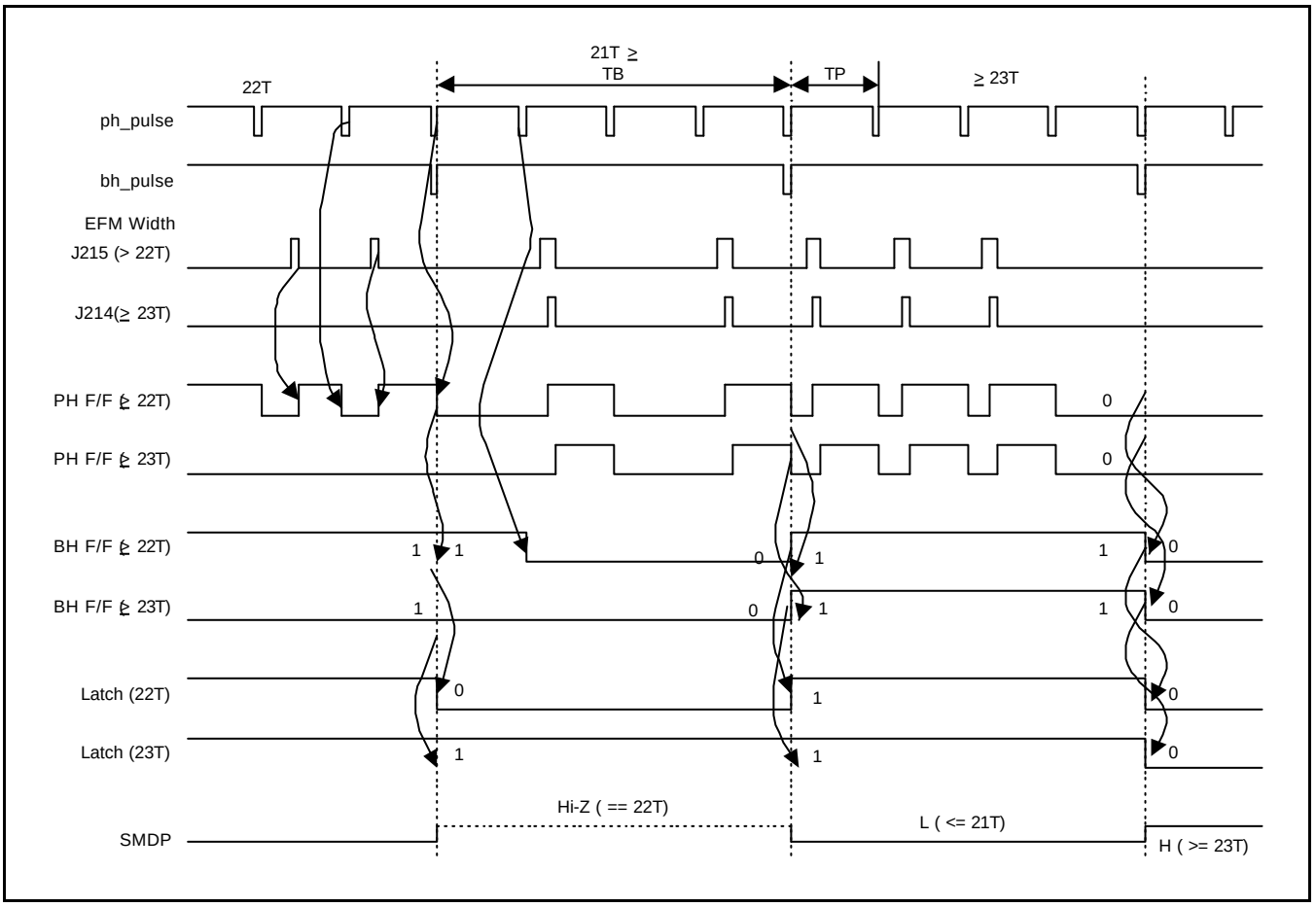


Figure 21. In CLV-S Mode, when GAIN is 'H', SMDP Output

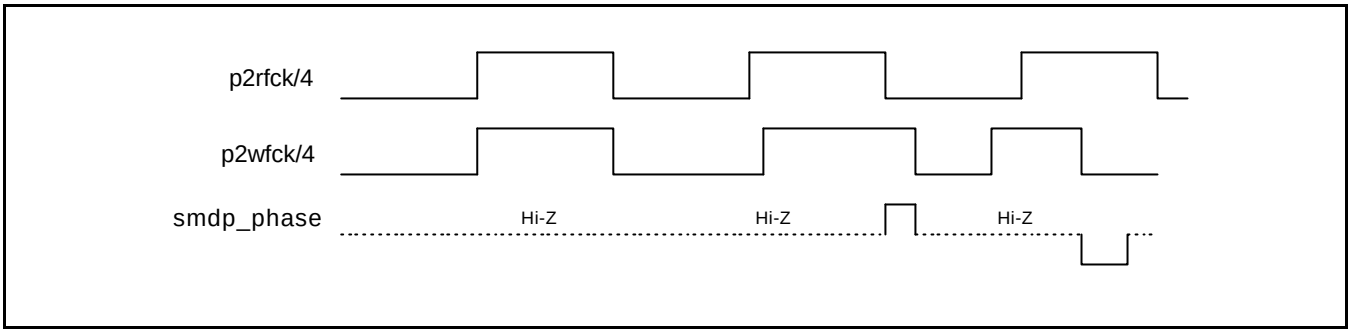


Figure 22. SMDP output in CLV-P Mode

¾ CLV-A Mode (XPHSD Mode): This mode is for normal action. The GFS generated in the EFM block is sampled at WFCK/16 period. If GFS is sampled as "H", the CLV-P mode (phase mode) is carried out, and if it is sampled as "L" 8 consecutive times, it automatically carries out the CLV mode (Speed mode). At this time, the $E0 command decides the peak hold cycle in phase mode, and the bottom holds cycle and gain in the speed mode. When PLL is locked, (LOCK=1) SMEF is "Hi-Z", and SMDS operates like SLV-P mode. When PLL is unlocked, (LOCK=0) SMEF is "L", and SMDS is "Hi-Z".

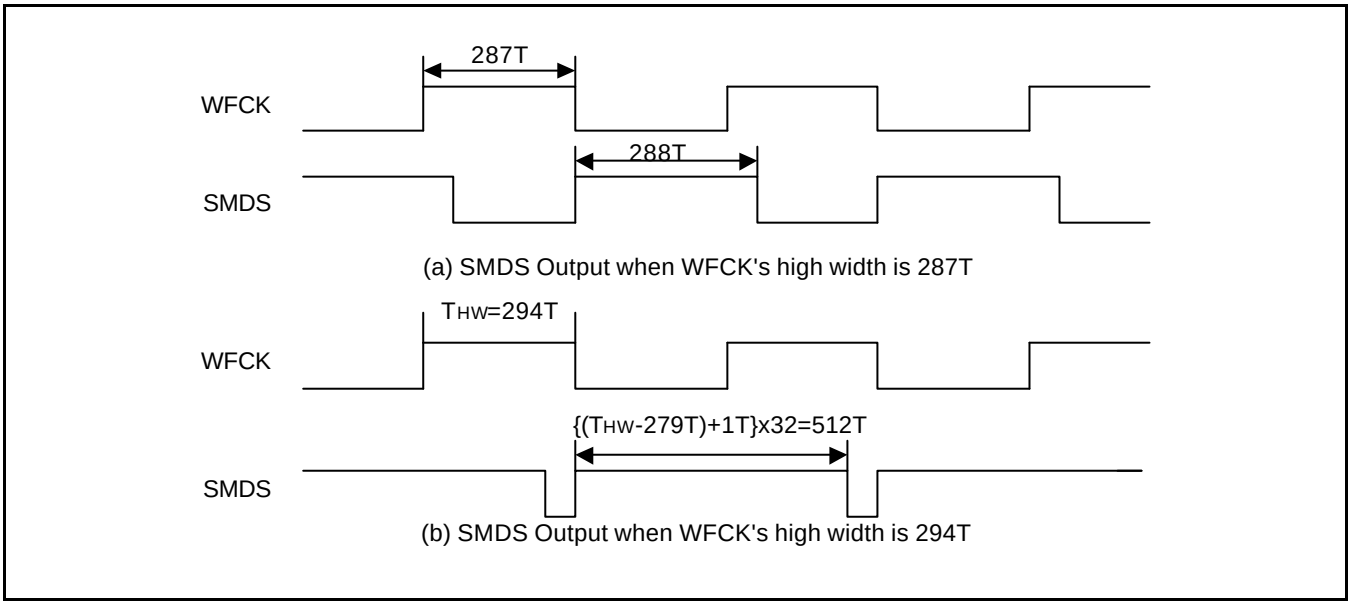


Figure 23. SMDS Output in CLV-P Mode (T:One frequency of 4.2336MHz, WFCK @ 7.35kHz)

— CLV-A Mode (VPHSP Mode): This mode is for rough servo control. To test the EFM pattern, use pll-generated 8.6436MHz clock instead of crystal clock. When 0 dB, (ATTN=0&&AMUTE=0) it operates like CLV-A mode, and if it isn't 0 dB, (ATTN=1 // AMUTE=1) GFS is 1, and SMEF is "Hi-Z", and SMDS operates like CLV-P Mode. When GFS is 0, SMEF is "L", and SMDS is "Hi-Z".

— STOP Mode: This mode is to stop the spindle motor. The outputs of SMDP, SMDS, SMEF, and SMON are "L", "Hi-Z", "L", and "L"-Spindle Motor Off respectively.

LOCK Generation

This is the period of WFCK (1x: 7.35 kHz, 2x: 7.35*2 kHz). According to the micro-controller command LC ($E3), LOCK is generated as in the table below. In other words, whether it is 1x or 2x, after GFS becomes "L", lock status is maintained for 127 frames. Since the LOCK is synchronized to WFCK, GFS default action takes place when LC is "0".

Table 10. Lock control (T: Frequency of WFCK)

	Normal	Double
LC = 0	127T	127*2T
LC = 1	127T	127T

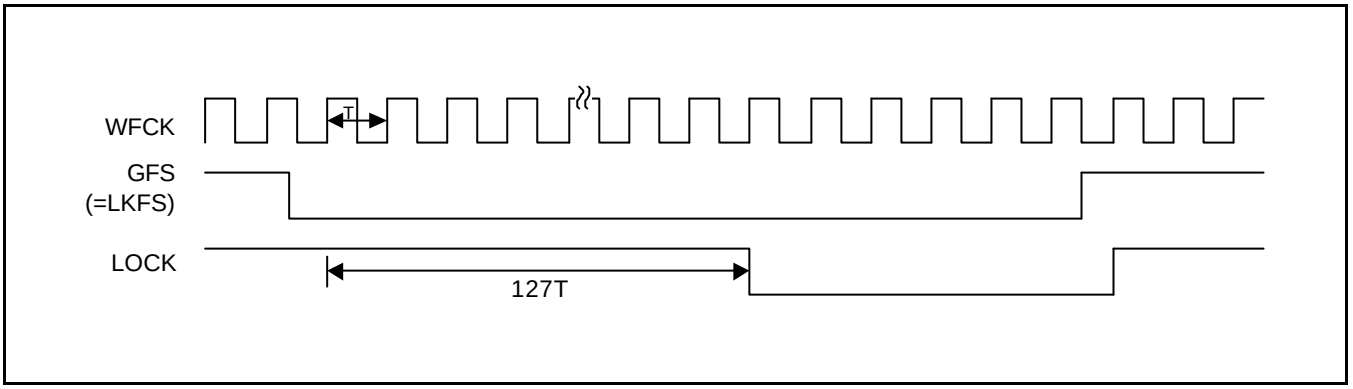


Figure 24. LOCK generation (LC= '1')

PLL

Functional Block Diagram

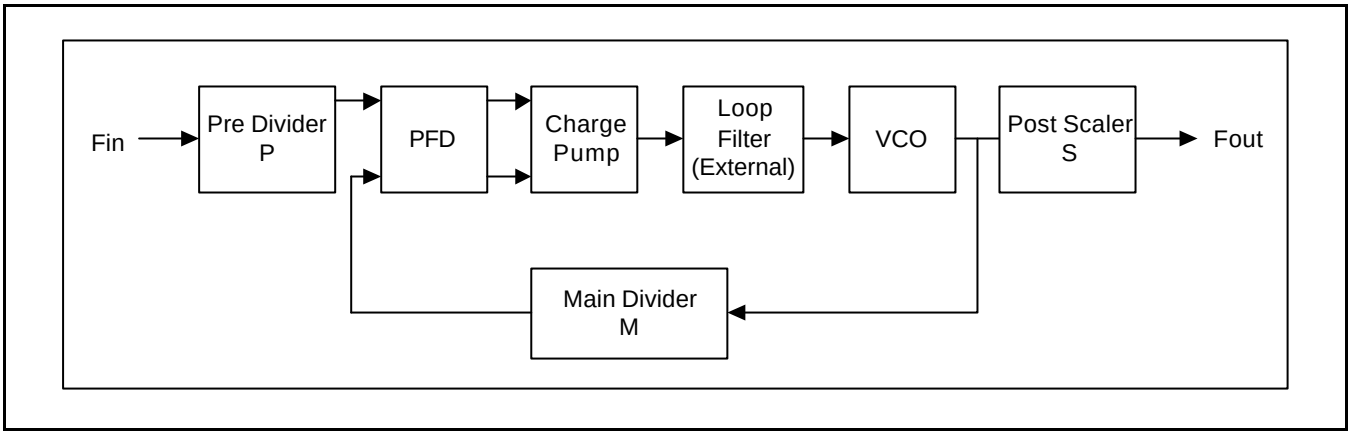


Figure 25. Phase Locked Loop Block Diagram

Functional Descriptions

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.
In this application, it includes the following basic blocks.

- The voltage-controlled oscillator to generate the output frequency
- The divider P divides the reference frequency by p
- The divider M divides the VCO output frequency by m
- The divider S divides the VCO output frequency by s
- The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.
- The loop filter removes high frequency components in charge pump voltage and does smooth and clean control of VCO

The m, p, s values can be programmed by 16bit digital data from the external source. So the PLL can be locked in the desired frequency.

Fout = m * Fin / p*s

where Fin = 14.318MHz, and m = M+8 , p = P+2, s = 2^S

Digital data format:

Main Divider	Pre Divider	Post Divider
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S0, S1

NOTES

1. S1 - S0 : Output Frequency Scaler
2. M7 - M0 : VCO Frequency Divider
3. P5 - P0 : Reference Frequency Input Divider

1-BIT DAC

This product is ΣΔ Digital-To-Analog Converter for digital audio System (CDP). The product contains Serial-to-Parallel Converter and Compensation Filter, Digital Volume Attenuate by the MICRO-CONTROLLER Interface, De-Emphasis Filter, FIR filter, Sinc Filter, digital sigma-delta modulator, analog post-filter, AIF (Anti-Image-Filter). The normal input and output channels provides 95dB SNR (Signal to Noise Ratio) over in band (20kHz).

The product employs the 1bit 4th-order sigma-delta architecture with 16bit resolution, over sampling of 64X. And analog post-filter with low clock sensitivity and linear phase, filters the shaping-noise and outputs analog voltage with high resolution. An on-chip reference voltage is included to allow single supply operations.

FEATURES

— 16bit ΣΔ Digital-To-Analog Converter
— Built-in Analog Post-filter
— Filtered Line-Level Outputs, Linear Phase Filtering
— 95dB SNR
— Sampling Rate 32kHz/44.1kHz/48kHz
— Input Rate 1Fs or 2Fs by Normal Mode/Double Mode Selection
— Zero Input Detection Mute
— Built-in Compensation Filter
— Input Volume Attenuate by the MICRO-CONTROLLER Interface
— Built-in De-Emphasis Filter (32kHz/44.1kHz/48kHz)
— Built-in 4 times over-sampling Digital Filter
— Low Clock Jitter Sensitivity
— 3.3V — 2.5V Power Supply

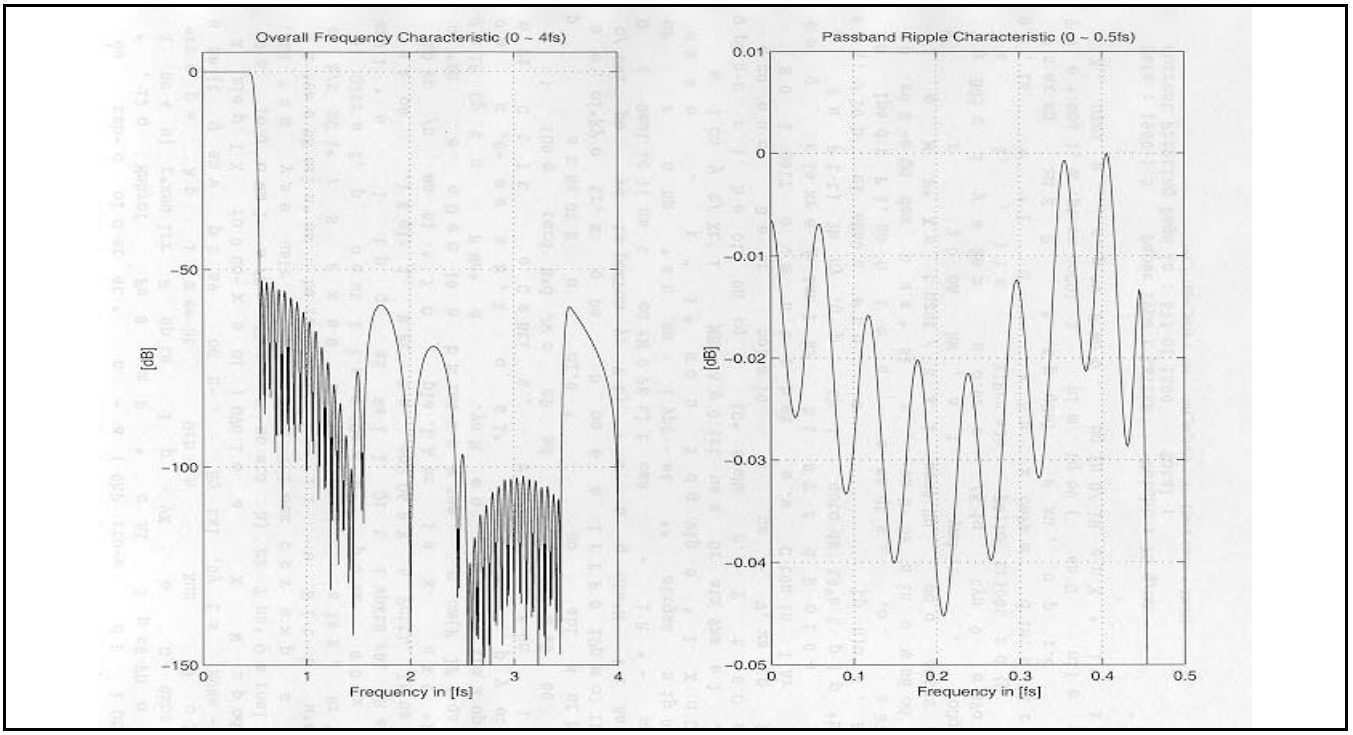


Figure 26. Overall Frequency Characteristic (left) and Passband Ripple Characteristic (Right)

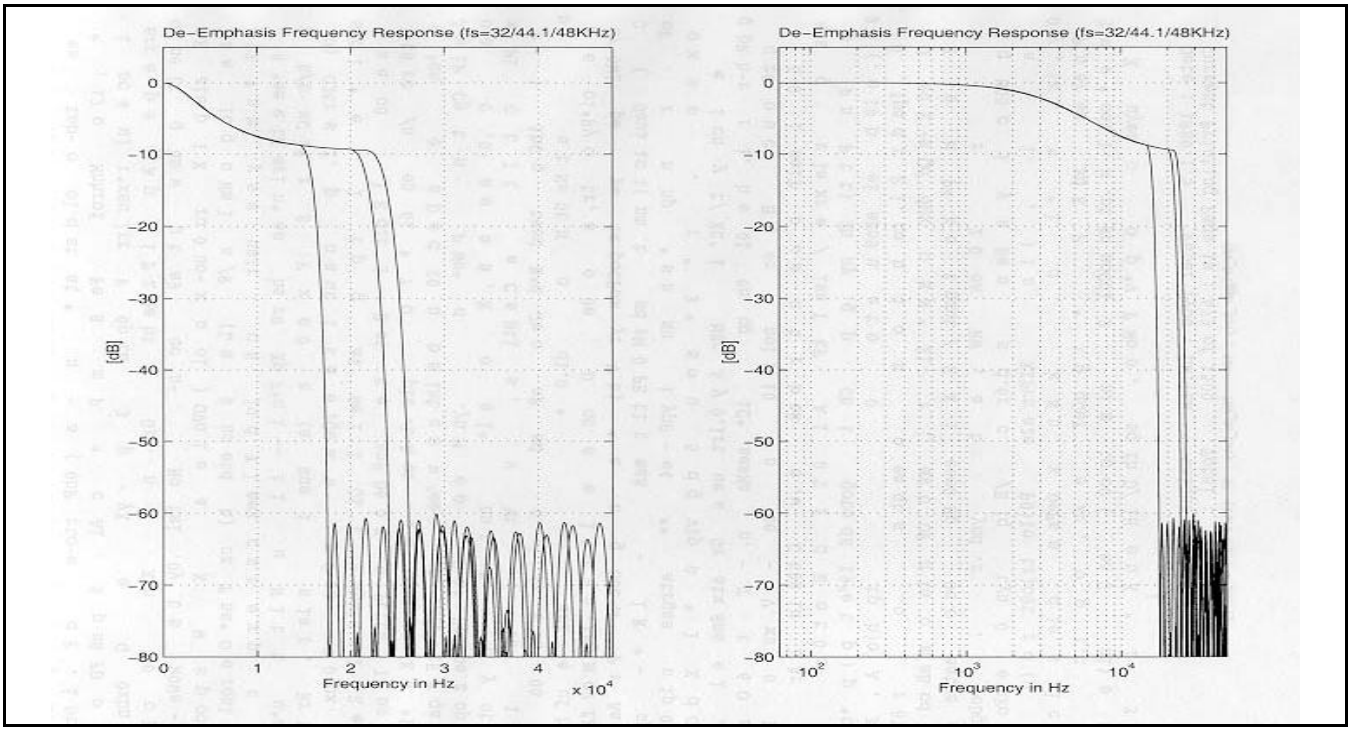
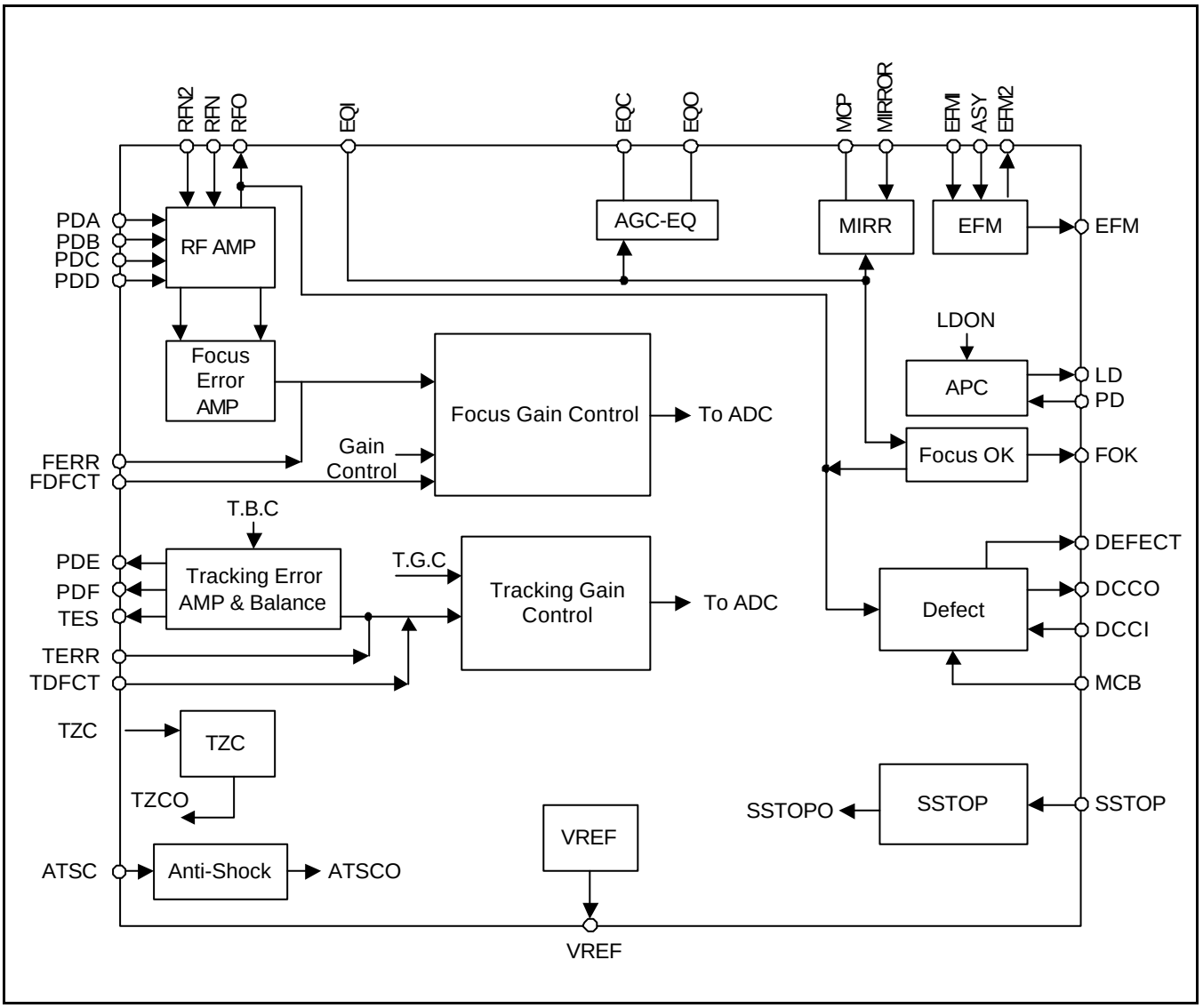


Figure 27. De-emphasis Frequency Response

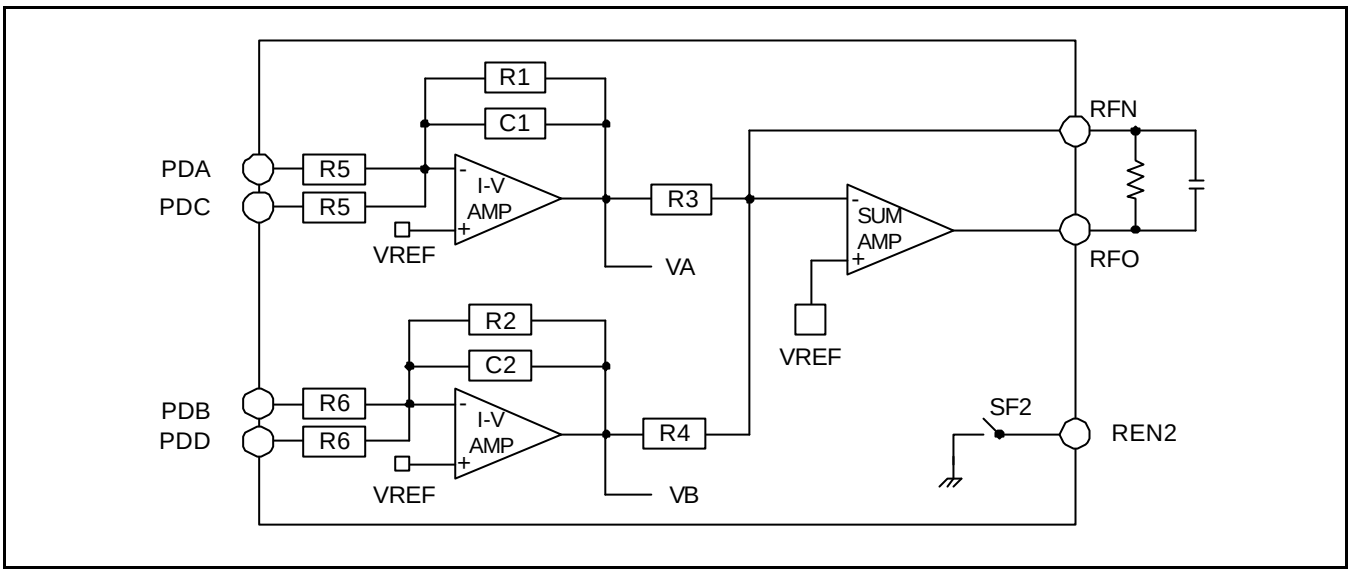
CMOS RF

The CMOS RF is the S5L9232's analog block, and it fulfills the function of receiving (from pick-up) and handling EFM, focusing/tracking RF signals, and sending them to servo.



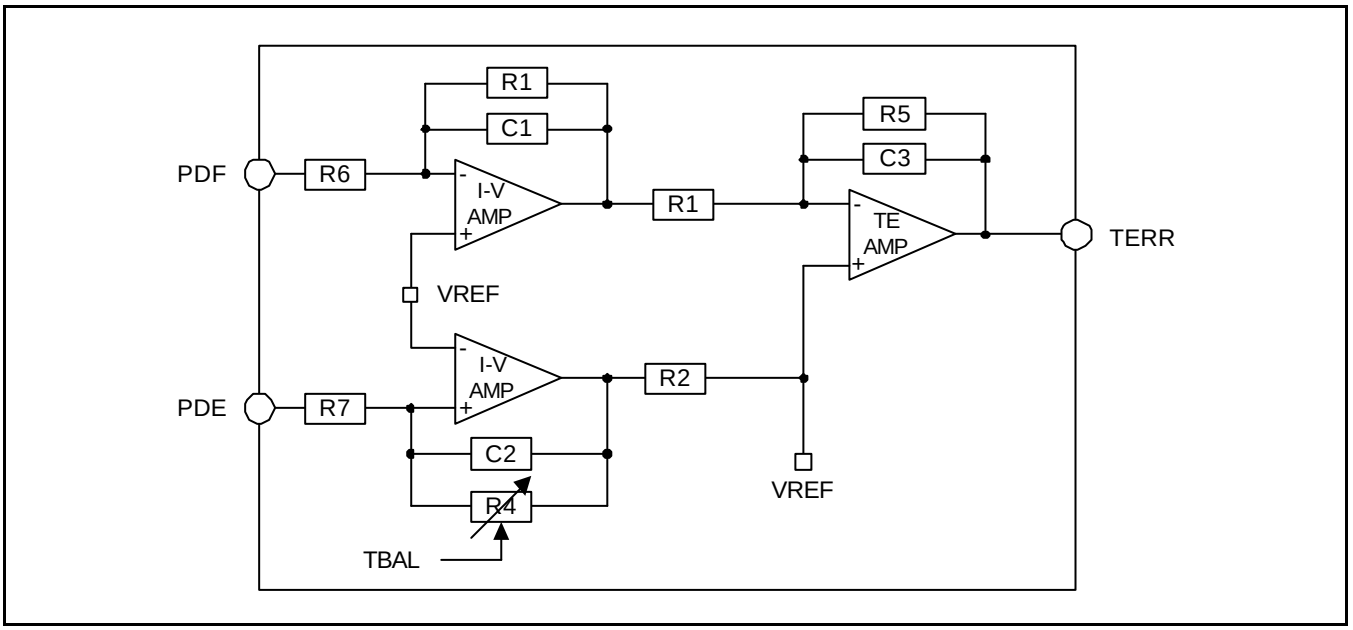
RF AMPLIFIER

The Photo Diode's input into the input pins PDA,B,C,D, are transformed from current to voltage in the RF I/V AMP. The Photo Diode (A+B+C+D)'s transformed voltage value is output to the RFO block. Also, this RF Amplifier Block supports CD-RW Disc. There are 4 modes (1X,2X,3X,and 4X) according to the values of Variable R1 and R2, which are set by MICRO-CONTROLLER command.



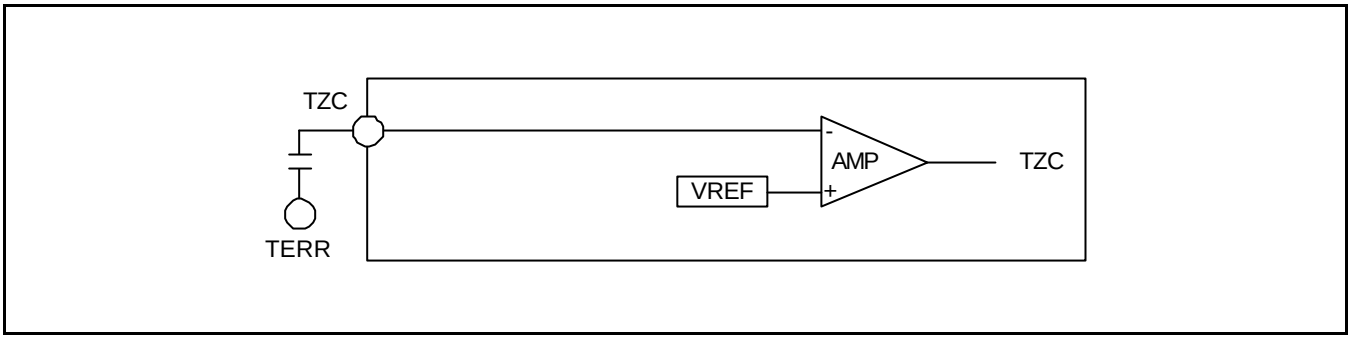
TRACKING ERROR AND BALANCE BLOCK

The Side Spot Photo Diode current input into PDE and PDF blocks, goes through I-V AMP and is converted into voltage, and the difference is gotten from the Tracking Error AMP. The MICRO-CONTROLLER programming carries out the balance adjustments by adjusting the PDE blocks gain. Also, this RF Amplifier Block supports CD-RW Disc. There are 4 modes (1X,2X,3X,and 4X) according to the values of Variable R3 and R4, which are set by MICRO-CONTROLLER command.



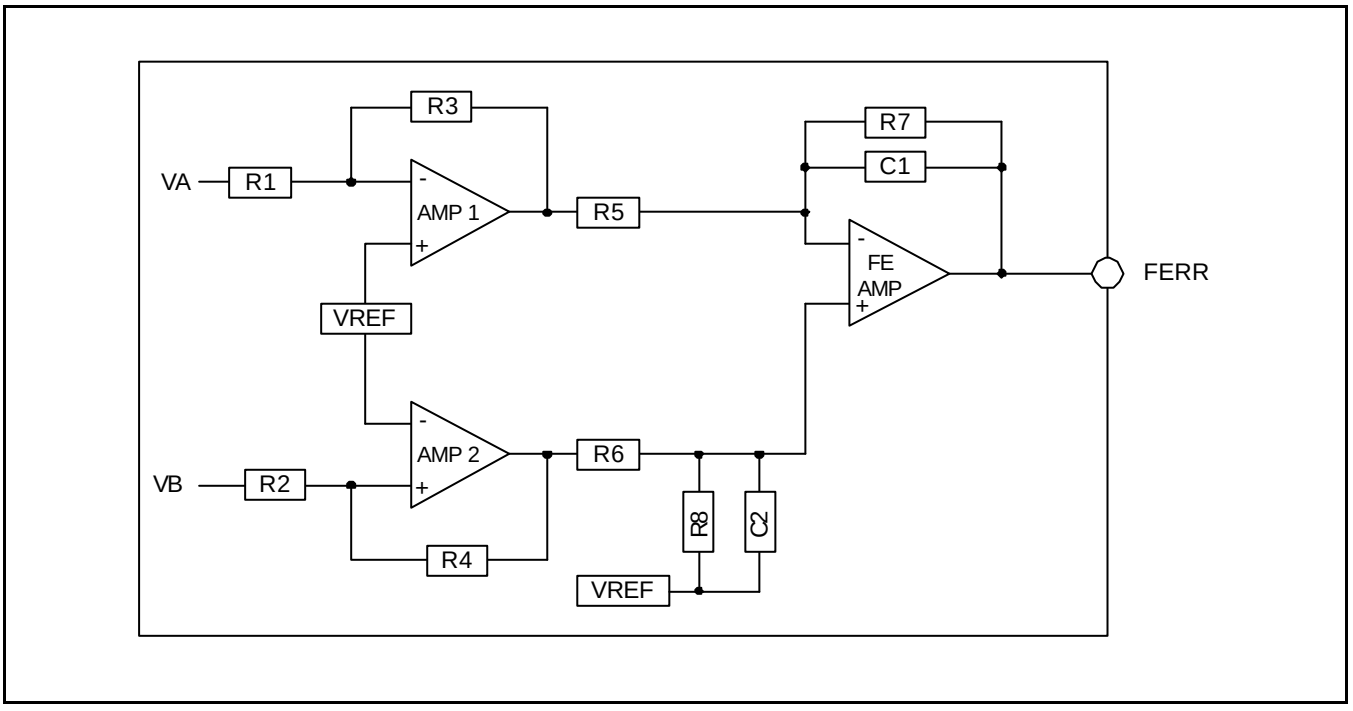
TRACKING ZERO CROSS

The TZC carries out the function of changing the TE signal to digital. It receives TE input from the RF, passes it through the voltage follower, and then compares it to the standard voltage. The TZCI connects a capacitor to the input to receive the TE signal as input and is buffered to send out digital output as TZC. TZC is applied when phase compensating within the tracking servo, TZC is applied to activate the pick-up by sending the compensated value to the tracking activation block.



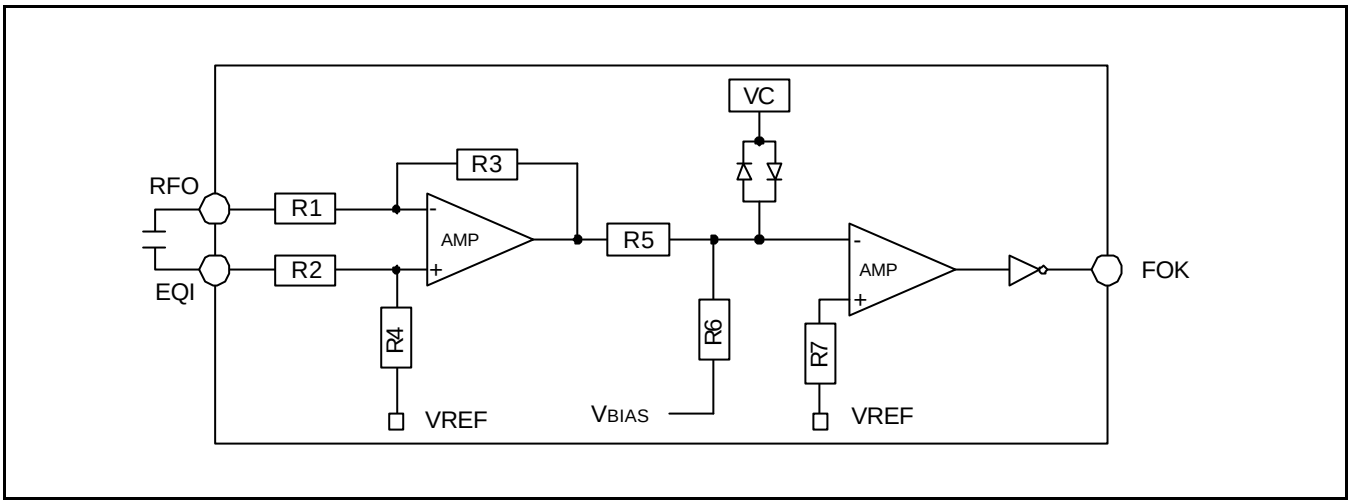
FOCUS ERROR AMP AND BALANCE BLOCK

This block takes the difference between the RF I-V AMPs output VA and the RF I-V output VB, and outputs the Photo Diode ((A+C)-(B+D))'s I-V transformed voltage.



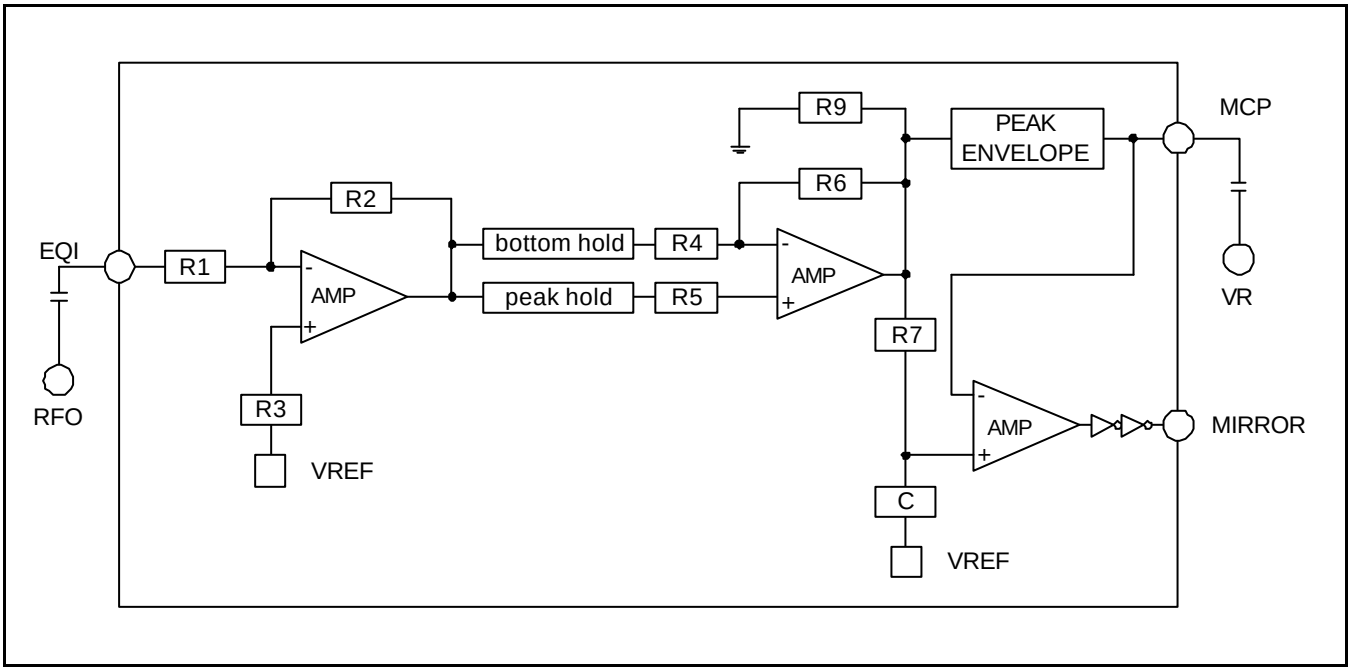
FOCUS OK

EQI and RFO blocks' DC components are extracted and compared with the standard DC values. If the RF level is above standard, FOK is output to make the timing window, which carries out focus "on" while in focus search status by the Focus OK circuit.



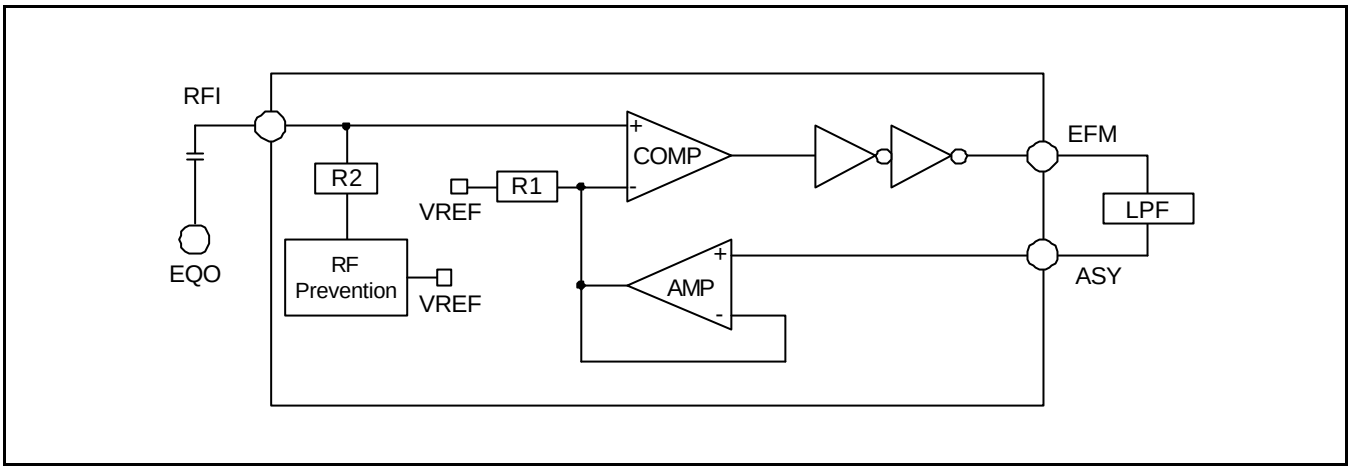
MIRROR

The EQI signal is amplified and then carries out the peak and bottom hold. Peak hold can follow up to 100 kHz traverses, and bottom hold can follow the envelope changes of the radiation frequency. Mirror output above 1 kHz on the discs track is "L", and between tracks is "H". If a defect above 1.4 ms is detected, it is also "H".



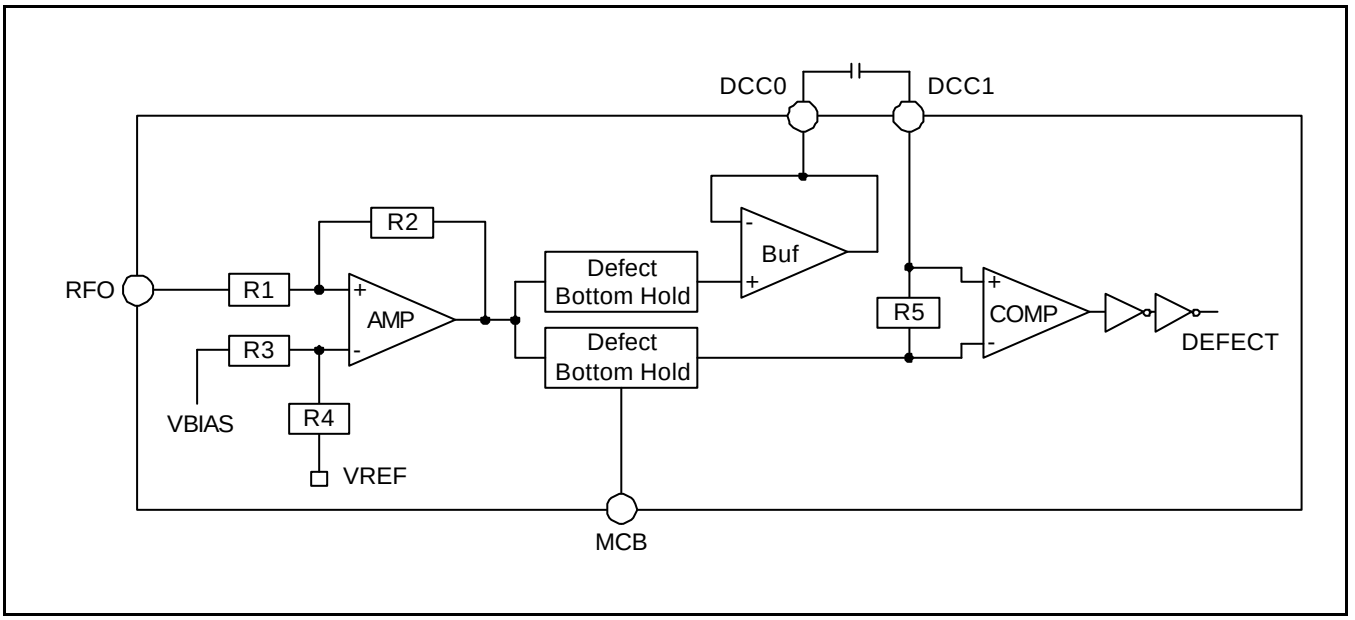
EFM SLICER

The EFM comparator changes the RF signal to binary signal. Asymmetry generated during disc production cannot be eliminated by the AC coupling, but by adjusting the EFM comparators standard voltage.(Embedded RF Peaking Prevention Circuit & Asymmetry Hold Circuit)



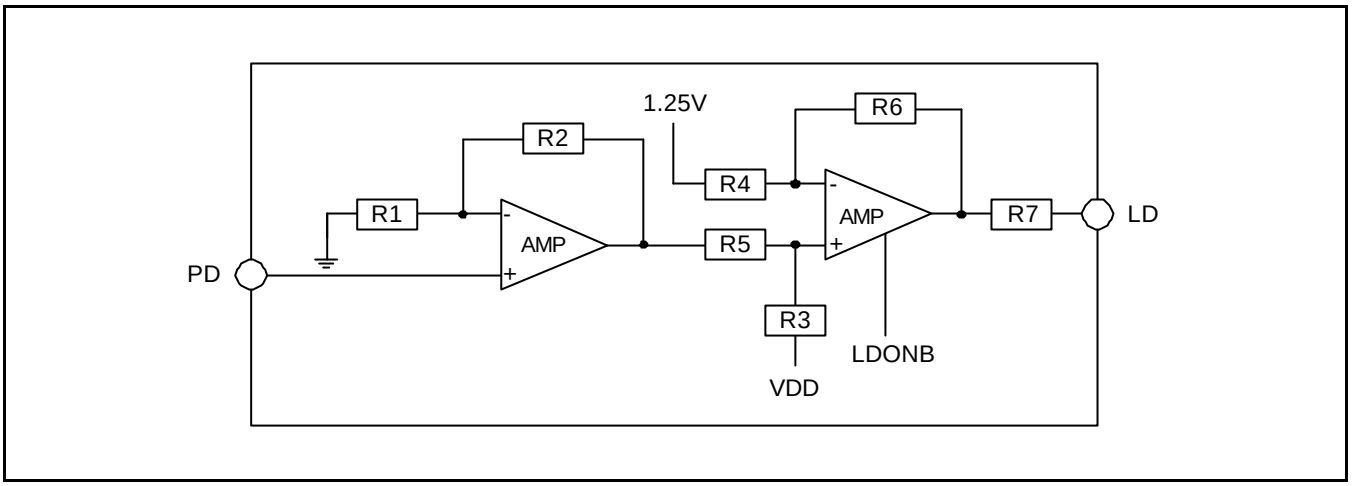
DEFECT DETECTION FUNCTION

After inverting the RFO signal, bottom hold is carried out by 2 kinds of the time constants, which are long and short. The bottom hold of the time constants holds the defect level just before the defect. The level is differentiated by coupling, then level shifted to compare the signals of both directions to generate the defect detection signal.



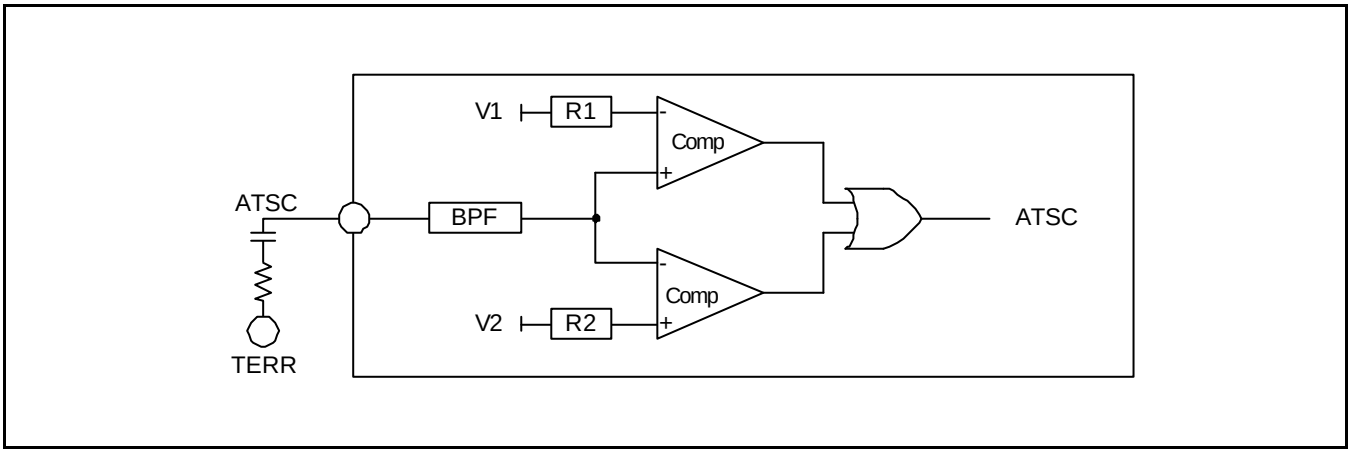
AUTOMATIC POWER CONTROL FUNCTION

If you use it in the constant current state, the laser diode has a negative temperature characteristic with a large optical output, and this function controls the monitor photo diode's output so that it is regular.(P-SUB Only)



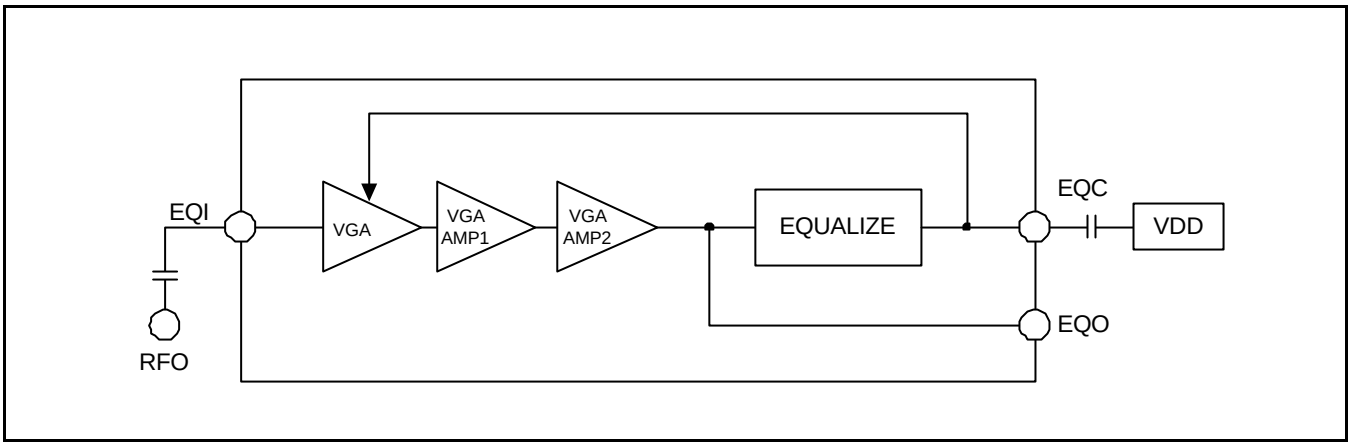
ANTI-SHOCK FUNCTION

A defect circuit for tracking gain improvement against shock is configured as a window comparator. This circuit detects physical shock from external factors during disc playback. Regular tracking error signal has a very small value, but for external shock, the error value is very large. So if the width of change is large in the TEs level, "H" is output.



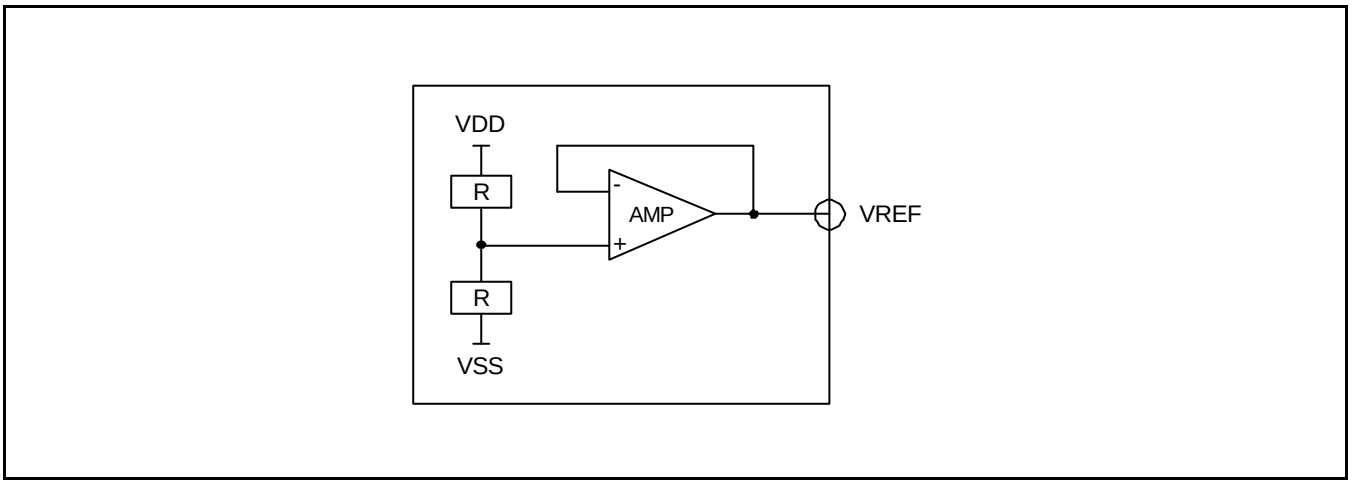
AUTOMATIC GAIN CONTROL FUNCTION

The AGC block, which has a 3T gain boost feature, maintains the RF peak to peak level at a certain level. The block detects the RF envelope, compares it to standard voltage, and then adjusts the gain. It also receives RF output, stabilizes the RF level to 1Vpp, and applies this output as EFM slice input.



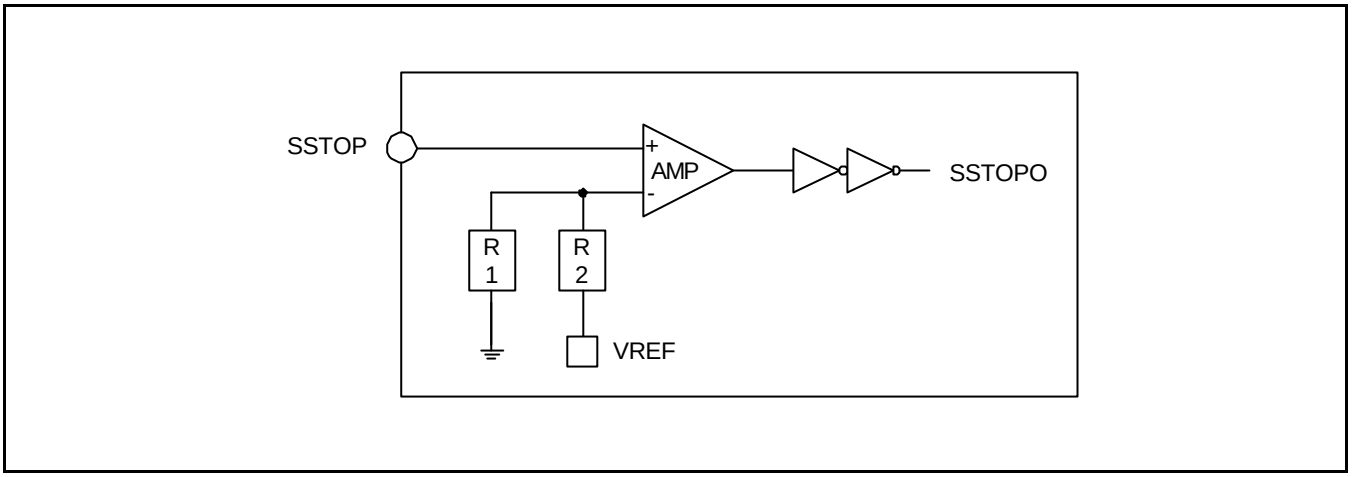
REFERENCE VOLTAGE GENERATOR

This generator makes reference voltage using the resistance divider.

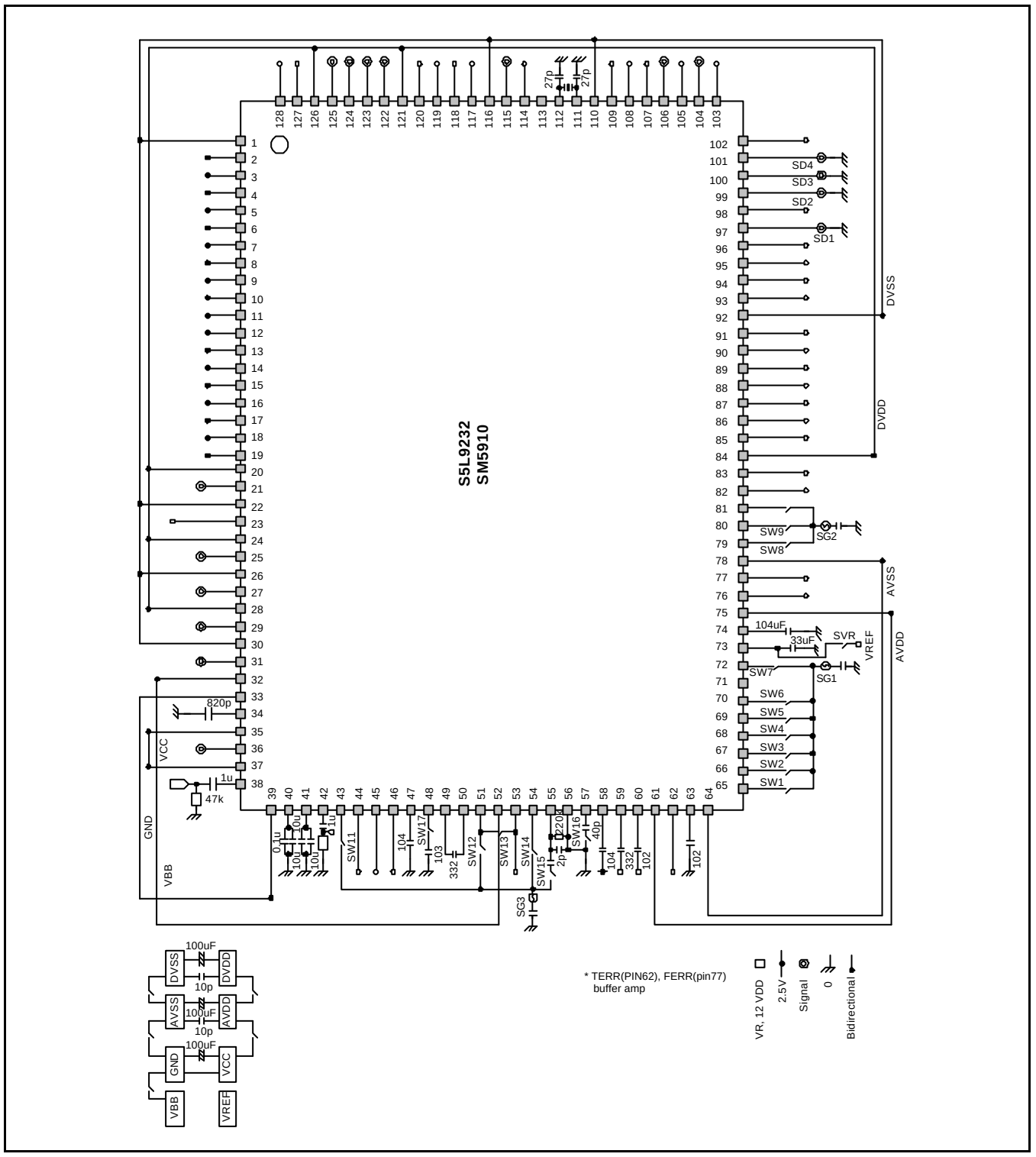


SSTOP BLOCK

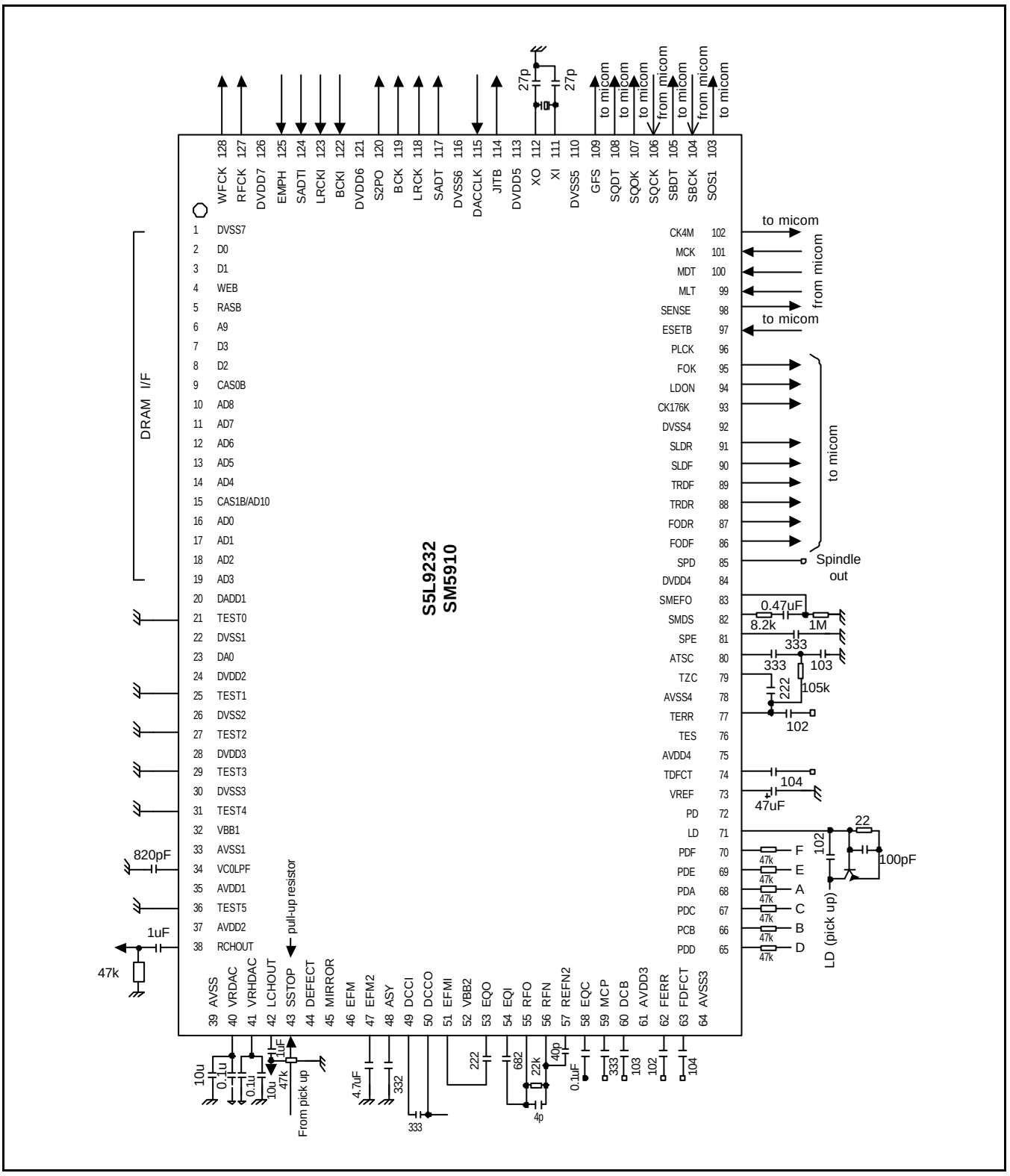
When the pick-up is at the innermost circumference of the disc, the SSTOP block generates the stop signal.



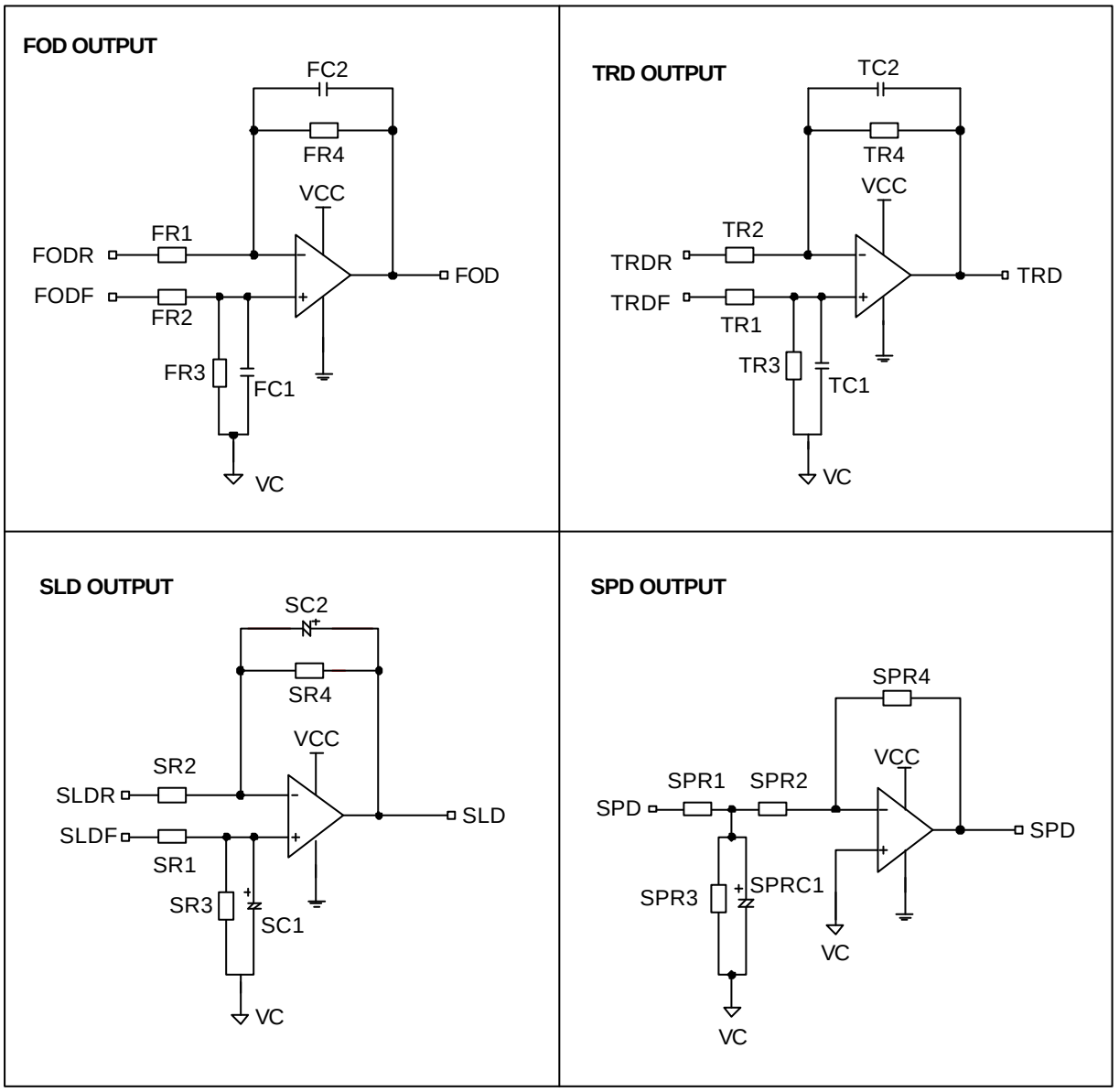
TEST CIRCUIT



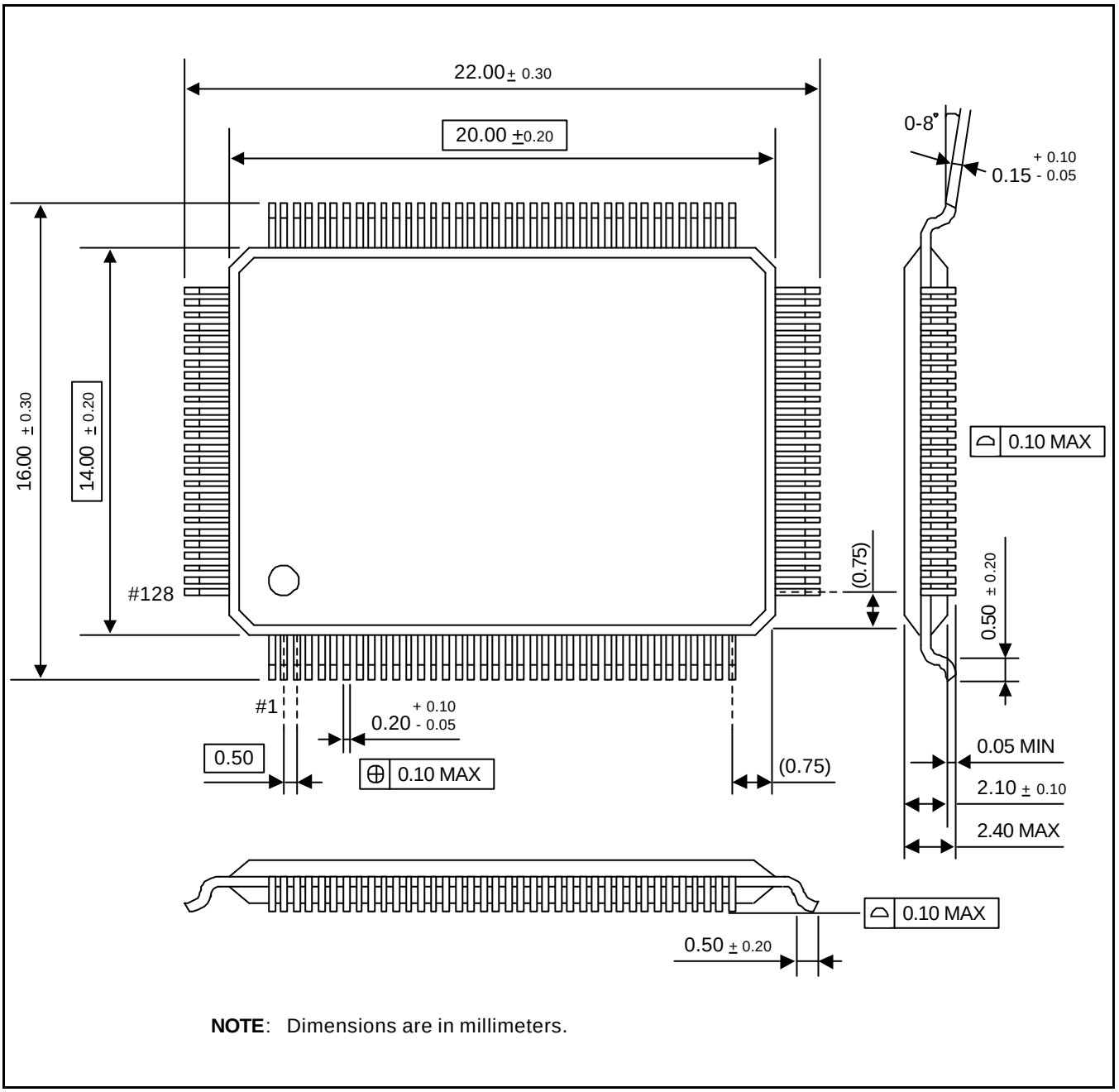
APPLICATION CIRCUIT



APPLICATION CIRCUIT (CONT.) FOR PWM OUTPUT



PACKAGE DIMENSION



NOTE: Dimensions are in millimeters.