

TENTATIVE

TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

8,388,608-WORD BY 72-BIT SYNCHRONOUS DRAM MODULE

DESCRIPTION

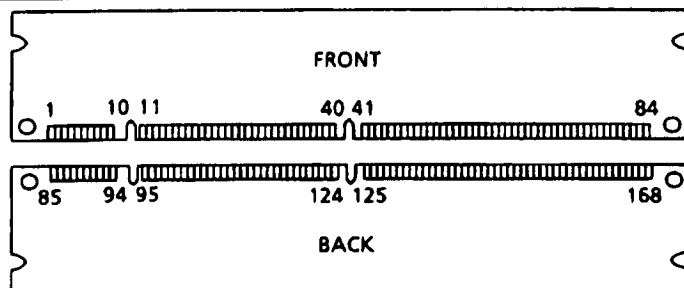
The THMY7280F1BEG is a 8,388,608-word by 72-bit synchronous dynamic RAM module consisting of nine TC59S6408BFT DRAMs and an unbuffer on a printed circuit board.

FEATURES

- 8,388,608-word by 72-bit (single-bank) organization
- Single power supply of $3.3\text{ V} \pm 0.3\text{ V}$
- Pipeline architecture
- Auto-refresh and Self-refresh capability
- All inputs and outputs LVTTL-compatible
- 4096 refresh cycles per 64 ms
- Package: 168-pin DIMM Gold contacts
- Based on Intel PC100

	-80
t_{CK} Clock Cycle Time (CL = 2)	10 ns
t_{RAS} Active-to-Precharge Command Period (min)	48 ns
t_{AC} Access Time from CLK (CL = 2)	6 ns
t_{RC} Ref/Active-to-Ref/Active Command Period (min)	68 ns

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A11	Address Inputs
BA0, 1	Bank Select
DQ0 to DQ63	Data Inputs/Outputs
CB0 to 7	Check Bits
/CS0, 2	Chip Select
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQMB0 to 7	Output Disable/Write Mask
CLK0, 2	Clock Input
CKE	Clock Enable
SDA	Serial Data/Address for PD
SCL	Clock for PD
SA0 to 2	Address for PD
VDD	Power (+3.3 V)
VSS	Ground
NC	No Connection

1 VSS	85 VSS	29 DQMB1	113 DQMB5	57 DQ18	141 DQ50
2 DQ0	86 DQ32	30 /CS0	114 NC	58 DQ19	142 DQ51
3 DQ1	87 DQ33	31 NC	115 /RAS	59 VDD	143 VDD
4 DQ2	88 DQ34	32 VSS	116 VSS	60 DQ20	144 DQ52
5 DQ3	89 DQ35	33 A0	117 A1	61 NC	145 NC
6 VDD	90 VDD	34 A2	118 A3	62 NC	146 NC
7 DQ4	91 DQ36	35 A4	119 A5	63 NC	147 NC
8 DQ5	92 DQ37	36 A6	120 A7	64 VSS	148 VSS
9 DQ6	93 DQ38	37 A8	121 A9	65 DQ21	149 DQ53
10 DQ7	94 DQ39	38 A10	122 BA0	66 DQ22	150 DQ54
11 DQ8	95 DQ40	39 BA1	123 A11	67 DQ23	151 DQ55
12 VSS	96 VSS	40 VDD	124 VDD	68 VSS	152 VSS
13 DQ9	97 DQ41	41 VDD	125 CLK1	69 DQ24	153 DQ56
14 DQ10	98 DQ42	42 CLK0	126 NC	70 DQ25	154 DQ57
15 DQ11	99 DQ43	43 VSS	127 VSS	71 DQ26	155 DQ58
16 DQ12	100 DQ44	44 NC	128 CKE	72 DQ27	156 DQ59
17 DQ13	101 DQ45	45 /CS2	129 NC	73 VDD	157 VDD
18 VDD	102 VDD	46 DQMB2	130 DQMB6	74 DQ28	158 DQ60
19 DQ14	103 DQ46	47 DQMB3	131 DQMB7	75 DQ29	159 DQ61
20 DQ15	104 DQ47	48 NC	132 NC	76 DQ30	160 DQ62
21 CB0	105 CB4	49 VDD	133 VDD	77 DQ31	161 DQ63
22 CB1	106 CB5	50 NC	134 NC	78 VSS	162 VSS
23 VSS	107 VSS	51 NC	135 NC	79 CLK2	163 CLK3
24 NC	108 NC	52 CB2	136 CB6	80 NC	164 NC
25 NC	109 NC	53 CB3	137 CB7	81 NC (WP)	165 SA0
26 VDD	110 VDD	54 VSS	138 VSS	82 SDA	166 SA1
27 /WE	111 /CAS	55 DQ16	139 DQ48	83 SCL	167 SA2
28 DQMB0	112 DQMB4	56 DQ17	140 DQ49	84 VDD	168 VDD

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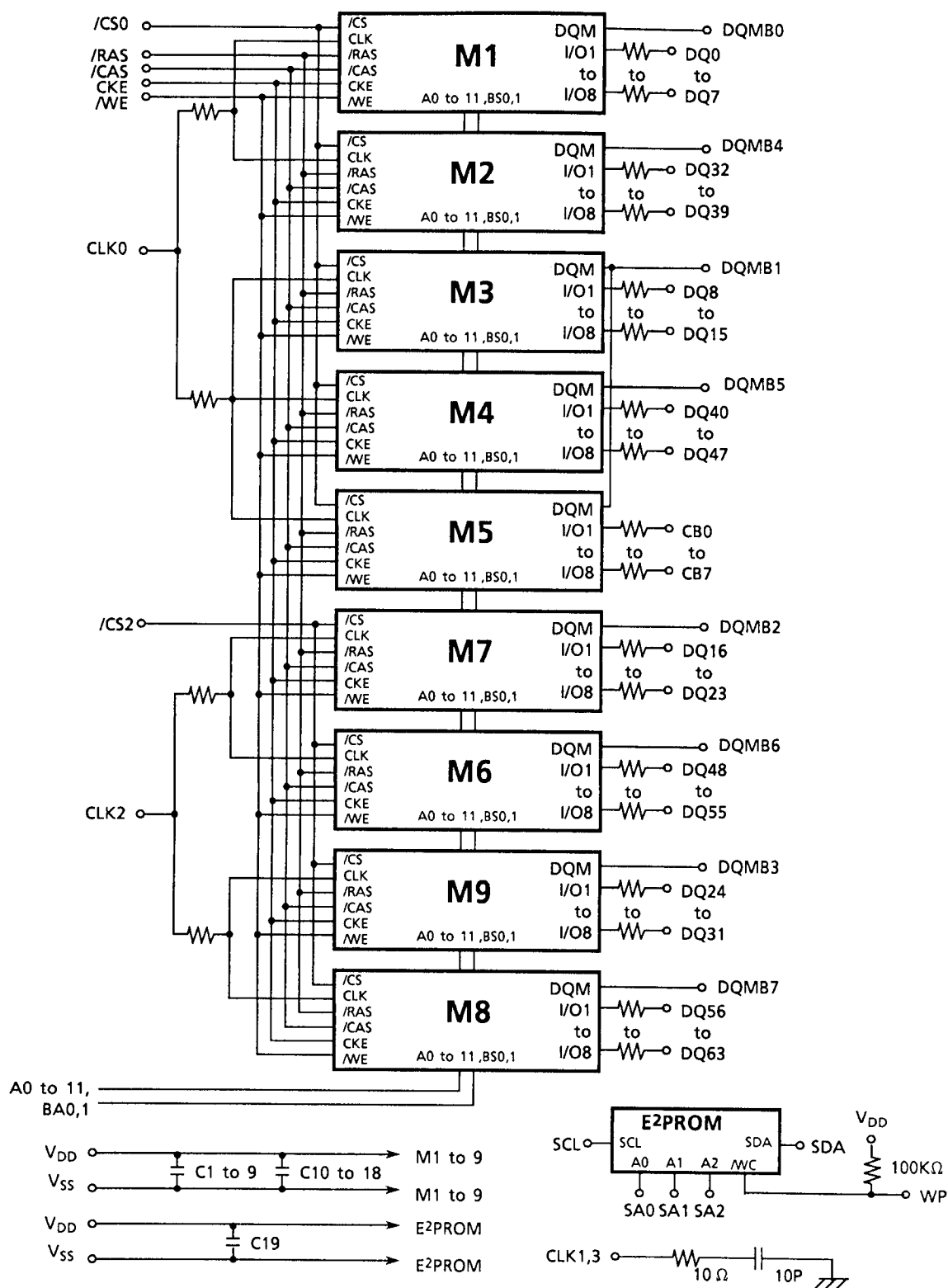
SERIAL PRESENCE DETECT (REV. 1.2A)

Byte Number	Function Described	Entry Value	Entry
0	Defines # Bytes Written into Serial Memory at Module mfg	128 Bytes	80h
1	Total # Bytes in SPD Memory Device	256 Bytes	08h
2	Fundamental Memory Type (FPM, EDO, SDRAM...) from Appendix A	SDRAM	04h
3	# Row Addresses on this Assembly	RA0-RA11	0Ch
4	# Column Addresses on this Assembly	CA0-CA8	09h
5	# Module Banks on this Assembly	1 Bank	01h
6	Data Width of this Assembly...	x72	48h
7	...Data Width Continuation	x72	00h
8	Voltage Interface Standard for this Assembly	LVTTL	01h
9	SDRAM Cycle Time at Max. Supported CAS Latency (CL), CL = X	CL = 3, 8.0 ns	80h
10	SDRAM Access from Clock @ CL = X	CL = 3, 6.0 ns	60h
11	DIMM Configuration Type (Non-parity, Parity, ECC)	ECC	02h
12	Refresh Rate/Type	15.625 μ s/Self-Refresh	80h
13	SDRAM Width, Primary DRAM	x8	08h
14	Error Checking SDRAM Data Width	x8	08h
15	Minimum Clock Delay, Back-to-Back Random Column Addresses	1 CLK	01h
16	Burst Lengths Supported	1,2,4,8 Full page	8Fh
17	# Banks on Each SDRAM Device	4 Banks	04h
18	CAS # Latencies Supported	2,3	06h
19	CS # Latency		01h
20	WE # Latency		01h
21	SDRAM Module Attributes		00h
22	SDRAM Device Attributes: General		0Eh
23	Minimum Clock Cycle Time at CL- X-1	CL = 2, 10 ns	A0h
24	Maximum Data Access Time from Clock @ CL X-1	CL = 2, 6.0 ns	60h
25	Minimum Clock Cycle Time at CL X-2		00h
26	Maximum Data Access Time from Clock @ CL X-2		00h
27	Minimum Row Precharge Time	20 ns	14h
28	Minimum Row-Active-to-Row-Active Delay	20 ns	14h
29	Minimum RAS-to-CAS Delay	20 ns	14h
30	Minimum RAS Pulse Width	48 ns	30h
31	Module/Bank Density	64 MB	10h
32	CMD & Add Input Setup time	2 ns	20h
33	CMD & Add Input Hold time	1 ns	10h
34	Data Input Setup time	2 ns	20h
35	Data Input Hold time	1 ns	10h
36-61	Superset Information (May Be Used in Future)		FFh
62	SPD Revision	Rev. 1.2A	12h
63	Checksum for Bytes 0-62	1ED8h	DBh

OPTION

64	Manufacturers JEDEC ID Code per JEP-106E		
65-71			
72	Manufacturing Location		
73-90	Manufacturer's Part Number		
91-92	Revision Code		
93-94	Date of Manufacture		
95-98	Assembly Serial Number		
99-125	Manufacturer-Specific Data		
126	Reserved	Intel Specification	64h
127	Reserved	Intel Specification	A7h
128-255			

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	- 0.3 to $V_{CC} + 0.3$	V	1
V_{OUT}	Output Voltage	- 0.3 to $V_{CC} + 0.3$	V	1
V_{DD}	Power Supply Voltage	- 0.3 to 4.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1
T_{STG}	Storage Temperature	- 55 to 125	°C	1
P_D	Power Dissipation	9.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0^\circ$ to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	-	$V_{DD} + 0.3$	V	2
V_{IL}	LVTTL Input Low Voltage	- 0.3	-	0.8	V	2

CAPACITANCE ($V_{CC} = 3.3\text{ V}$, $f = 1\text{ MHz}$, $T_a = 25^\circ\text{C}$)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_1	Input Capacitance (A0 to A11)	-	T.B.D.	pF
C_2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0,1)	-	T.B.D.	pF
C_3	Input Capacitance (CLK0,2)	-	T.B.D.	pF
C_4	Input Capacitance ($\overline{CS0}$,2)	-	T.B.D.	pF
C_5	Input Capacitance (DQMB0 to 7)	-	T.B.D.	pF
C_{DQ}	I / O Capacitance (DQ0 to DQ63, CB0 to 7)	-	T.B.D.	pF

DC CHARACTERISTICS ($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $T_a = 0^\circ\text{ to } 70^\circ\text{C}$)

SYMBOL	ITEM		MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Active-Precharge Command Cycling without Burst Operation ($t_{CK} = \text{min}$, $t_{RC} = \text{min}$)	1-Bank Operation	–	810	mA	3
I_{CC2}	STANDBY CURRENT ($t_{CK} = \text{min}$, $\overline{CS} = V_{IH}$, $V_{IH/L} = V_{IH}(\text{min}) / V_{IL}(\text{max})$ Bank: Inactive State)	CKE = V_{IH}	–	450	mA	3
I_{CC2P}		CKE = V_{IL} (Power-down Mode)	–	9		
I_{CC2S}	STANDBY CURRENT (CLK = V_{IL} , $\overline{CS} = V_{IH}$, $V_{IH/L} = V_{IH}(\text{min}) / V_{IL}(\text{max})$ Bank: Inactive State)	CKE = V_{IH}	–	90	mA	
I_{CC2PS}		CKE = V_{IL} (Power-down Mode)	–	9		
I_{CC3}	NO OPERATING CURRENT ($t_{CK} = \text{min}$, $\overline{CS} = V_{IH}(\text{min})$ Bank: Active State (2 banks))	CKE = V_{IH}	–	540	mA	3
I_{CC3P}		CKE = V_{IL} (Power-down Mode)	–	72		
I_{CC4}	BURST OPERATING CURRENT ($t_{CK} = \text{min}$, $\overline{CS} = V_{IH}(\text{min})$, Read / Write Command Cycling)		–	1080	mA	3, 4
I_{CC5}	AUTO-REFRESH CURRENT ($t_{CK} = \text{min}$, $t_{RC} = \text{min}$, Auto-Refresh Command Cycling)		–	1260	mA	3
I_{CC6}	SELF-REFRESH CURRENT (Self-Refresh Mode, CKE = 0.2 V)		–	9	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT ($0\text{ V} \leq V_{IN} \leq V_{DD}$, All Other Pins Not under Test = 0 V)		– 5	5	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, $0\text{ V} \leq V_{OUT} \leq V_{DD}$)		– 5	5	μA	
V_{OH}	OUTPUT LEVEL LVTTTL Output H Level Voltage ($I_{OUT} = -2\text{ mA}$)		2.4	–	V	
V_{OL}	OUTPUT LEVEL LVTTTL Output L Level Voltage ($I_{OUT} = 2\text{ mA}$)		–	0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 0.3 V, T_a = 0° to 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
t _{RC}	Ref/Active-Ref/Active Command Period		68		ns	9
t _{RAS}	Active- Precharge Command Period		48	100000		
t _{RCD}	Active-Read/Write Command Delay Time		20			
t _{CCD}	Read/Write(a) -Read/Write(b) Command Period		1		cycle	
t _{RP}	Precharge-Active Command Period		20		ns	
t _{RRD}	Active(a)-Active(b) Command Period		20			
t _{WR}	Write Recovery Time	CL* = 2	10			
		CL* = 3	8			
t _{CK}	CLK Cycle Time	CL* = 2	10	1000		
		CL* = 3	8	1000		
t _{CH}	CLK High Level Width		3			10
t _{CL}	CLK Low Level Width		3			
t _{AC}	Access Time from CLK	CL* = 2		6		
		CL* = 3		6		
t _{OH}	Output Data Hold Time		3			
t _{HZ}	Output Data High Impedance Time		3	8		8
t _{LZ}	Output Data Low Impedance Time		0			
t _{SB}	Power-down Mode Entry Time		0	8		
t _T	Transition Time of CLK (Rise and Fall)		0.5	8		
t _{DS}	Data-in Set-up Time		2			
t _{DH}	Data-in Hold Time		1			
t _{AS}	Address Set-up Time		2			
t _{AH}	Address Hold Time		1			
t _{CKS}	CKE Set-up Time		2			
t _{CKH}	CKE Hold Time		1			
t _{CMS}	Command Set-up Time		2			
t _{CMH}	Command Hold Time		1			
t _{REF}	Refresh Time			64	ms	
t _{RSC}	Mode Register Set Cycle Time		16		ns	9

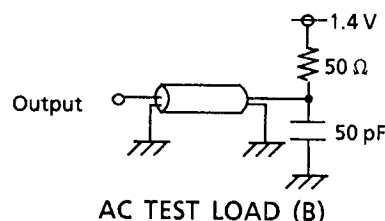
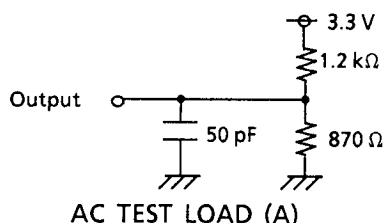
* CL is $\overline{\text{CAS}}$ latency.

NOTES

1. Conditions outside the limits listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and their values are measured at the minimum cycle rate value t_{CK} and t_{RC} . Input signals are changed once during t_{CK} .
4. These parameters depend on the output loading. The specified values are obtained with the output open.
5. The power-up sequence is described in Note 11.

6. AC TEST CONDITIONS

Reference Level of Output Signals	1.4 V / 1.4 V
Output Load	See the diagram for AC Test Load (B) below
Input Signal Levels	2.4 V / 0.4 V
Transition Time (Rise and Fall) of Input Signals	2 ns
Reference Level of Input Signals	1.4 V



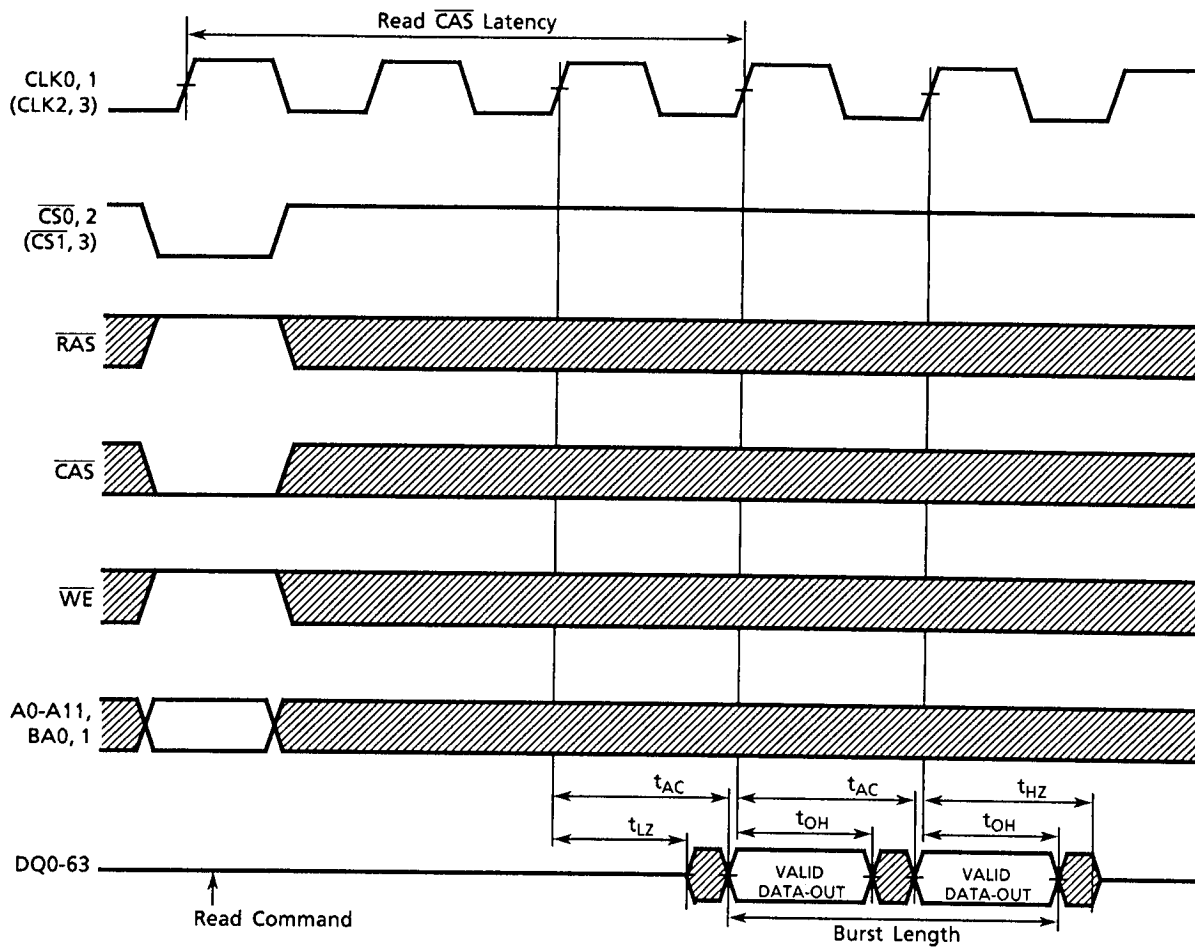
7. Transition times are measured between the V_{IH} and V_{IL} levels. The transition (rise and fall) of input signals has a fixed slope.
8. t_{HZ} defines the time at which the outputs go open circuit and are not reference levels.
9. These parameters depend on the number of clock cycles and depend on the operating frequency of the clock as follows:

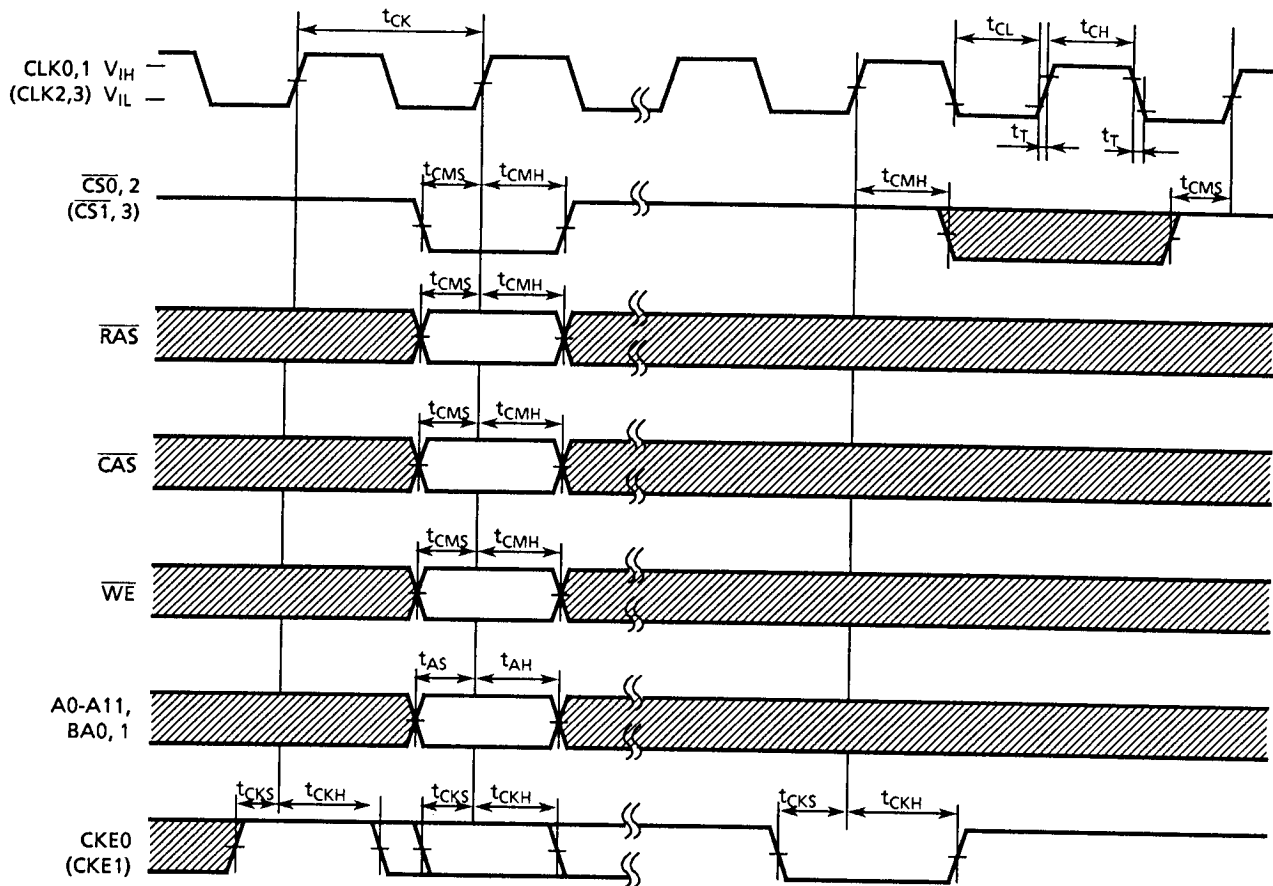
Number of clock cycles = Specified value of timing / Clock period
(Round up fractions to a whole number.)

10. t_{CH} is the pulse width of CLK measured from the positive edge to the negative edge and referenced to $V_{IH}(\min)$. t_{CL} is the pulse width of CLK measured from the negative edge to the positive edge and referenced to $V_{IL}(\max)$.
11. Power-up Sequence
Power-up must be performed in the following sequence.
 - 1) Power must be applied to V_{DD} with all input signals held in the NOP state. The CLK signal must be started at the same time as power is applied.
 - 2) After power-up a pause of at least 200 μ seconds is required. Then, DQMB and CKE must be held High (at the V_{DD} level) to ensure that the DQ and CB outputs are high-impedance.
 - 3) Both banks must be precharged.
 - 4) The Mode Register Set command must be asserted to initialize the Mode register.
 - 5) An Auto-Refresh operation must consist of at least eight Auto-Refresh cycles.The order in which 4) and 5) are performed is interchangeable.

TIMING DIAGRAMS

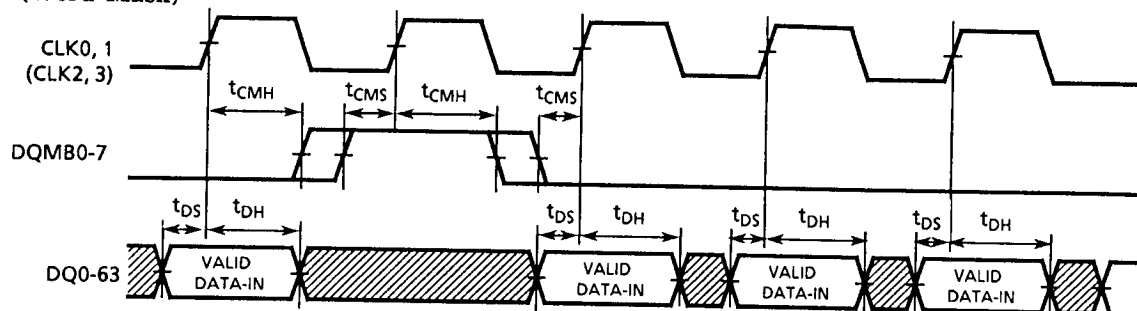
Read Timing



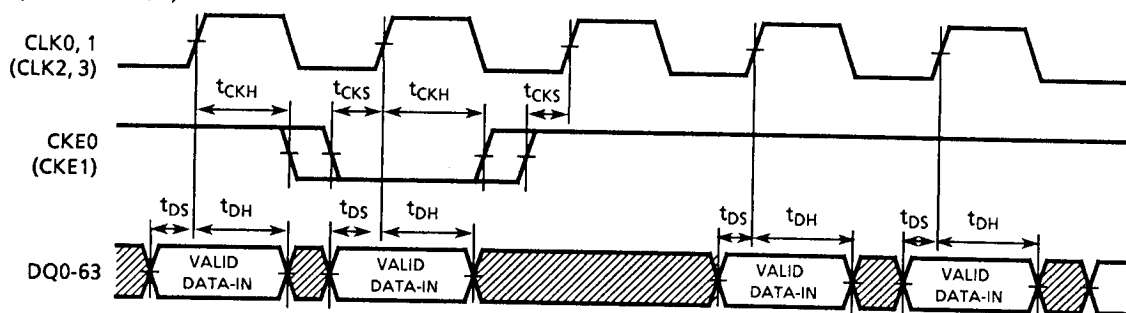
Command Input Timing

Control Timing for Input Data

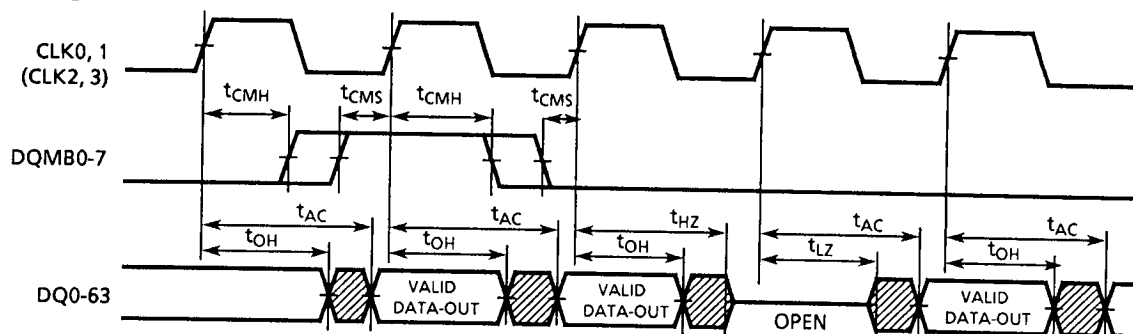
(Word Mask)



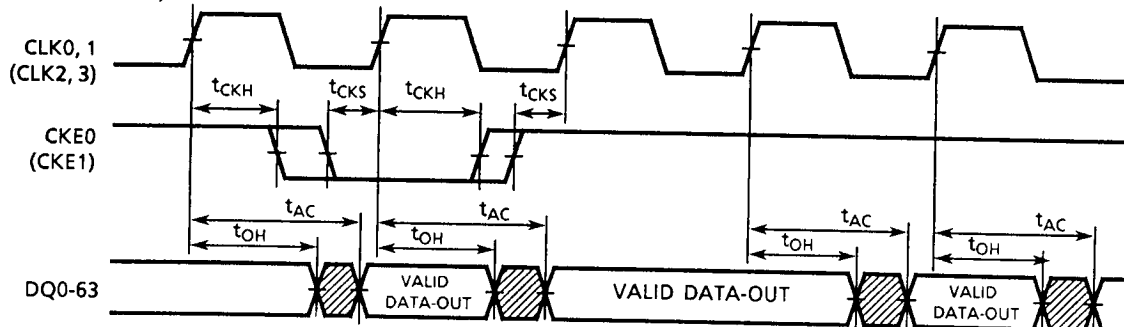
(Clock Mask)

Control Timing for Output Data

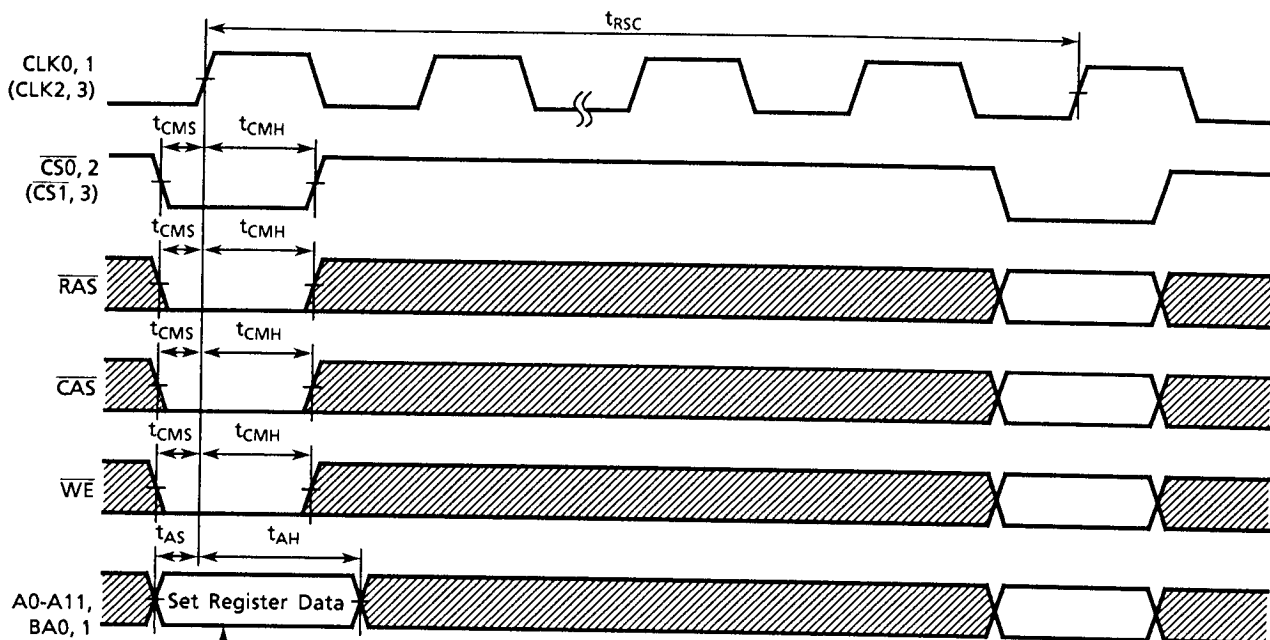
(Output Enable)



(Clock Mask)



Mode Register Set Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	0	(Test Mode)
A8	0	Reserved
A9	Write Mode	
A10	0	Reserved
A11	0	
BA0	0	
BA1	0	

			Burst Length	
A2	A1	A0	Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleave

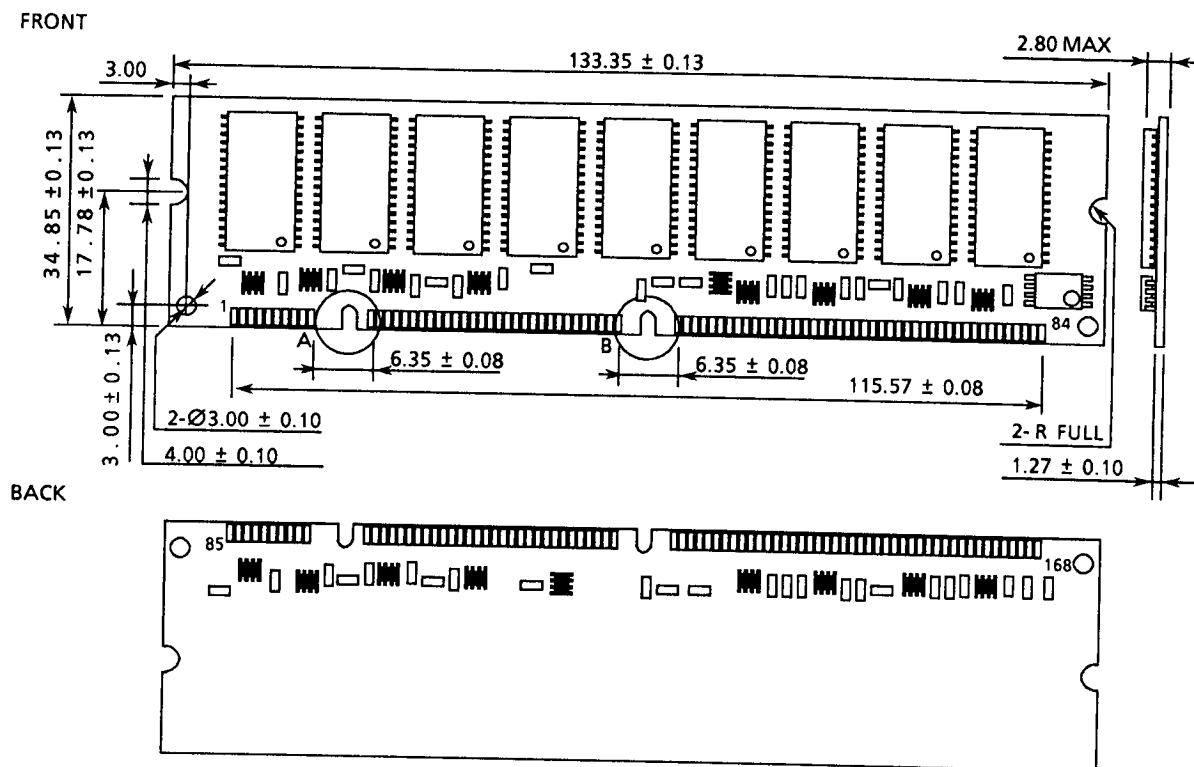
A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4

A9	Single-Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Next Command

PACKAGE DIMENSIONS (THMY7280F1BEG)

Unit: mm



CONTACT DIMENSIONS

A: Unbuffered keying

B: 3.3-V keying

