FEATURES

- ☐ Comprehensive MIL-STD-1553 dual redundant Bus Controller (BC), Remote Terminal (RT), and Monitor Terminal (MT) with integrated Bus Transceivers, Memory, and Memory Management Unit (MMU)
- ☐ Compliant MIL-STD-1553B, Notice II RT
  - Internal command illegalization in the RT mode
  - 16-bit read/write time-tag with user-defined resolution
  - Subaddress double buffering
- ☐ Simultaneous RT/MT mode of operation
- ☐ Flexible BC architecture designed to off-load the host computer
  - Minor frame timing
  - Efficient command block flow statements (Branch, Go to, Call)
  - Status word polling
  - Programmable retries
- ☐ Programmable interrupt architecture with automatic interrupt logging available in all modes
- ☐ Autonomous operation in all three modes of operation
  - External initialization bus
  - Ideal for low cost remote terminals
- ☐ Internal Memory Management Unit interfaces host/subsystem to 512Kbit SRAM
  - Wait state and zero-wait state configurations
- ☐ Built-in test capability
- ☐ Supports JTAG 1149.1
- ☐ Flexible power supply configurations
  - +5-volt only operation
  - -15-volt and 5-volt operation
  - -12-volt and 5-volt operation
- ☐ Flexible MCM-C packaging offering:
  - 139-pin pingrid array (PGA)
  - 140-lead flatpack
  - Complete interface in 1.9 in^2 of board space

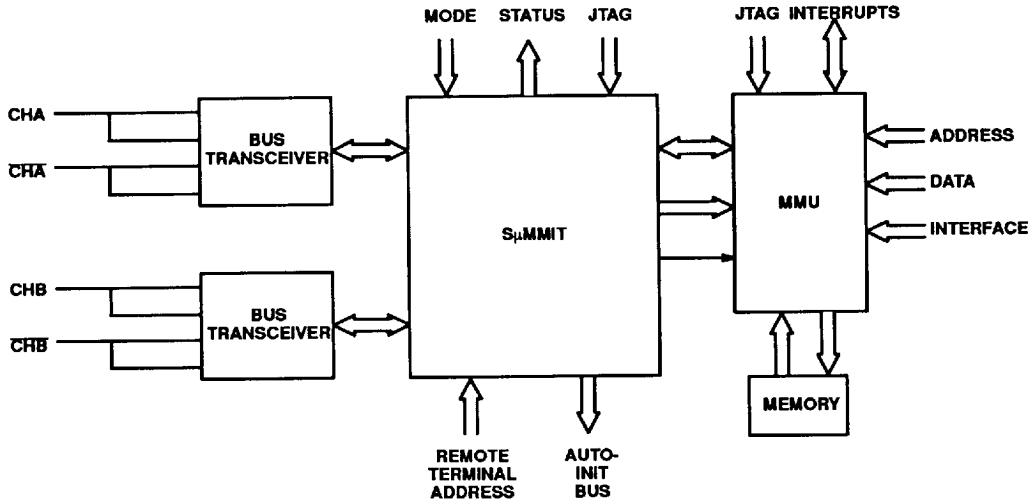


Figure 1. UT69151 SμMMIT XT Block Diagram

1.0 INTRODUCTION

The SμMMIT XT provides the system designer with an intelligent highly integrated solution to MIL-STD-1553 A/B multiplexed serial data bus design problems. The SμMMIT XT is a multi-chip module device that implements all three of the defined MIL-STD-1553 functions - Remote Terminal, Bus Controller, and Monitor. Using multi-chip module package technology the SμMMIT XT incorporates internal memory, a memory management unit, and bus transceivers.

Operating either autonomously or with a tightly coupled host, the SμMMIT XT will solve a wide range of MIL-STD-1553 interface problems. A powerful RISC processing unit provides automatic message handling, message status, and interrupt information. The register based interface architecture provides many programmable functions as well as extensive information pertinent to device maintenance. In either of the three operating modes, the SμMMIT XT can access up to 32K x 16 of internal memory.

1.1 Remote Terminal Features

The SμMMIT XT Remote Terminal (SRT) conforms to the requirements of MIL-STD-1553B, Notice II. In addition to meeting the requirements of the Standard, the SRT has an extensive list of flexible features to meet any MIL-STD-1553B interface requirement.

Indexing

The SRT can buffer up to 256 receive messages on a subaddress-by-subaddress basis. Upon reception of the specified number of messages, the SRT can generate an interrupt by signaling either the host or subsystem that data is ready for processing. The indexing feature is commonly used to implement bulk data transfer algorithms or a virtual circular buffer.

Buffer Ping-Pong

To support the transfer of periodic data, double buffering schemes are often incorporated into remote terminal designs. Periodic data transfer incorporates the use of two data buffers per subaddress. The remote terminal processes messages (receive or transmit) via the designated primary buffer. The host or subsystem uses the secondary buffer to collect new data for transmission or process data received during the defined time interval. Upon completion of a message, the remote terminal will switch the primary and secondary data buffers (i.e., ping-pong). The SRT supports ping-pong buffering via a user-selected ping-pong architecture consisting of dual subaddress data pointers.

Internal Illegalization

An internal 256-bit (16 x 16) RAM allows for the illegalization of all mode codes and subaddresses. The illegalization RAM is accessed at the beginning of message processing to determine if the valid command is prohibited. To eliminate host or subsystem overhead, the SμMMIT XT can initialize the 256-bit illegalization RAM during the auto-initialization sequence.

Broadcast

Designed to meet the requirements of MIL-STD-1553B Notice II, the SRT can store all data associated with a broadcast command in separate memory from non-broadcast commands. This feature is user-selected via the Descriptor Control word and internal Control Register.

Interrupt History

A programmable interrupt structure allows the host or subsystem the flexibility to enter 16 interrupts into a 32-word buffer before service. This feature allows the logging of multiple interrupts if immediate service is restricted. The interrupt structure enters an Interrupt Information word (IIW) and an Interrupt Address word (IAW) indicating what subaddress or command block generated the interrupt. All modes of operation support interrupt logging. For more details on the interrupt structure, refer to section 5.0.

Message Information

The SRT generates a Message Information word and time-tag (16-bit) for all transacted messages. This information is written into memory along with message data words. The Message Information word contains word count, message errors, and message type information.

1.2 Bus Controller Features

The SμMMIT XT Bus Controller (SBC) is a powerful MIL-STD-1553 bus controller developed to meet the requirements of multi-frame processing with low host overhead. User-defined decision making allows the SBC to operate autonomously from the host until a designated event or series of events has taken place.

Multiple Message Processing
The SBC architecture allows the chaining of multiple MIL-STD-1553 commands into major and minor frames depending on the application. This feature allows the host to structure message frames that perform independent tasks such as periodic data transfer, service requests, and bus diagnostics (initiate BIT). The SBC uses a simple opcode scheme to control the command block flow.

Message Scheduling
The SBC allows host entry of data to control the time between messages. This feature is useful when the BC has to perform periodic message transactions with multiple remote terminals.

Polling
The host instructs the SBC to interrogate the status word response of remote terminals to determine if any SBC action is required. The SBC can detect the assertion of status word bits and generate interrupts or branch to a new message frame. Polling is useful if the application requires control of message frame flow as a function of remote terminal response.

Automatic Retry
The SBC can automatically retry a message on busy, message error, or other status word bit response. If enabled, the SBC can retry up to four times on the primary bus or alternate bus.

1.3 Monitor Terminal Features
The SμMMIT XT Monitor Terminal (SMT) is a full-featured MIL-STD-1553B bus monitor designed to monitor all or selected remote terminals on the bus. Requiring little host intervention, the SMT will monitor selected remote terminals until a pre-defined message count is reached. Generation of an interrupt alerts the host that SMT service is required.

Message Information
Each message transaction generates a message information word. This information helps determine message validity and remote terminal health. The message information word is stored in memory along with message data words.

1.4 Remote Terminal/Monitor Terminal Features

Monitor and Remote Terminal
For those applications that require the SMT to transfer or receive information, the SμMMIT XT is configured as both a remote terminal (SRT) and monitor (SMT). This feature allows the SMT to communicate on the bus as an RT, and monitor bus activity. Configuration as both SMT and SRT precludes the SMT from monitoring its own remote terminal address.

1.5 Protocol Definition
For maximum flexibility, the SμMMIT XT has been designed to operate in many different systems which use various protocols. Specifically, two of the protocols that the SμMMIT XT may interface is MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, the SμMMIT XT may be configured through an external pin or through control register bits.

1.6 Transceivers
Internal monolithic transceivers are complete transmitter and receiver pairs for MIL-STD-1553A and 1553B applications. The receiver section of the SμMMIT XT accepts biphase-modulated Manchester II bipolar data from a MIL-STD-1553 data bus and produces TTL-level signal data at its internal RXOUT and $\overline{\text{RXOUT}}$ outputs.

The transmitter section accepts biphase TTL-level signal data at its internal TXIN and $\overline{\text{TXIN}}$ and produces MIL-STD-1553 data signals. The transmitter's output voltage is typically $10_{V_{P-P,\,LL}}$ for the UT69151-XT5 and $42_{\,V_{P-P,\,LL}}$ for the UT69151-XT15 & XT12.

2.0 Remote Terminal Architecture

The SRT is an interface device linking a MIL-STD-1553 serial data bus to a host microprocessor and/or subsystem. The SRT's MIL-STD-1553 interface includes encoding/decoding logic, error detection, command recognition, control/configuration registers, clock, and reset logic. The following sections review the architecture and use. Each section supplies information on the SRT's configuration and operation.

2.1 Register Descriptions

The following list provides the bit descriptions of the 32 internal registers that control SRT operation. All register bits are active high and reflect a logic zero condition (0000 hex) after Master Reset (except those reflecting input pins).

Register Number	Name	Register Address
0	Control Register	0000 (hex)
1	Operational Status Register	0001 (hex)
2	Current Command Register	0002 (hex)
3	Interrupt Mask Register	0003 (hex)
4	Pending Interrupt Register	0004 (hex)
5	Interrupt Log List Pointer Register	0005 (hex)
6	BIT Word Register	0006 (hex)
7	Time-Tag Register	0007 (hex)
8	SRT Descriptor Pointer Register	0008 (hex)
9	1553 Status Word Bits Register	0009 (hex)
10-15	Not Applicable	000A to 000F (hex)
16-31	Illegalization Registers	0010 to 001F (hex)

2.1.1 Control Register (Read/Write) - Register 0

This 16-bit register controls SRT configuration. To make changes to the SRT and this register, the STEX bit (Bit 15 of the Control Register) must be logic zero.

Note: The user has 5µs after $\overline{\text{TERACT}}$ active to stop execution.

Bit Number	Mnemonic	Description
15	STEX	Start Execution. Assertion of this bit initiates SµMMIT XT operation. A Control Register write negating this bit inhibits SµMMIT XT operation. A remote terminal address parity error prevents SRT operation regardless of the logical state of this bit. If an RT address parity error exists, bit 3 of Register 1 will be set low and bit 2 of Register 1 will be set high.
14	SBIT	Start BIT. Assertion of this bit places the SµMMIT XT into the Built-In Test routine. The BIT test takes 1ms to execute the SµMMIT and 70ms to execute the memory test with a fault coverage of 93.4%. If the SµMMIT XT has been started, the host must halt the device in order to place the SµMMIT XT into the Built-In Test routine (STEX = 0). Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13	SRST	Start Software Reset. Assertion of this bit immediately places the SµMMIT XT into a software reset. The software reset (which takes 5µs to execute), like $\overline{\text{MRST}}$, clears all internal logic. Note: During auto-initialization this bit should not be loaded with a logic one. SRST will only function after $\overline{\text{READY}}$ is asserted.

Bit Number	Mnemonic	Description
12	CHAEN	Channel A Enable. Setting this bit enables Channel A operation. If negated, the SRT does not recognize commands received over Channel A.
11	CHBEN	Channel B Enable. Setting this bit enables Channel B operation. If negated, the SRT does not recognize commands received over Channel B.
10	ETCE	External Timer Clock Enable. Assertion of this bit to a logic one allows the external timer clock input to supply stimulus to the internal time-tag counter. Refer to section 2.1.8. Note: The user can only change the clock frequency before starting the device (i.e., setting bit 15 of Register 0 to a logic one).
9-7	N/A	Not Applicable.
6	BUFR	Buffer Mode Enable. Assertion of this bit enables the buffer mode of operation.
5	N/A	Not Applicable.
4	BCEN	Broadcast Enable. Assertion of this bit enables the SRT broadcast option. Negation of this bit enables remote terminal address 31 as a unique remote terminal address.
3	DYNBC	Dynamic Bus Control Acceptance. This bit controls the SRT's ability to accept the dynamic bus control mode code. Assertion of this bit allows the SRT to respond to a dynamic bus control mode code with status word bit 18 set to a logic one. Negation of this bit prevents the assertion of status word bit 18 upon reception of the dynamic mode code.
2	PPEN	Ping-Pong Enable. Assertion of this bit enables the ping-pong buffer feature of the SRT and disables the message indexing feature. Negation of this bit disables the ping-pong feature and enables the message indexing feature.
1	INTEN	Interrupt Log Enable. Assertion of this bit enables the SμMMIT XT interrupt logging feature. Negation of this bit prevents the logging of interrupts.
0	XMTSW	Transmit Last Status Word. Assertion of this bit allows the SRT to automatically execute the TRANSMIT LAST STATUS WORD mode code when configured for MIL-STD-1553A mode operation. Refer to section 2.9 of this document for further definition.

2.1.2 Operational Status Register (Read/Write) - Register 1

This register reflects pertinent status information for the SRT and is not reset to 0000 (hex) on $\overline{MRST}$. Instead, the register reflects the actual stimulus applied to input pins RTA(4:0), RTAPTY, MSEL(1:0), A/$\overline{B}$ STD, and $\overline{LOCK}$. Assertion of the $\overline{LOCK}$ input prevents the modification of the remote terminal address, mode selects, and A or B Standard. In this case, a write to this register's most significant nine bits is meaningless. If $\overline{LOCK}$ is negated, a read of this register reflects the information written into this register's most significant nine bits.

Note: To make changes to the SRT and this register, the STEX bit (Bit 15 in Register 0) must be logic zero.

Bit Number	Mnemonic	Description
15	RTA4	Terminal Address Bit 4. This bit is the most significant bit of the remote terminal address. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active.
14	RTA3	Terminal Address Bit 3. This bit is Bit 3 of the remote terminal address. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active.
13	RTA2	Terminal Address Bit 2. This bit is Bit 2 of the remote terminal address. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active.
12	RTA1	Terminal Address Bit 1. This bit is Bit 1 of the remote terminal address. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active.
11	RTA0	Terminal Address Bit 0. This bit is the least significant bit of the remote terminal address. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active.
10	RTAPTY	Terminal Address Parity Bit. This bit is appended to the remote terminal address bus (RTA(4:0)) to supply odd parity. The SRT requires odd parity for proper operation. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active.
9	MSEL(1)	Mode Select 1. In conjunction with MSEL(0), this bit determines the SμMMIT XT mode of operation. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active.
8	MSEL(0)	Mode Select 0. In conjunction with MSEL(1), this bit determines the SμMMIT XT mode of operation. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active. MSEL(1) MSEL(0) Mode of Operation 0 0 SBC 0 1 SRT 1 0 SMT 1 1 SMT/SRT
7	A/$\overline{B}$ STD	Military Standard 1553A or 1553B Standard. This bit determines whether the SRT will be set to operate under MIL-STD-1553A or B. Assertion of this bit enables the XMTSW bit (Bit 0 of the Control Register). Negation of this bit automatically allows the SRT to operate under the MIL-STD-1553B protocol. This bit is latched on the rising edge of $\overline{MRST}$ and is a read only bit if the $\overline{LOCK}$ pin is active. See section 2.9 for further definition.
6	LOCK	$\overline{LOCK}$ Pin. This read-only bit reflects the inverted state of input pin $\overline{LOCK}$ and is latched on the rising edge of $\overline{MRST}$.

Bit Number	Mnemonic	Description
5	AUTOEN	$\overline{\text{AUTOEN}}$ Pin. This read-only bit reflects the inverted state of input pin $\overline{\text{AUTOEN}}$. Assertion of this input enables SRT auto-initialization.
4	SSYSF	$\overline{\text{SSYSF}}$ Pin. This read-only bit reflects the inverted state of the input pin $\overline{\text{SSYSF}}$.
3	EX	SμMMIT XT Executing. This read-only bit indicates whether the SRT is presently executing or whether it is idle. A logic one indicates that the SμMMIT XT is executing; logic zero indicates that the SμMMIT XT is idle.
2	TPARF	Terminal Parity Fail. This bit indicates the observance of a terminal address parity error. The SRT checks for odd parity. This read only bit reflects the parity of Operational Status Register bits 15-10, and is latched on the rising edge of $\overline{\text{MRST}}$.
1	READY	$\overline{\text{READY}}$ Pin. This read-only bit reflects the inverted state of the output pin $\overline{\text{READY}}$ and is cleared on reset.
0	TERACT	$\overline{\text{TERACT}}$ Pin. Assertion of this bit indicates that the SRT is presently processing a message. This read only bit reflects the inverted state of output pin $\overline{\text{TERACT}}$ and is cleared on reset.

RT

Note: Remote Terminal Address and Parity checked on start of execution.

2.1.3 Current Command Register (Read-only) - Register 2

This 16-bit register contains the last valid command processed by the SRT.

Bit Number	Mnemonic	Description
15 to 0	CC15-CC0	Current Command Bits. This register contains the last valid command received by the SRT. This register is valid 13μs after $\overline{\text{TERACT}}$ is negated. (Bit 15 MSB - Bit 0 LSB).

2.1.4 Interrupt Mask Register (Read/Write) - Register 3

The SRT interrupt architecture allows for the masking of all interrupts. An interrupt is masked if the corresponding bit of this register is set to logic zero. This feature allows the host or subsystem to temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail Interrupt
14	WRAPF	Wrap Fail Interrupt
13	TAPF	Terminal Address Parity Fail Interrupt
12	BITF	BIT Fail Interrupt
11	MERR	Message Error Interrupt
10	SUBAD	Subaddress Accessed Interrupt
9	BDRCV	Broadcast Command Received Interrupt
8	IXEQ0	Index Equal Zero Interrupt
7	ILLCMD	Illegal Command Interrupt
6-0	N/A	Not Applicable

2.1.5 Pending Interrupt Register (Read-only) - Register 4

The Pending Interrupt Register contains information that identifies events that generate interrupts. The assertion of any bit in this register asserts an output pin, $\overline{\text{MSG\_INT}}$ or $\overline{\text{YF\_INT}}$. A register read of the Pending Interrupt Register will clear all bits. Writing to the most significant 4 bits of this register generates a $\overline{\text{YF\_INT}}$.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail Interrupt. Once the SμMMIT XT issues the $\overline{\text{DMAR}}$ signal, an internal timer starts. If all DMA activity is not completed by the time the counter decrements to zero, the interrupt is generated. In the SRT mode, the $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked), current command processing ends, and the SRT will remain on-line.
14	WRAPF	Wrap Fail Interrupt. The SRT automatically compares the transmitted word (encoder word) to the reflected decoder word via the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is asserted in the BIT Word Register and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked). The loop-back path is via the MIL-STD-1553 bus transceiver.
13	TAPF	Terminal Address Parity Fail Interrupt. This bit reflects the outcome of the remote terminal address parity check. A logic one indicates a parity failure. When a parity error occurs, the SRT does not begin operation (STEX bit forced to logic zero), channel A and B do not enable, the TAPF bit is asserted here and in the BIT Word Register, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked).

Bit Number	Mnemonic	Description
12	BITF	BIT Fail Interrupt. Assertion of this bit indicates a BIT failure. Status word bit 19 is automatically set to a logic one when a BIT failure occurs. If a BIT fails, the BITF bit is asserted here and in the BIT Word Register, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked). Operation continues.
11	MERR	Message Error Interrupt. Assertion of this bit indicates that a message error condition exists. The SRT can detect Manchester errors, sync-field, word count errors (too many or too few), MIL-STD-1553 word parity errors, bit count errors (too many or too few), and protocol errors. If not masked, this bit is always set when the SRT asserts bit 9 of the status word (e.g., illegal commands, invalid data word, etc.). $\overline{\text{MSG\_INT}}$ interrupt generated.
10	SUBAD	Subaddress Accessed Interrupt. Assertion of this bit indicates a pre-selected subaddress has transacted a message. To determine the exact subaddress, the host interrogates the interrupt log IAW. $\overline{\text{MSG\_INT}}$ interrupt generated.
9	BDRCV	Broadcast Command Received Interrupt. This bit is set to a logic one to indicate the SRT's receipt of a valid broadcast command. The SRT suppresses status word transmission. $\overline{\text{MSG\_INT}}$ interrupt generated.
8	IXEQ0	Index Equal Zero Interrupt. The SRT asserts this bit to indicate the completion of a pre-defined number of commands by the SRT. Upon assertion of this interrupt, the host or subsystem updates the subaddress descriptor to prevent the potential loss of data. $\overline{\text{MSG\_INT}}$ interrupt generated.
7	ILCMD	Illegal Command Interrupt. This bit is set to a logic one to indicate the reception of an illegal command by the SRT. Upon receipt of this command, the SRT responds with a status word only; Bit 9 of the status word is set to a logic one. $\overline{\text{MSG\_INT}}$ interrupt generated.
6-0	N/A	Not Applicable.

Note: In the 8-bit mode of operation a single read to the Register 4 clears the entire register.

2.1.6 Interrupt Log List Pointer Register (Read/Write) - Register 5

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32 word ring-buffer that contains information pertinent to the service of interrupts. The SμMMIT XT architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant/upper 11 bits of this register designate the location of the Interrupt Log List within a 32K memory space. The lower 5 bits of this register should be initialized to a logic zero. The SμMMIT XT controls the lower 5 bits to implement the ring-buffer architecture. The host or subsystem reads this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Note: Bits 15-5 indicate the starting Base address while bits 4-0 indicate the ring location of the Interrupt Log List. See sections 5.0-5.3 for a description of the Interrupt Architecture.

Bit Number	Mnemonic	Description
15-0	INTA(15:0)	Interrupt Log List Pointer Bits. (Bit 15 MSB - Bit 0 LSB).

2.1.7 BIT Word Register (Read/Write) - Register 6

This register contains information on the SRT's current health. The SRT transmits the contents of this register upon reception of a Transmit Bit Word Mode Code. The lower 8 bits of this register are user-defined.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail. This bit is set if all DMA activity is not completed and the timer decrements to zero (i.e., 7μs).
14	WRAPF	Wrap Fail. The SRT automatically compares the transmitted word (encoder word) to the reflected decoder word via the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit asserts and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked). The loop-back path is via the MIL-STD-1553 bus transceiver.
13	TAPF	Terminal Address Parity Fail. This bit reflects the outcome of the remote terminal address parity check. A logic one indicates a parity failure. When a parity error occurs the SRT does not begin operation (STEX bit forced to a logic zero), channel A and B do not enable, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked).
12	BITF	BIT Fail. Assertion of this bit indicates a BIT failure. Bits 11 and 10 should be interrogated to determine the specific channel that failed. Status word bit 19 is automatically set to a logic one when a BIT failure occurs. If a BIT fails, the BITF bit is asserted, and a $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked).
11	CHAF	Channel A Fail. Assertion of this bit indicates a BIT test failure in Channel A.
10	CHBF	Channel B Fail. Assertion of this bit indicates a BIT test failure in Channel B.
9	MSBF	Memory Test Fail. Most significant memory byte failure.
8	LSBF	Memory Test Fail. Least significant memory byte failure.
7-0	UDB(7:0)	User-Defined Bits.

2.1.8 Time-Tag Register (Read/Write) - Register 7

The Time-Tag Register reflects the state of a 16-bit free running counter. The resolution of this counter is user-defined via input TCLK or fixed at 64µs/bit. The Time-Tag counter is automatically reset when the SRT receives a valid synchronize without data mode code. The SRT automatically loads the Time-Tag counter with the data associated with reception of a valid synchronize with data mode code. The Time-Tag counter begins operation on the rising edge of $\overline{\text{MRST}}$ or within 64µs; after the receipt of a valid mode code, reset remote terminal, or sync with/without data. When the SRT is halted (STEX = 0), the Time-Tag continues to run.

Bit Number	Mnemonic	Description
15-0	TT(15:0)	Time-Tag Counter Bits. (Bit 15 MSB - Bit 0 LSB)

2.1.9 Remote Terminal Descriptor Pointer Register (Read/Write) - Register 8

The SRT accesses a block of external memory to gain information on how to process a valid command. Each subaddress and mode code has a block of memory reserved for this task. Located contiguously in memory, these reserved memory locations are called a descriptor space. The Remote Terminal Descriptor Pointer Register contains an address that points to the top of this memory space. The SRT uses the T/$\overline{\text{R}}$ bit, subaddress/mode code field, and mode code to select one block within the descriptor table for message processing. The Remote Terminal Descriptor Pointer Register is static during message processing.

Bit Number	Mnemonic	Description
15-0	RTDA(15:0)	Remote Terminal Descriptor Address Bits. (Bit 15 MSB - Bit 0 LSB)

2.1.10 1553 Status Word Bits Register (Read/Write) - Register 9

The host or subsystem accesses this register to control the outgoing MIL-STD-1553 status word. The host or subsystem controls the Instrumentation, Busy, Terminal Flag, Service Request, and Subsystem Flag by writing to bits 9 through 0 of this register. The SRT's status word response reflects assertion of these bit(s) until negated by the host or subsystem unless the Immediate Clear Function is enabled. The Immediate Clear Function automatically clears these bits after being transmitted in a status word.

The Immediate Clear Function does not affect the operation of the Transmit Last Status word and Transmit Last Command word Mode Codes. Transaction of a legal valid command with the INS bit set to a logic one and the Immediate Clear Function enabled, results in the transmission of a status word with Bit 10 asserted. If the ensuing command is a Transmit Last Status word or Last Command mode code, Bit 10 of the outgoing status word remains a logic one. For MIL-STD-1553B applications, the register is as follows:

Bit Number	Mnemonic	Description
15	IMCLR	Immediate Clear Function. Assertion of this bit enables the Immediate Clear Function (IMF) of the SRT. Enabling the IMF results in the clearing of the INS, BUSY, TF, SRQ, and/or SUBF bit immediately after a message is completed. This function is enabled by asserting this bit when asserting bit(s) INS, BUSY, TF, SRQ, and/or SSYSF.
14-10	N/A	Not Applicable.
9	INS	Instrumentation Bit. This bit asserts the Instrumentation bit of the MIL-STD-1553B status word. (Bit 10 of the Status Word).
8	SRQ	Service Request Bit. This bit asserts the Service Request bit of the MIL-STD-1553B status word. (Bit 11 of the Status Word).
7-4	N/A	Not Applicable.
3	BUSY	Busy Bit. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. Assertion of this bit prevents memory accesses. (Bit 16 of the Status Word).
2	SSYSF	Subsystem Flag Bit. This bit asserts the Subsystem Flag bit of the MIL-STD-1553B status word and may also be set with the SSYSF input pin. (Bit 17 of the Status Word).
1	N/A	Not Applicable.
0	TF	Terminal Flag. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. The SRT automatically asserts this bit if a BIT failure occurs. Inhibit Terminal Flag mode code prevents the assertion by the host or subsystem. Override Inhibit Terminal Flag Mode Code re-establishes the Terminal Flag option. (Bit 19 of the Status Word).

For MIL-STD-1553A applications, the register is as follows:

Bit Number	Mnemonic	Description
15	IMCLR	Immediate Clear Function. Assertion of this bit enables the Immediate Clear Function (IMF) of the SRT. Enabling the IMF results in the clearing of the bit times 10-19 immediately after a status word is transmitted. This function is enabled by asserting this bit when asserting bit times 10-19. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
14-10	N/A	Not Applicable.
9	SB10	Status bit time 10.
8	SB11	Status bit time 11.
7	SB12	Status bit time 12.
6	SB13	Status bit time 13.
5	SB14	Status bit time 14.
4	SB15	Status bit time 15.
3	SB16	Status bit time 16.
2	SB17	Status bit time 17.
1	SB18	Status bit time 18.
0	SB19	Status bit time 19.

2.1.11 Illegalization Registers

The 16 registers are divided into 8 blocks, 2 registers per block (see table 1).

Table 1. Illegalization Register Blocks

Block Name	Address (hex)
Receive	0010 and 0011
Transmit	0012 and 0013
Broadcast Receive	0014 and 0015
Broadcast Transmit (Automatically Illegalized)	0016 and 0017
Mode Code Receive	0018 and 0019
Mode Code Transmit	001A and 001B
Broadcast Mode Code Receive	001C and 001D
Broadcast Mode Code Transmit	001E and 001F

The blocks correspond to the following types of commands. Register address 0010 (hex) and 0011 (hex) illegalize receive commands to 32 subaddresses. The most significant bit of register 0010 (hex) controls the illegalization of subaddress 01111. The least significant bit controls subaddress 00000. Register 0011 (hex) controls illegalization of subaddresses 10000 through 11111. The least significant bit relates to subaddress 10000; the most significant bit relates to subaddress 11111. Transmit commands and broadcast commands (both receive and transmit) use the same encoding scheme as receive subaddress illegalization.

Registers 18 (hex) through 1F (hex) control the illegalization of mode codes. Register 18 governs the illegalization of receive mode codes ($T/\overline{R}$ bit = 0) 00000 through 01111 and register 19 mode codes 10000 through 11111. Register blocks Transmit Mode Code ($T/\overline{R}$ bit = 1), Broadcast Receive Mode Codes, and Broadcast Transmit Mode Codes use the same decode scheme as receive mode codes.

Table 2 shows the illegalization register map. For each block, the numbers shown in the column under each bit number identifies the specific subaddress or mode code (in hex) that the register bit illegalizes. (Logical 0 = legal, Logical 1 = illegal)

Table 2. Illegalization Register Map

Name	Register Number																
Bit Number		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Receive	16	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	17	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Transmit	18	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	19	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Brd Receive	20	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	21	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Brd Transmit	22	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
	23	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
Mode Receive	24	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	25	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Transmit	26	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	27	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Brd Receive	28	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	UU	01	WW
	29	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Brd Transmit	30	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	ZZ	01	XX
	31	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY

Notes:
1. Brd = Broadcast
2. Mode = Mode code
3. XX= Automatically illegalized by SRT.
4. YY= Automatically illegalized by SRT in 1553B only.
5. ZZ= Automatically illegalized by SRT in 1553B and 1553A if XMTSW is enabled.
6. WW = Automatically illegalized in 1553A.
7. UU = Automatically illegalized in 1553A if XMTSW enabled.

RT

2.2 Descriptor Block

To process messages, the SRT uses data supplied in the internal registers with data stored in memory. The SRT accesses a four word descriptor block stored in memory. The descriptor block is accessed at the beginning and end of command processing. Multiple descriptor blocks are sequentially entered into memory to form a descriptor table. The following paragraphs discuss the descriptor block in detail.

The host or subsystem controlling the SRT allocates 512 consecutive memory spaces for the subaddress and mode code descriptor table (see figure 2). The top of the descriptor table can reside at any address location. Defined and entered into memory by the host, the SRT is linked to the descriptor table via the Descriptor Address Register contents. Each descriptor block contains a Control Word, Data Pointer A, Data Pointer B, and Broadcast Data Pointer. Each subaddress and mode code is assigned a descriptor for receive and transmit commands (T/$\overline{R}$ bit equal zero or one).

Control word information allows the SRT to generate interrupts, buffer messages, and control message processing. For a receive command, the Data List Pointer is read to determine the top of the data buffer. The SRT stores data sequentially from the top of data buffer plus two locations (e.g., 0100, 0101, 0102, 0103, etc.). When processing a transmit command, the Data List Pointer is read to determine where data words are retrieved. The SRT retrieves data words sequentially from the address the Data List Pointer designates plus two address locations.

The Broadcast Data Pointer allows for separate storage of non-broadcast data from broadcast data per MIL-STD-1553B Notice II. The host or subsystem enables or disables this feature via the Control Word's least significant bit. When disabled, the non-broadcast and broadcast data is stored via Data List Pointer A or B. For transmit commands, the Broadcast Data Pointer is not used. The SRT does not transmit any information on the receipt of a broadcast transmit command.

The SRT reads the descriptor block during command processing (i.e., after assertion of $\overline{\text{TERACT}}$). The SRT arbitrates for the memory bus. After receiving control of the bus, the SRT reads the control word and three Data Pointers. The SRT then begins the acquisition of data words for either transmission or storage.

After transmission or reception, the SRT begins post-processing. Command post-processing begins with arbitration for the memory bus. An optional interrupt log entry is performed after a descriptor update. During the descriptor update, the SRT modifies the Control Word index field and bits 4, 2 , and 1, if required. The SRT updates Data Pointer A if no message errors occurred during the message transaction. Reception of a broadcast command, with no message errors, results in the update of the Broadcast Data Pointer. Neither Data Pointer A, B or Broadcast is updated if the SRT has the ping-pong mode of operation enabled.

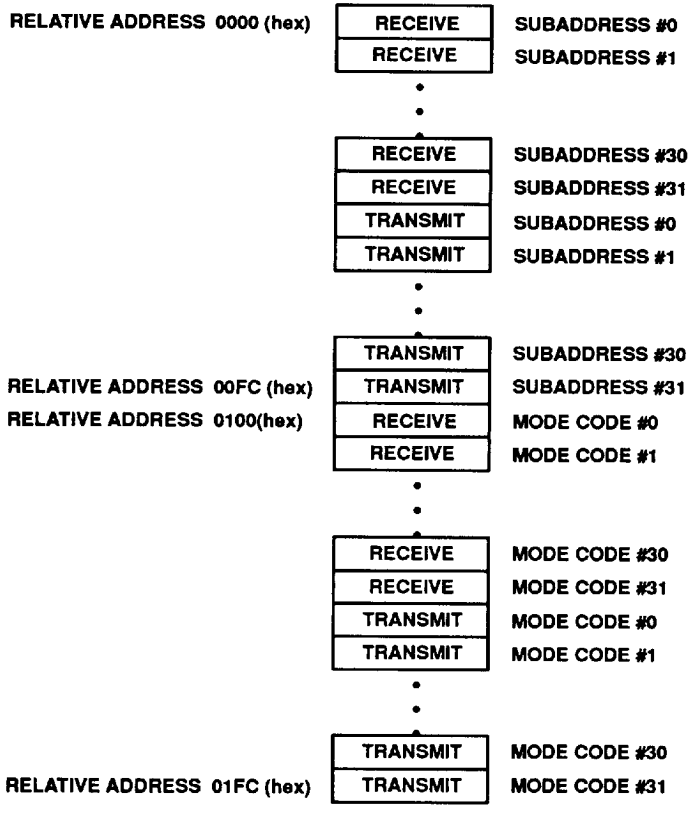


Figure 2. Descriptor Table

2.2.1 Receive Control Word

The following bits describe the receive subaddress descriptor Control word. Information contained in this word assists the SRT in message processing. The descriptor control word is initialized by the host or subsystem and updated by the SRT during command post-processing.

Bit Number	Mnemonic	Description
15-8	INDX	Index Field. These bits define multiple message buffer length. The host or subsystem uses this field to instruct the SRT to buffer "N" messages. "N" can range from 0 (00 hex) to 256 (FF hex). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). During ping-pong mode operation, initialize the index field to 00 (hex). The SRT does not perform multiple message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the subaddress is illegalized. The SRT can generate an interrupt when the index field transitions from one to zero (see bit 7).
7	INTX	Interrupt Index Equals Zero. Assertion of this bit enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid broadcast command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero; the SRT overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	N/A	Not Applicable.
2	A/$\overline{\text{B}}$	Buffer A/$\overline{\text{B}}$. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a valid broadcast command.
0	NII	Notice II. Assertion of this bit enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. When negated, broadcast information is stored in the same buffer as non-broadcast information.

2.2.2 Transmit Control Word

The following bits describe the transmit subaddress descriptor Control word. Information contained in this word assists the SRT in message processing. The descriptor control word is initialized by the host or subsystem and updated by the SRT during command post-processing.

Bit Number	Mnemonic	Description
15-7	N/A	Not Applicable.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{\text{MSG\_INT}}$ asserts after message processing.
5	N/A	Not Applicable.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero, the SRT overwrites the zero with a logic one upon completion of message processing. After interrogation, the host should reset this bit to zero to observe further accesses.
3	N/A	Not Applicable.
2	A/$\overline{\text{B}}$	Buffer A/$\overline{\text{B}}$. Indicates the data pointer to access when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a broadcast command.
0	N/A	Not Applicable.

2.2.3 Mode Code Receive Control Word

The following bits describe the receive mode code descriptor Control word. Information contained in this word assists the SRT in message processing. The descriptor control word is initialized by the host or subsystem and updated by the SRT during command post-processing.

Note: In MIL-STD-1553A, all mode codes are without data, and the T/$\overline{R}$ bit is ignored. See section 2.9 for the MIL-STD-1553A operation.

Bit #	Mnemonic	Description
15-8	INDX	Index Field. These bits define message buffer length. The host or subsystem uses this field to instruct the SRT to buffer "N" messages. "N" can range from 0 (00 hex) to 256 (FF hex). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). The SRT does not perform message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the mode code is illegalized. The SRT can generate an interrupt when the index field transitions from one to zero (see bit 7).
7	INTX	Interrupt Index Equals Zero. Assertion of this bit enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when a valid broadcast mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero; the SRT overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	N/A	Not Applicable.
2	A/$\overline{B}$	Buffer A/$\overline{B}$. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A, logic zero a indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a valid broadcast command.
0	NII	Notice II. Asserting this bit enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. When negated, broadcast information is stored in the same buffer as non-broadcast information.

2.2.4 Mode Code Transmit Control Word

The following bits describe the transmit mode code descriptor Control word. Information contained in this word assists the SRT in message processing. The descriptor control word is initialized by the host or subsystem and updated by the SRT during command post-processing.

Note: In MIL-STD-1553A, all mode codes are without data, and the T/$\overline{R}$ bit is ignored. See section 2.9 for the MIL-STD-1553A operation.

Bit Number	Mnemonic	Description
15-7	N/A	Not Applicable.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when a broadcast mode code is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. Output pin $\overline{MSG\_INT}$ asserts after message processing.
4	BAC	Block Accessed. The subsystem or host initializes this bit to zero; the SRT overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	N/A	Not Applicable.
2	A/$\overline{B}$	Buffer A/$\overline{B}$. This bit indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a broadcast command.
0	N/A	Not Applicable.

2.2.5 Data Pointer A and B

Data List Pointer A and B contain address information for the retrieval and storage of message data words. In the index mode of operation, the SRT reads Data Pointer A to determine the location of data for retrieval or storage. The SRT uses the Data Pointer to initialize an internal counter, the counter increments after each data word. For a receive command, the SRT stores the incoming data word sequentially into memory. As part of command post-processing, the SRT writes a new data pointer into the descriptor block. The SRT continues to update the data pointer until the Control Word index field decrements to zero. An example is shown in figure 3.

Note: The index feature is not applicable for transmit commands (i.e., T/$\overline{R}$ bit = 1).

For ping-pong buffer operation, the host uses either Data Pointer A or Data Pointer B. The SRT determines which pointer to access via the state of Control Word bit 2. The SRT retrieves or stores data words from the address contained in the data pointer, automatically incrementing the data pointer as data words are received. The data pointer is never updated as part of command post-processing in the ping-pong mode of operation. See figures 4 and 5.

Bit Number	Mnemonic	Description
15-0	DP(15:0)	Data Pointer Bits. The second and third words of the descriptor block contain the data buffer location. The SRT accesses either Data Pointer A or Data Pointer B depending on the state of Control Word Bit 2 during ping-pong operation. For index operation, the SRT accesses only Data Pointer A. The SRT updates data pointer A after message processing is complete and the index field is not equal to zero and pingpong operation disabled. Bit 15 is the most significant bit; bit 0 is the least significant bit.

2.2.6 Broadcast Data Pointer

The following bits describe the receive subaddress/mode code descriptor Broadcast Data Pointer. This word contains the address for the Message Information word, Time-Tag word, and data words associated with a broadcast command. The SRT automatically increments this data pointer during command post-processing, if ping-pong operation disabled.

Bit Number	Mnemonic	Description
15-0	BP(15:0)	Broadcast Data Pointer. The fourth word of the descriptor block contains the broadcast data buffer location. This pointer can reside anywhere inside of a 32K data space. The SRT accesses this pointer when Control Word bit 0 is a logic one and broadcast is enabled. Bit 15 is the most significant bit, bit 0 is the least significant bit. Note: If ping-pong is enabled, this pointer does not update. Note: When the broadcast command is followed by a Transmit Last Command or Last Status Word mode code, the SRT transmits a status word with bit 15 of the status word set to a logic one. The broadcast bit is cleared by reception of the next valid non-broadcast command.

2.3 Data Structures

The following sections discuss the data structures that result from command processing. For each complete message processed, the SRT generates a Message Information word and Time-Tag word. These words aid the host or subsystem in further message processing. The Message Information word contains word count, message type, and message error information. The Time-Tag word is a 16-bit word containing the command validity time. The Time-Tag word data comes from the SRT's internal Time-Tag counter.

Receive Subaddress #1 Descriptor Block	CONTROL WORD	Index field contents: 03XX (hex)	
	DATA POINTER A	Data Pointer A: 0100 (hex)	
	DATA POINTER B	Data Pointer B: XXXX (hex)	
	BROADCAST DATA POINTER	Broadcast Data Pointer: XXXX (hex)	
Command #1 Receive three words	MESSAGE INFO WORD	0100 (hex)	Index equals three
	TIME-TAG	0101 (hex)	
	DATA WORD #1	0102 (hex)	
	DATA WORD #2	0103 (hex)	
	DATA WORD #3	0104 (hex)	Index decrements to two
Command #2 Receive two words	MESSAGE INFO WORD	0105 (hex)	Index equals two
	TIME-TAG	0106 (hex)	
	DATA WORD #1	0107 (hex)	
	DATA WORD #2	0108 (hex)	Index decrements to one
Command #3 Receive three words	MESSAGE INFO WORD	0109 (hex)	Index equals one
	TIME-TAG	010A (hex)	
	DATA WORD #1	010B (hex)	
	DATA WORD #2	010C (hex)	
	DATA WORD #3	010D (hex)	Index decrements to zero (Data Pointer A updated to 010E (hex), interrupt generated if enabled)

Note:
x = "don't care"

Figure 3. Non-Broadcast Receive Message Indexing

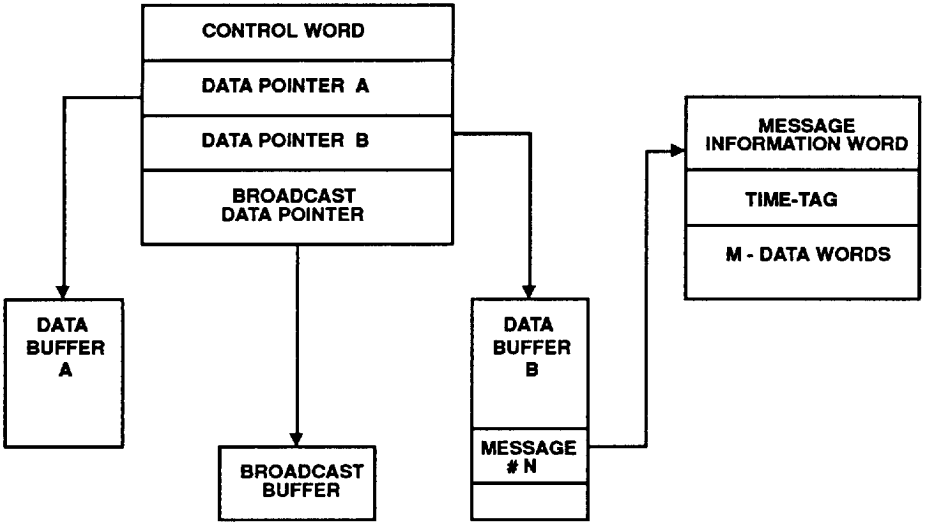


Figure 4. SRT Descriptor Block (Receive)

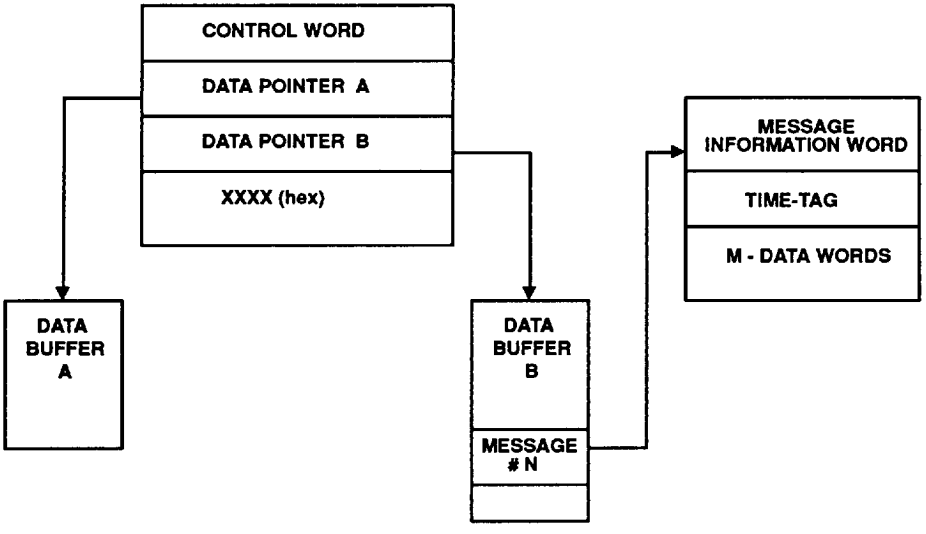


Figure 5. SRT Descriptor Block (Transmit)

2.3.1 Subaddress Receive Data

For receive commands, the SRT stores data words plus two additional words. The SRT adds a Receive Information word and Time-Tag word to each receive command data packet. The SRT places the Receive Information word and Time-Tag word ahead of the data words associated with a receive command (see figures 3, 4, and 5). When message errors occur, the SRT enters the Receive Information word, and Time-Tag word. Once a message error condition is observed, all data words are considered invalid.

Data storage occurs at the memory location pointed to by the data pointer plus two locations.

2.3.1.1 Receive Information (Info) Word

The following bits describe the Receive Information Word contents.

Bit Number	Mnemonic	Description
15-11	WC(4:0)	Word Count Bits. These five bits contain word count information extracted from the receive command word bits 15 to 19.
10	N/A	Not Applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on channel A. Conversely, if this bit is set to logic zero, the message was received on channel B.
8	RTRT	Remote Terminal to Remote Terminal Transfer. The command processed was an RT-to-RT transfer.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	N/A	Not Applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	TO	Time-Out Error. Assertion of this bit indicates the SRT did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
2	OVR	Overrun Error. Assertion of this bit indicates the SRT received a word when none was expected or the number of data words received was greater than expected.
1	PRTY	Parity Error. Assertion of this bit indicates the SRT observed a parity error in the incoming data words.
0	MAN	Manchester Error. Assertion of this bit indicates the SRT observed a Manchester error in the incoming data words.

2.3.2 Subaddress Transmit Data

The host or subsystem is responsible for organization of the data packet (i.e., M data words) into memory and establishing the applicable data pointer. The host or subsystem allocates two memory locations at the top of the data packet for the storage of the Transmit Information word and Time-Tag word. An example transmit data structure for three words is shown below.

```
Data Pointer A -----> 0100 (hex)  XXXX  ;reserved for Transmit Info word
equals 0100 (hex)     0101 (hex)  XXXX  ;reserved for Time-Tag word
                      0102 (hex)  FFFF  ;data word
                      0103 (hex)  FFFF  ;data word
                      0104 (hex)  FFFF  ;data word
```

Note: Data Pointer A points to the top of the data structure not to the top of the data words.

2.3.2.1 Transmit Information (Info) Word

The following bits describe the Transmit Information word contents.

Bit Number	Mnemonic	Description
15-11	WC(4:0)	Word Count Bits. These five bits contain word count information extracted from the receive command word bits 15 to 19.
10	N/A	Not Applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on the A bus. Conversely, if this bit is set to logic zero, the message was received on the B bus.
8	N/A	Not Applicable.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for more detail.
6-5	N/A	Not Applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	N/A	Not Applicable.
2	OVR	Overrun Error. Assertion of this bit indicates the SRT received a data word with a Transmit Command.
1-0	N/A	Not Applicable.

2.3.3 Mode Code Data

The transmit and receive data structures for mode codes are similar to those for subaddress. The receive data structure contains an Information word, Time-Tag word, and message data word. All receive mode codes with data have one associated data word. Data storage occurs at the memory location pointed to by the data pointer plus two locations. Reception of the synchronize with data mode code automatically loads the Time-Tag counter and stores the data word at the address defined by the data pointer plus two locations.

The transmit mode code data structure contains an Information word, Time-Tag word, and associated data word. The subsystem or host is responsible for linking the SRT Data Pointer to the data (e.g., Transmit Vector word). For mode codes with internally generated data words (e.g., Transmit BIT word, Transmit Last Command), the transmitted data word is added to the data structure.

For MIL-STD-1553A mode of operation, all mode codes are defined without data words. For mode codes without data, the data structure contains the Message Information word and Time-Tag word only.

Note: In MIL-STD-1553A, all mode codes are without data and the T/$\overline{R}$ bit is ignored. See section 2.9 for the MIL-STD-1553A operation.

2.3.3.1 Mode Code Receive Information (Info) Word

The following bits describe the Mode Code Receive Information word contents.

Bit Number	Mnemonic	Description
15-11	MC (4:0)	Mode Code. These five bits contain the mode code information extracted from the receive command word bits 15 to 19.
10	N/A	Not Applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on the A bus. Conversely, if this bit is set to logic zero, the message was received on the B bus.
8	RTRT	Remote Terminal to Remote Terminal Transfer. Assertion of this bit indicates the command processed was an RT-to-RT transfer.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	N/A	Not Applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	TO	Time-out Error. Assertion of this bit indicates the SRT did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
2	OVR	Overrun Error. Assertion of this bit indicates the SRT received a word when none was expected, or the number of data words received was greater than expected.
1	PRTY	Parity Error. Assertion of this bit indicates the SRT observed a parity error in the incoming data words.
0	MAN	Manchester Error. Assertion of this bit indicates the SRT observed a Manchester error in the incoming data words.

2.3.3.2 Mode Code Transmit Information (Info) Word

The following bits describe the Mode Code Transmit Information word contents.

Bit Number	Mnemonic	Description
15-11	MC (4:0)	Mode Code. These five bits contain the mode code information extracted from the command word bits 15 to 19.
10	N/A	Not Applicable.
9	CHA/$\overline{B}$	Channel A/$\overline{B}$. Assertion of this bit indicates that the message was received on the A bus. Conversely, if this bit is set to logic zero, the message was received on the B bus.
8	N/A	Not Applicable.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	N/A	Not Applicable.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	N/A	Not Applicable.
2	OVR	Overrun Error. Assertion of this bit indicates the SRT received a data word with a Transmit Command.
1-0	N/A	Not Applicable.

2.4 Mode Code and Subaddress

The SμMMIT XT provides subaddress and mode code decoding that meets MIL-STD-1553B requirements. In addition, the device has internal illegal command decoding for reserved MIL-STD-1553B mode codes. Table 3 shows the SRT's response to all possible mode code combinations.

Table 3. Mode Code Descriptions

T/R	Mode Code	Function	Operation
0	00000-01111	Undefined (w/o data)	1. Command word stored 2. Status word transmitted
0	10000	Undefined (with data)	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10001	Synchronize (with data)	1. Command word stored 2. Data word stored 3. Time-Tag counter loaded with data word value 4. Status word transmitted
0	10010	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10011	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10100	Selected Transmitter Shutdown	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10101	Override Selected Transmitter Shutdown	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10110-11111	Reserved	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control	1. Command word stored 2. Dynamic Bus Acceptance bit set in outgoing status word if enabled in the Control Register 3. Status word transmitted
1	00001	Synchronize	1. Command word stored 2. Time-Tag counter reset to 0000 (hex) 3. Status word transmitted
1	00010	Transmit Status Word	1. Command word stored 2. Last status word transmitted 3. Status word cleared after master reset Note: SRT updates status word if illegalized.
1	00011	Initiate Self-Test	1. Command word stored 2. Status word transmitted 3. BIT initiated 4. TF bit set if BITF bit asserted
1	00100	Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus disabled

Table 3. Mode Code Descriptions (Cont.)

T/R	Mode Code	Function	Operation
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus enabled Note: Reception of the override transmitter shutdown mode code does not enable a channel not previously enabled in the Control Register. Reset remote terminal mode code clears the transmitter shutdown function.
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal flag bit set to zero and assertion disabled 3. Status word transmitted
1	00111	Override Inhibit Terminal Flag	1. Command word stored 2. Terminal Flag bit enabled for assertion 3. Status word transmitted
1	01000	Reset Remote Terminal	1. Command word stored 2. Status word transmitted 3. SRT reset, see section 2.8 for more information on software reset
1	01001-01111	Reserved	1. Command word stored 2. Status word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Service request bit set to a logic zero in out going status. 3. Status word transmitted 4. Data word transmitted 5. Clears the SRQ bit in the 1553 status word bits register (Register 9)
1	10001	Reserved	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10010	Transmit Last Command	1. Command word not stored 2. Last status word transmitted 3. Last command word transmitted 4. Data word stored (Transmit Last Command) 5. Transmitted data word is all zero after reset Note: The SRT stores the Transmit Last Command mode code if illegalized and updates status word.
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. BIT word transmitted from BIT Word Register 4. Data word stored (Transmit BIT Word)
1	10100-10101	Undefined (with data)	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10110-11111	Reserved	1. Command word stored 2. Status word transmitted 3. Data word transmitted

2.5 Encoder and Decoder

The SRT interfaces directly to a transmitter/receiver via the SRT Manchester II encoder/decoder. The SRT receives the command word from the MIL-STD-1553 bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the SRT processes each incoming data word for correct format, word count, and contiguous data. If a message error is detected, the SRT stops processing the remainder of the message, suppresses status word transmission, and asserts bit 9 (ME bit) of the status word. The SRT will track the message until proper word count is finished.

The SRT automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is asserted in the BIT Word Register and the $\overline{\text{YF\_INT}}$ will be generated, if enabled. In addition to the loop-back compare test, a timer precludes a transmission greater than 800µs by the assertion of Fail-Safe Timer. This timer is reset upon receipt of another command. Remote Terminal Response Time:

MIL-STD-1553A = 7µs
MIL-STD-1553B = 10µs
Data Contiguity Time-Out = 1.0µs

2.6 RT-RT Transfer Compare

The RT-to-RT Terminal Address compare logic ensures that the incoming status word's Terminal Address matches the Terminal Address of the transmitting RT specified in the command word. An incorrect match results in setting the message-error bit and suppressing transmission of the status word. (RT-to-RT transfer time-out = 55 to 59µs). The receiving SRT does not check ME or SSYSF of the transmitting remote terminal.

2.7 Terminal Address

The SRT Terminal Address is programmed via six input pins: RTA(4:0) and RTPTY. Negating $\overline{\text{MRST}}$ latches the SRT's Terminal Address from pins RTA(4:0) and parity bit RTPTY. The address and parity cannot change until the next assertion and negation of the $\overline{\text{MRST}}$ input (for $\overline{\text{LOCK}}$ = 0). The Terminal Address parity is odd; input pin RTPTY is set to a logic state to satisfy this requirement. Assertion of Operational Status Register bit 2 (TAPF) indicates incorrect Terminal Address parity. The Operational Status Register bit 2 is valid after the rising edge of $\overline{\text{MRST}}$.

For example:

RTA(4:0) = 05 (hex) = 00101
RTPTY = 1 (hex) = 1 Sum of 1s = 3 (odd), Operational Status Register Bit 2 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 0 (hex) = 0 Sum of 1s = 1 (odd), Operational Status Register Bit 2 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 1 (hex) = 0 Sum of 1s = 2 (even), Operational Status Register Bit 2 = 1

Note:

- The SRT checks the Terminal Address and parity after the SRT has been started. With Broadcast disabled, RTA(4:0) = 11111 operates as a normal RT address.
- The BIT Word Register parity fail bit is valid after the SRT has been started.
- The Terminal Address is also programmed via a write to the Operational Status Register ($\overline{\text{LOCK}}$ = 1). The SRT loads the Terminal Address on the completion of the Control Register write which starts the SRT.
- YF_INT occurs if enabled.

2.8 Reset

The SµMMIT XT provides for several different reset mechanisms. The SµMMIT XT software reset (Control Register Bit 13) is equal to a master reset and takes 5µs to complete. Assertion of this bit results in the immediate reset of the SRT and termination of command processing. The host or subsystem is responsible for the re-initialization of the SRT for operation. Configuration of the device for auto-initialization frees the host or subsystem from this task.

A Reset Remote Terminal mode code (Mode Code 01000, $T/\overline{R}$ =1) is equal to a master reset only if $\overline{\text{AUTOEN}}$ is enabled. If $\overline{\text{AUTOEN}}$ is not enabled, the reset remote terminal mode code clears the encoder/decoders, resets the time-tag, enables the channels to the programmed host state, and re-enables the Terminal Flag for assertion. This reset is performed after the transmission of the 1553 Status word.

Caution: Per the MIL-STD-1553 specification (sections 4.3.3.5.1.7.9 and 30.4.3), a remote terminal must "complete the reset function within 5ms following transmission of the status word." If the $\overline{\text{AUTOEN}}$ function is enabled in the SμMMIT XT, reset may require additional time depending on the application.

2.9 MIL-STD-1553A Operation

To maximize flexibility, the SμMMIT XT has been designed to operate in many different systems which use various protocols. Specifically, two of the protocols that the SμMMIT XT may be interfaced to are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, the SμMMIT XT may be configured through an external pin or through control register bits (depending on the state of the $\overline{\text{LOCK}}$ pin). Table 4 defines the three ways to program the SμMMIT XT.

Table 4. MIL-STD-1553A Operation

A/$\overline{\text{B}}$ STD (pin or bit)	XMT SW (bit only)	RESULT (protocol selected)
0	X	1553B response, 1553B Standard
1	0	1553A response, 1553A Standard
1	1	1553A response, Auto execute the TRANSMIT LAST STATUS WORD mode code.

When configured as a remote terminal to meet MIL-STD-1553A, the SμMMIT XT will operate as follows:

- responds with a status word within 7μs;
- ignores the T/$\overline{\text{R}}$ bit for all mode codes;
- all mode codes are defined without data;
- all mode codes use mode code transmit control and information words;
- mode code 00000 is defined as Dynamic Bus Control (DBC);
- subaddress 00000 defines a mode code;
- ME and TF bits are defined in the 1553 status word; all other status word bits are programmable (i.e., NO BUSY mode, etc.);
- broadcast of all mode codes, except Mode Code 00000 (DBC) and Mode Code 00010 (Transmit Status word if enabled), is allowed;
- to illegalize a Mode Code, the user needs to illegalize both the receive and transmit versions;
- illegalization of row 1F (hex) is not automatic.

3.0 Bus Controller Architecture

The SμMMIT XT bus controller (SBC) is an interface device linking a MIL-STD-1553 serial data bus to a host microprocessor and/or subsystem. The SBC's architecture is based on a Command Block structure and internal, programmable registers. Designed to run autonomously and reduce host overhead, the SBC's RISC-based core automatically executes data handling, message error checking, memory control, and related protocol functions. This section discusses the following SBC features and functions:

- Multiple Message Processing
- Message Scheduling
- Polling Capability
- Executable Architecture
- Built-In Test
- Interrupt Structure
- Memory Management

3.1 Register Descriptions

To initialize the SμMMIT XT as a bus controller, the designer must understand the internal registers. The SBC registers offer many programmable functions and allow host access to extensive information. All registers have active high bits and, on master reset, all bits (except those reflecting input pins) will be initialized to inactive low (0000 hex). Each register associated with the bus controller mode of operation is individually described below.

Register Number	Name	Register Address
0	Control Register	0000 (hex)
1	Operational Status Register	0001 (hex)
2	Current Command Block Register	0002 (hex)
3	Interrupt Mask Register	0003 (hex)
4	Pending Interrupt Register	0004 (hex)
5	Interrupt Log List Pointer Register	0005 (hex)
6	BIT Word Register	0006 (hex)
7	Minor-Frame Timer	0007 (hex)
8	Command Block Pointer Register	0008 (hex)
9	Not Applicable	0009 (hex)
10	BC Command Block Initialization Count Register	000A (hex)
11-31	Not Applicable	000B to 001F (hex)

3.1.1 Control Register (Read/Write)- Register 0

The Control Register's function is to configure the SμMMIT XT for operation. To make changes to the SBC and this register, the STEX bit (Bit 15) must be logic zero. To operate the SμMMIT XT as a bus controller (SBC), use the following bits.

Bit Number	Mnemonic	Description
15	STEX	Start Execution. Assertion of this bit commences operation of the SμMMIT XT. A Control Register write negating this bit inhibits operation of the SμMMIT XT. After execution begins, a write of logic zero will halt the SBC after completing the current 1553 message.
14	SBIT	Start BIT. Assertion of this bit places the SμMMIT XT into the Built-In Test routine. The BIT test takes 1ms to execute and has a fault coverage of 93.4%. Once the SμMMIT XT has been started, the host must halt the device in order to place the SμMMIT XT into the Built-In Test routine (STEX = 0) or use the bit opcode. Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13	SRST	Start Software Reset. Assertion of this bit immediately places the SμMMIT XT into a software reset. Like $\overline{\text{MRST}}$, the software reset (which takes 5μs to execute) clears all internal logic. Note: During auto-initialization, do not load this bit with a logic one. SRST will only function after $\overline{\text{READY}}$ is asserted.
12-11	N/A	Not Applicable.
10	ETCE	External Timer Clock Enable. Assertion of this bit enables an external clock used with an internal counter for variable minor frame timing. Refer to section 3.1.8. Note: The user can only change the clock frequency before starting the device (i.e., setting bit 15 of Register 0 to a logic one).
9-7	N/A	Not Applicable.
6	BUFR	Buffer Mode Enable. Assertion of this bit enables the buffer mode of operation. Refer to section 8.5 for more information.
5	N/A	Not Applicable.
4	BCEN	Broadcast Enable. Assertion of this bit enables the broadcast option for the SBC. Negation of this bit enables the remote terminal address 31 as a unique RT address. When enabled, the SBC does not expect a status word response from the remote terminal.
3	N/A	Not Applicable.
2	PPEN	Ping-Pong Enable. This bit controls the method by which the SBC will retry messages. A logic one allows the SBC to ping-pong between buses during retries. A logic zero dictates that all retries will be performed on the programmed bus as defined in the Command Block control word. (Section 3.2.1 of this document defines the retry bit).
1	INTEN	Interrupt Log List Enable. Assertion of this bit enables the Interrupt Log List. Negation of this bit prevents the logging of interrupts as they occur.
0	N/A	Not Applicable.

3.1.2 Operational Status Register (Read/Write) - Register 1

This register provides pertinent status information for the SBC and is not reset to 0000 (hex) on $\overline{\text{MRST}}$. Instead, the register reflects the actual stimulus applied to input pins MSEL(1:0), A/$\overline{\text{B}}$ STD, and $\overline{\text{LOCK}}$. Assertion of the $\overline{\text{LOCK}}$ input prevents the modification of the mode selects and the A or B standard bits. In this case, a write to this register's most significant nine bits is meaningless. If $\overline{\text{LOCK}}$ is negated, a read of this register reflects the information written into this register's most significant nine bits.

Note: To make changes to the SBC and this register, the STEX bit (Register 0, bit 15) must be logic zero.

Bit Number	Mnemonic	Description
15-10	N/A	Not Applicable.
9	MSEL(1)	Mode Select 1. In conjunction with Mode Select 0, this bit determines the SμMMIT XT mode of operation.
8	MSEL(0)	Mode Select 0. In conjunction with Mode Select 1, this bit determines the SμMMIT XT mode of operation. MSEL(1) 0 0 Bus Controller = SBC 0 1 Remote Terminal = SRT 1 0 Monitor Terminal = SMT 1 1 SMT/SRT
7	A/$\overline{\text{B}}$ STD	Military Standard 1553A or 1553B. This bit determines whether the SBC will operate under MIL-STD-1553A or 1553B protocol. Assertion of this bit forces the SBC to look for all responses in 11μs or generate time-out errors. Negation of this bit automatically allows the SBC to operate under the MIL-STD-1553B protocol. See section 3.6 for further information.
6	LOCK	$\overline{\text{LOCK}}$ Pin. This read-only bit reflects the inverted state of the $\overline{\text{LOCK}}$ input pin and is latched on the rising edge of $\overline{\text{MRST}}$.
5	AUTOEN	$\overline{\text{AUTOEN}}$ Pin. This read-only bit defines whether or not the auto enable feature will be used in the design. This bit shows the inverse of the auto enable ($\overline{\text{AUTOEN}}$) input pin.
4	N/A	Not Applicable.
3	EX	SμMMIT XT Executing. This read-only bit indicates whether the SBC is presently executing or is idle. A logic one indicates that the SμMMIT XT is executing; logic zero indicates the SμMMIT XT is idle.
2	N/A	Not Applicable.
1	READY	$\overline{\text{READY}}$ Pin. This read-only bit reflects the inverted state of the output pin $\overline{\text{READY}}$ and is cleared on reset.
0	TERACT	$\overline{\text{TERACT}}$ Pin. Assertion of this bit indicates that the SBC is presently processing a message. This read-only bit reflects the inverted state of output pin $\overline{\text{TERACT}}$ and is cleared on reset.

Note: When STEX transitions from 1 to 0, EX and $\overline{\text{TERACT}}$ stay active until command processing is complete.

BC

3.1.3 Current Command Register (Read-only) - Register 2

This register contains the last 1553 command that was transmitted by the SBC. Upon the execution of each Command Block, this register will automatically be updated. This register is updated when transmission of the Command Word begins. In an RT-RT transfer, the register will reflect the latest Command Word as it is transmitted.

Bit Number	Mnemonic	Description
15-0	CC(15:0)	Current Command. These bits contain the latest 1553 command that was transmitted by the bus controller.

3.1.4 Interrupt Mask Register (Read/Write) - Register 3

The SBC interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked if the corresponding bit of this register is set to a logic zero.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail Interrupt.
14	WRAPF	Wrap Fail Interrupt.
13	N/A	Not Applicable.
12	BITF	BIT Fail Interrupt.
11	MERR	Message Error Interrupt.
10-6	N/A	Not Applicable.
5	EOL	End Of List Interrupt.
4	ILLCMD	Illogical Command Interrupt.
3	ILLOP	Illogical Opcode Interrupt.
2	RTF	Retry Fail Interrupt.
1	CBA	Command Block Accessed Interrupt.
0	N/A	Not Applicable.

3.1.5 Pending Interrupt Register (Read-only) - Register 4

This register is used to identify which of the interrupts occurred during operation. The assertion of any bit in this register asserts an output pin, $\overline{\text{MSG\_INT}}$ or $\overline{\text{YF\_INT}}$. Note that all register bits are cleared on a host read.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail Interrupt. Once the SμMMIT XT has issued the $\overline{\text{DMAR}}$ signal, an internal timer is started. If all DMA activity has not been completed, the interrupt is generated. In the SBC mode, the $\overline{\text{YF\_INT}}$ interrupt is generated (if not masked) and command processing stops.
14	WRAPF	Wrap Fail Interrupt. The SRT automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit asserts and the $\overline{\text{YF\_INT}}$ interrupt is generated. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	N/A	Not Applicable.
12	BITF	BIT Fail Interrupt. Assertion of this bit indicates a BIT failure. Interrogate Bit Word Register bits 11 and 10 to determine the specific channel that failed. In SBC mode, the $\overline{\text{YF\_INT}}$ interrupt is generated and command processing stops if initiated by opcode.
11	MERR	Message Error Interrupt. Assertion of this bit indicates the occurrence of a message error. The SBC can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an $\overline{\text{MSG\_INT}}$ interrupt generated (if not masked) after message processing is complete.
10-6	N/A	Not Applicable.
5	EOL	End Of List Interrupt. Assertion of this bit indicates that the SBC is at the end of the command block. $\overline{\text{MSG\_INT}}$ generated.
4	ILLCMD	Illogical Command Interrupt. Assertion of this bit indicates that an illogical command (i.e., Transmit Broadcast or improperly formatted RT-RT message) was written into the Command Block. The SBC checks for RT-RT Terminal address field match, RT-RT transmit/receive bit mismatch and correct order, and broadcast transmit commands. If illogical commands occur, the SBC will halt execution. $\overline{\text{MSG\_INT}}$ generated.
3	ILLOP	Illogical Opcode Interrupt. Assertion of this bit indicates an illogical opcode (i.e., any reserved opcode) was used in the command block. The SBC halts operation if this condition occurs. $\overline{\text{MSG\_INT}}$ generated.
2	RTF	Retry Fail Interrupt. Assertion of this bit indicates all programmed retries failed. $\overline{\text{MSG\_INT}}$ generated.
1	CBA	Command Block Accessed Interrupt. Assertion of this bit indicates a command block was accessed (Opcode 1010), if enabled. $\overline{\text{MSG\_INT}}$ generated.
0	N/A	Not Applicable.

Note: In the 8-bit mode of operation a single read to the Register 4 clears the entire register.

BC

3.1.6 Interrupt Log List Pointer Register (Read/Write) - Register 5

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts. The SμMMIT XT architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 32K memory space. Initialize the lower five-bits of this register to a logic zero. The SμMMIT XT controls the lower five-bits to implement the ring-buffer architecture. The host or subsystem reads this register to determine the location and number of interrupts within the Interrupt Log List (least significant five-bits).

Bit Number	Mnemonic	Description
15-0	INTA(15:0)	Interrupt Log List Pointer Bits. These bits indicate the starting location of the Interrupt Log List.

3.1.7 BIT Word Register (Read/Write) - Register 6

This register contains information on the current health of the SBC. The lower 8 bits of this register are user-defined.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail. Assertion of this bit indicates that all DMA activity had not been completed when the timer decrements to zero (i.e., 7μs).
14	WRAPF	Wrap Fail. The SBC automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit asserts. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	N/A	Not Applicable.
12	BITF	BIT Fail. Assertion of this bit indicates a BIT failure. Interrogate bit 11 and 10 to determine the specific channel that failed.
11	CHAF	Channel A Fail. Assertion of this bit indicates a BIT test failure in Channel A.
10	CHBF	Channel B Fail. Assertion of this bit indicates a BIT test failure in Channel B.
9	MSBF	Memory Test Fail. Most significant memory byte failure.
8	LSBF	Memory Test Fail. Least significant memory byte failure.
7-0	UDB(7:0)	User-Defined Bits.

3.1.8 Minor Frame Timer Register (Read-only) - Register 7

This register is loaded via the Minor Frame Timer (MFT) opcode (Opcode 1110). For user-defined resolution use TCLK.

Bit Number	Mnemonic	Description
15-0	MFT(15:0)	Minor Frame Timer. These bits indicate the value of the Timer.

3.1.9 Command Block Pointer Register (Read/Write) - Register 8

This register contains the location to start the Command Blocks. After execution begins, this register is automatically updated with the address of the next block.

Bit Number	Mnemonic	Description
15-0	CBA(15:0)	Command Block Address. These bits indicate the starting location of the Command Block.

3.1.10 BC Command Block Initialization Count Register (Read/Write)-Register 10

This register contains the number of command blocks that will be initialized when using the auto-initialize feature. If 0000H is written into this register, then NO blocks will be set up. Because each Command Block requires eight contiguous memory locations, the largest value allowed in this register is 1FFFH. If a larger value is written into this register, the SBC ignores the three most significant bits.

Bit Number	Mnemonic	Description
15-0	CBC(15:0)	Command Block Count. These bits indicate the number of Command Blocks set up during auto-initialization.

3.2 SBC Architecture

As defined in MIL-STD-1553, the bus controller initiates all communications on the bus. To meet MIL-STD-1553 bus controller requirements, the SμMMIT XT utilizes a Command Block architecture that takes advantage of both internal registers and internal memory. Each command word transmitted over the bus must be associated with a Command Block. The Command Block requires eight contiguous memory locations for each message. These eight locations include a control word, two command word locations, a data pointer, two status word locations, a branch address location, and a timer value.

The host, or ROM for autonomous operation, must initialize each of the locations associated with each Command Block (the exception is for the two status locations which will be updated as command words are transmitted and corresponding status words are received). Figure 6 shows the SBC's Command Block architecture while Sections 3.2.1 through 3.2.6 describe each location associated with the Command Block.

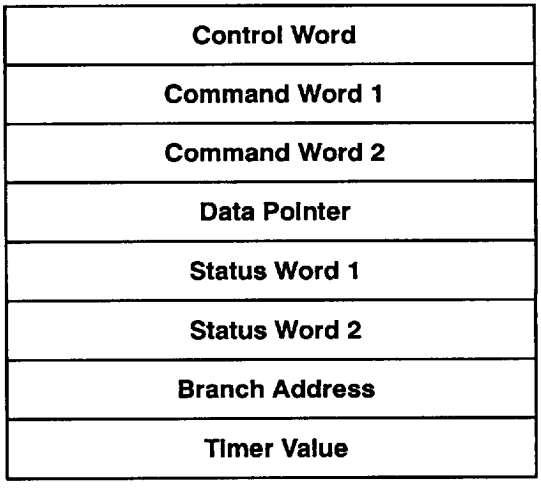


Figure 6. SBC Command Block Architecture

3.2.1 Control Word

The first memory location of each SBC Command Block contains the control word. Each control word contains the opcode, retry number, bus definition, RT-RT instruction, condition codes, and the block access message error. The SBC's control word is defined below.

15 12	11 10	9	8	7 1	0
Opcode	Retry #	CHA/$\overline{B}$	RT-RT	Condition Codes	Block Access ME

Bit Number	Description
15-12	Opcode. These bits define the opcode to be used by the SBC for that particular Command Block. If the opcode does not perform any 1553 function, all other bits are ignored. Each of the available opcodes is defined in section 3.2.1.1.
11-10	Retry Number. These bits define the number of retries for each individual Command Block and if a retry opcode is used. If bit 2 of the Control Register is not enabled, all retries will occur on the programmed bus. However, if bit 2 is enabled, the first retry will always occur on the alternate bus, the second retry will occur on the primary bus, the third retry will occur on the alternate bus, and the fourth retry will occur on the primary bus.

BIT 11	BIT 10	# of Retries
0	1	1
1	0	2
1	1	3
0	0	4

9	Bus A/$\overline{B}$. This bit defines on which of the two buses the command will be transmitted (i.e., primary bus). (Logic 1 = Bus A, Logic 0 = Bus B).
8	RT-RT Transfer. This bit defines whether or not the present Command Block is an RT-RT transfer and if the SBC should transmit the second command word. Data associated with an RT-RT is always stored by the SBC.
7-1	Condition Codes. These bits define the condition code the SBC uses for that particular Command Block. Each of the available condition codes are defined in section 3.2.1.2.
0	Block Access Message Error. Assertion of this bit indicates a protocol message error occurred in the RT's response. For this occurrence, the SBC will overwrite this bit prior to storing the Control Word into memory. Noise on the 1553 bus may be one example of such an error.

3.2.1.1 Opcode Definition

Opcode	Definition
0000	End Of List. This opcode instructs the SBC that the end of the command block has been encountered. Command processing stops and the interrupt is generated if the interrupt is enabled. No command processing takes place (i.e., no 1553).
0001	Skip. This opcode instructs the SBC to load the message-to-message timer with the value stored in timer value location. The SμMMIT XT will then wait the specified time before proceeding to the next command block. This opcode allows for scheduling of specific time between message execution. No command processing takes place (i.e., no 1553).
0010	Go To. This opcode instructs the SBC to "go to" the command block as specified in the branch address location. No command process takes place (i.e., no 1553).
0011	Built-in Test. This opcode instructs the SBC to perform an internal built-in test. If the device passes the built-in test, then processing of the next command block will continue. However if the device fails the built-in test, then processing stops and an interrupt is generated, if the interrupt is enabled. No command processing takes place (i.e., no 1553).
0100	Execute Block; Continue. This opcode instructs the SBC to execute the current command block and proceed to the next command block. This opcode allows for continuous operations.
0101	Execute Block; Branch. This opcode instructs the SBC to execute the current command block and unconditionally branch to the location as specified in the branch address location.
0110	Execute Block; Branch on Condition. This opcode instructs the SBC to execute the current command block and branch only if the condition is met. If no conditions are met, the opcode appears as an execute and continue.
0111	Retry on Condition. This opcode instructs the SBC to perform automatic retries, as specified in the control word, if particular conditions occur. If no conditions are met, the opcode appears as an execute and continue.
1000	Retry on Condition; Branch. This opcode instructs the SBC to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met, the SBC retries. Once all retries have executed, the SBC branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and branch.
1001	Retry on Condition; Branch if all Retries Fail. This opcode instructs the SBC to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met and all the retries fail, the SBC branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and continue.
1010	Interrupt; Continue. This opcode instructs the SBC to interrupt and continue processing on the next command block. When using this opcode, no 1553 processing occurs.
1011	Call. This opcode instructs the SBC to "go to" the command block as specified in the branch address location without processing this block. The next command block address is saved in an internal register so that the SμMMIT XT may remember one address and return to the next command block. No command processing takes place (i.e., no 1553).
1100	Return to Call. This opcode instructs the SBC to return to the command block address saved during the Call opcode. No command processing takes place (i.e., no 1553).
1101	Reserved. The SBC will generate an illegal opcode interrupt (if interrupt enabled) and automatically stop execution if a reserved opcode is used.

Opcode	Definition
1110	Load Minor Frame Timer. This opcode instructs the SBC to load the minor frame timer (MFT) with the value stored in the eighth location of the current command block. The timer will be loaded after the previous MFT has decremented to zero. After the MFT timer is loaded with the new value, the SBC will proceed to the next command block. No command processing takes place (i.e., no 1553).
1111	Return to Branch. This opcode instructs the SBC to return to the command block address saved during a Branch opcode. No command processing takes place (i.e., no 1553).

Note: For retries with interrupts enabled, all interrupts are logged after message processing is complete.

3.2.1.2 Condition Codes

Condition codes have been provided as a means for the SBC to perform certain functions based on the RT's status word. In an RT-RT transfer, the conditions apply to both of the status words. Each bit of the condition codes is defined below.

Bit Number	Description
7	Message Error. This condition will be met if the SBC detects an error in the RT's response, or if it detects no response. (The SBC will wait 15μs in 1553B mode and 11μs in 1553A mode before declaring an RT no response.)
6	Status Word Response with the Message Error bit set (Bit time 9 in 1553A mode). This condition is met if the SBC detects that the RT's status word has the Message Error bit set.
5	Status Word Response with the Busy bit set (Bit time 16 in 1553A mode). This condition is met if the SBC detects that the RT's status word has the Busy bit set.
4	Status Word Response with the Terminal Flag bit set (Bit time 19 in 1553A mode). This condition is met if the SBC detects that the RT's status word has the Terminal Flag bit set.
3	Status Word Response with the Subsystem Fail bit set (Bit time 17 in 1553A mode). This condition is met if the SBC detects that the RT's status word has the Subsystem Fail bit set.
2	Status Word Response with the Instrumentation bit set (Bit time 10 in 1553A mode). This condition is met if the SBC detects that the RT's status word has the Instrumentation bit set.
1	Status Word Response with the Service Request bit set (Bit time 11 in 1553A mode). This condition is met if the SBC detects that the RT's status word has the Service Request bit set.

3.2.2 Command Words

The next two locations of the SBC Command Block are for 1553 command words. In most 1553 messages, only the first command word needs to be initialized. However, in an RT-RT transfer, the first command word is the Receive Command and the second command word is the Transmit Command.

3.2.3 Data Pointer

The fourth location in the SBC Command Block is the data pointer that points to the first memory location to store or fetch the data words associated with the message for that command block. This data structure allows the SBC to store or fetch the exact specified number of data words, thus saving memory space and providing efficient space allocation. (Note: In an RT-RT transfer, the SBC uses the data pointer as the location in memory to store the transmitted data in the transfer.) One common application for the data pointer occurs when the SBC needs to send the same data words to several RTs.

Here, each Command Block associated with those messages would contain the same data pointer value, and, therefore, fetch and transmit the same data. Note that the Data Pointer is never updated (i.e., the SBC reads and writes the pointer but never changes its value).

3.2.4 Status Words

The next two locations in the SBC Command Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. In an RT-RT transfer, the first status word will be the status of the Transmitting RT while the second status word will be the status of the Receiving RT.

3.2.5 Branch Address

The seventh location in the SBC Command Block contains the starting location of the branch. This location simply allows the SBC to branch to another location in memory when certain opcodes are used.

3.2.6 Timer Value

The last location in the SBC Command Block is the Timer Value. This timer is used for one of two purposes. First, the value may be used to set up minor frame schedules when using the Load Minor Frame Timer opcode (1110). The MFT counter may be driven by the TCLK input. If not driven by the TCLK input, the MFT counter is clocked at a 64µs internal clock. The MFT counter runs continuously during message processing and must decrement to zero prior to loading the next Minor Frame time value. Second, the value may be used as a message-to-message timer (MMT) when using the Skip opcode (0001). The MMT timer is clocked at the 24MHz rate and allows for scheduling of specific time between message execution.

3.3 Command Block Chaining

The host determines the first Command Block by setting the initial start address in the Command Block Pointer Register (Reg 8). The Command Blocks will execute in a contiguous fashion as long as no "go to", "branch", "call", or "return" opcodes are used. With the use of these opcodes, almost any memory configuration is possible. Figures 7a, 7b, and 8 show how several Command Blocks may be linked together to form a command frame and how branch opcodes may be used to link minor frames. The minimum BC intermessage gap is 28.0µs.

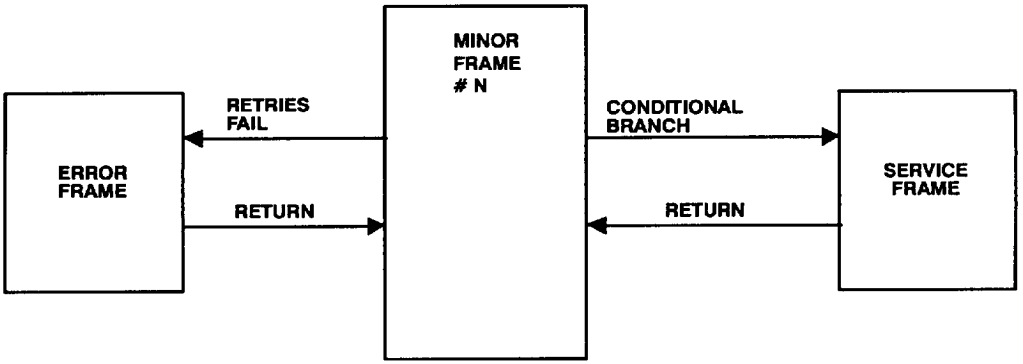


Figure 7a. Minor Frame Branching

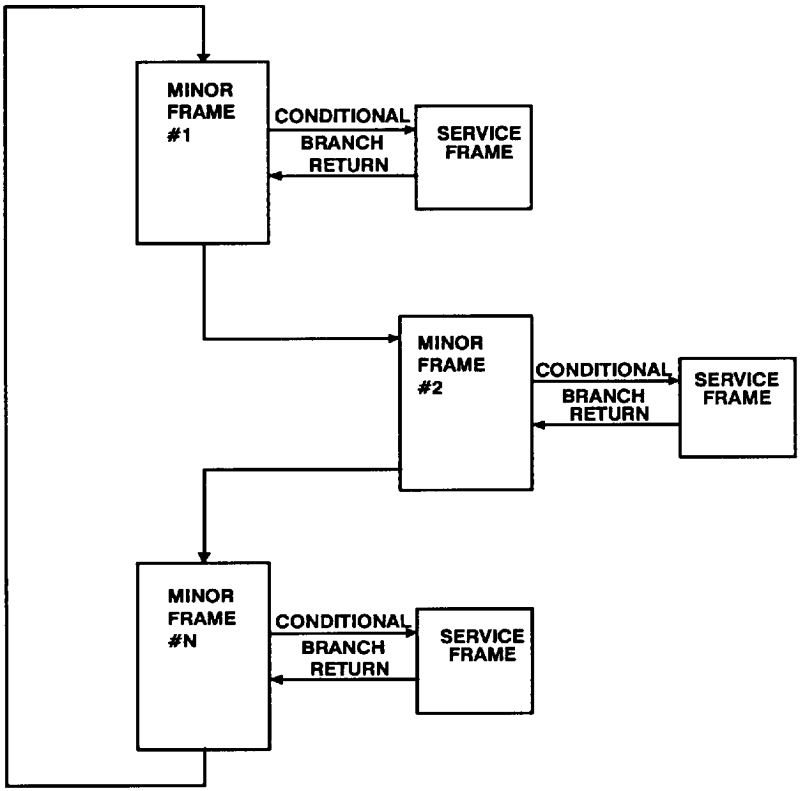


Figure 7b. Major Frame Sequencing

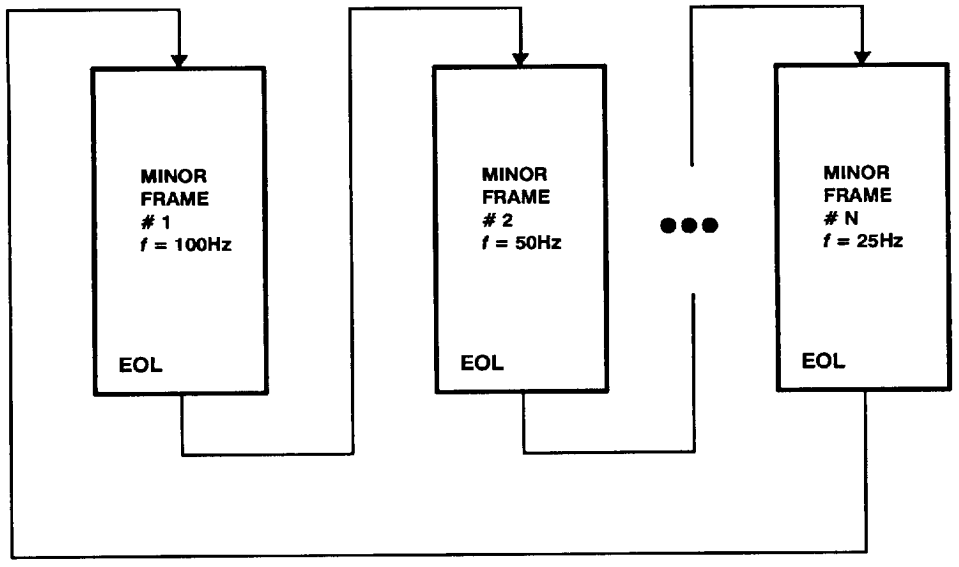


Figure 8. Minor Frame Sequencing

3.4 Memory Architecture

After reviewing the SBC's internal registers, it may be advantageous to look at the external memory requirements and how the host sets up memory to make the SμMMIT XT a bus controller. The intent of this section is to show one method for defining the memory configuration.

The configuration shows the Command Blocks, data locations, and the Interrupt Log List as separate entities. Figure 9 shows that the first block of memory is allocated for the Command Blocks. Notice that Register 8 initially points to the control word of the first Command Block. After completing execution of that first Command Block, Register 8 will automatically be updated to show the address associated with the next Command Block.

Following the Command Block locations is the memory required for all the data words. In BC applications, the number of data words for each Command Block is known. In figure 9, for example, the first Command Block has allocated several memory locations for expected data. Conversely, the second Command Block has only allocated a few memory locations. Since the number of data words associated with each Command Block is known, memory may be used efficiently.

Also shown as a separate memory area is the Interrupt Log List (refer to section 5.0 for a description of the Interrupt Log List). Notice that Register 5 points to the top of the initial Log List. After execution of that first SBC Command Block, Register 5 will automatically be updated.

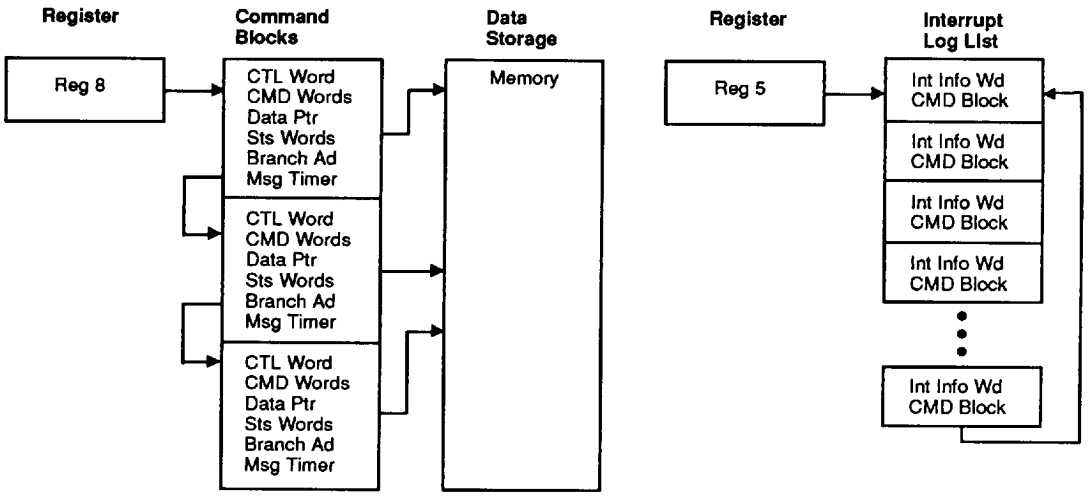


Figure 9. Memory Architecture for BC Mode

3.5 Message Processing

To process messages, the SBC uses data supplied in the internal registers along with data stored in external memory. The SBC accesses eight words stored in external memory called a command block. The command block is accessed at the beginning and end of command processing.

The SμMMIT XT features two different modes of transferring data to or from RAM: Buffer and Non-Buffer. The user selects the Buffer or Non-Buffer transfer mode by setting the BUFR bit (bit 6) in the control register.

Note: In the SBC mode of operation, the SμMMIT XT does not need to re-read the Command Block on a retry situation. Both transfer modes are described below.

The host or subsystem controlling the SBC allocates memory spaces for the minor frame. The top of the command blocks can reside at any address location. Defined and entered into memory by the host, the SBC is linked to the Command Block via the Command Block Pointer Register contents. Each command block contains a Control Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, Branch Address, and Timer Value. Refer to sections 3.2.1 - 3.2.6 for a complete description of each location.

Control word information allows the SBC to control the commands transmitted over the 1553 bus. The Control word allows the SBC to transmit commands on a specific channel, perform retries, initiate RT-RT transfers, and interrupt on certain conditions. The host or subsystem defines each command word associated with each command block. For normal 1553 commands, only the first command word location will contain valid data. For RT-RT commands, as specified in the Control word, the host must define the first command word as a receive and the second command word as a transmit.

For a receive command the Data Pointer is read to determine where data words are retrieved. The SBC retrieves data words sequentially from the address specified by the Data Pointer. For a transmit command the Data Pointer is read to determine the top memory location. The SBC stores data words sequentially from this top memory location.

Table 5. MIL-STD-1553A Operation

A/B STD (pin)	LOCK (pin)	RESULT
0	1	1553B response, 1553B standard
0	0	1553B response, 1553B standard
1	1	1553A response, 1553A standard
1	0	1553A response, 1553A standard

3.6 MIL-STD-1553A Operation

As discussed in section 2.9, the SμMMIT XT may be configured to meet the MIL-STD-1553A protocol.

When configured as a MIL-STD-1553A bus controller, the SμMMIT XT will operate as follows:

- looks for the RT response within 7μs;
- defines all mode codes without data;
- defines subaddress 00000 as a mode code.

4.0 Monitor Terminal Architecture

In many applications, the SμMMIT XT's Monitor Terminal may be required to be the Backup Bus Controller (BBC). With this in mind, the SμMMIT XT's monitor terminal (SMT) architecture is designed to function like the SBC's architecture. The SMT's architecture is based on a Monitor Block structure and internal, programmable registers. Designed to run autonomously and reduce host overhead, the SMT automatically executes data handling, message error checking, memory control, and related protocol functions. Discussed in this section are the following Monitor features and functions:

- Command History List
- Executable Architecture
- BIT Capability
- Interrupt History List
- Monitor All or Selected Terminals
- Memory Management

MT

4.1 Register Descriptions

To initialize the SμMMIT XT as a monitor terminal, the designer must understand the internal registers. A complete description of each register and the associated bits is provided. These registers offer many programmable functions and allow host access to extensive information.

All registers have active high bits, and, on master reset, all bits (except those reflecting input pins) will be initialized to inactive low. Each register associated with the monitor mode of operation is described below.

Register Number	Name	Register Address
0	Control Register	0000 (hex)
1	Operational Status Register	0001 (hex)
2	Current Command Block Register	0002 (hex)
3	Interrupt Mask Register	0003 (hex)
4	Pending Interrupt Register	0004 (hex)
5	Interrupt Log List Pointer Register	0005 (hex)
6	BIT Word Register	0006 (hex)
7	Time-Tag Register	0007 (hex)
8-10	Not Applicable	0008 to 000A (hex)
11	Initial Monitor Command Block Pointer Register	000B (hex)
12	Initial Monitor Data Pointer Register	000C (hex)
13	Monitor Block Counter Register	000D (hex)
14	Monitor Filter Register	000E (hex)
15	Monitor Filter Register	000F (hex)
16-31	Not Applicable	0010 to 001F (hex)

4.1.1 Control Register (Read/Write) - Register 0

To operate the SμMMIT XT as a monitor terminal, use the following bits. To make changes to the SMT and this register, the STEX bit (Bit 15) must be logic zero.

Note: The user has 5μs after $\overline{\text{TERACT}}$ active to stop execution.

Bit Number	Mnemonic	Description
15	STEX	Start Execution. Assertion of this bit commences operation of the SμMMIT XT. A Control Register write negating this bit inhibits operation of the SμMMIT XT. After execution has begun, a write of a logic zero will halt the SMT after completing the current 1553 message.
14	SBIT	Start BIT. Assertion of this bit places the SμMMIT XT into the Built-In Test routine. The BIT test takes 1ms to execute and has a 93.4% fault coverage. If the SμMMIT XT has been started, the host must halt the device in order to place the SμMMIT XT into the Built-In Test routine (STEX = 0). Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13	SRST	Start Software Reset. Assertion of this bit immediately places the SμMMIT XT into a software reset. The software reset (which takes 5μs to execute) clears all internal logic, just as the $\overline{\text{MRST}}$ does. Note: During auto-initialization, do not load this bit with a logic one. SRST will only function after $\overline{\text{READY}}$ is asserted.
12-11	N/A	Not Applicable.
10	ETCE	External Timer Clock Enable. If this bit is set to logic one, the SMT will use the external input clock to drive the Time-Tag counter. If set to logic zero, the SMT will use an internal clock to drive the time tag counter. Refer to section 4.1.8. Note: The user can only change the clock frequency before starting the device (i.e., setting bit 15 of Register 0 to a logic one).
9-7	N/A	Not Applicable.
6	BUFR	Buffer Mode Enable. Assertion of this bit enables the buffer mode of operation. For more detailed information on this feature refer to section 8.5.
5	SMTC	Monitor Control. This bit determines whether the SMT will monitor all RTs or selected RTs. If this bit is set to logic zero, the SMT will monitor all RTs. If this bit is set to logic one, the SMT will monitor only the RTs as specified in the Monitor Filter Registers (Registers 14 and 15).
4	BCEN	Broadcast Enable. This bit, if set to logic one, allows RT address 31 to be used as a Broadcast message. If set to logic zero, then address 31 is a normal address.
3-2	N/A	Not Applicable.
1	INTEN	Interrupt Log List Enable. Assertion of this bit enables the Interrupt Log List. Negation of this bit prevents the logging of interrupts as they occur.
0	N/A	Not Applicable.

4.1.2 Operational Status Register (Read/Write) - Register 1

This register reflects pertinent status information for the SMT and is not reset to 0000 (hex) on $\overline{\text{MRST}}$. Instead, the register reflects the actual stimulus applied to input pins RTA(4:0), RTAPTY, MSEL(1:0), A/$\overline{\text{B}}$ STD, and $\overline{\text{LOCK}}$. Assertion of the $\overline{\text{LOCK}}$ input prevents the modification of the remote terminal address, mode selects, and the A or B Standard bits. In this case, a write to this register's most significant nine bits is meaningless. If $\overline{\text{LOCK}}$ is negated, a read of this register reflects the information written into this register's most significant nine bits.

Note: To make changes to the SMT and this register, the STEX bit (Register 0, bit 15) must be logic zero.

Bit Number	Mnemonic	Description
15-10	N/A	Not Applicable.
9	MSEL(1)	Mode Select 1. In conjunction with Mode Select 0, this bit determines the SμMMIT XT mode of operation.
8	MSEL(0)	Mode Select 0. In conjunction with Mode Select 1, this bit determines the SμMMIT XT mode of operation.

MSEL(1)	MSEL(0)	Mode of Operation
0	0	Bus Controller = SBC
0	1	Remote Terminal = SRT
1	0	Monitor Terminal = SMT
1	1	SMT/SRT

7	A/$\overline{\text{B}}$ STD	Military Standard 1553A or 1553B Standard. This bit determines whether the SMT will look for the RT's response in 11μs (MIL-STD-1553A) or in 12μs (MIL-STD-1553B). Assertion of this bit forces the SMT to declare a time-out error condition if the RT has not responded in 7μs. Negation of this bit allows the SMT to declare a time-out error condition if the RT has not responded in 15μs. See section 4.7 for further definition.
6	LOCK	$\overline{\text{LOCK}}$ Pin. This read-only bit reflects the inverted state of the LOCK input pin. The Lock pin is latched on the rising edge of $\overline{\text{MRST}}$. If modes of operation must change, the user must perform a MRST.
5	AUTOEN	$\overline{\text{AUTOEN}}$ Pin. This read-only bit defines whether or not the auto enable feature will be used in the design. This bit shows the inverse of the auto enable ($\overline{\text{AUTOEN}}$) input pin.
4	N/A	Not Applicable.
3	EX	SμMMIT XT Executing. This read-only bit indicates whether the SMT is presently executing or whether it is idle. A logic one indicates that the SμMMIT XT is executing, logic zero idle.
2	N/A	Not Applicable.
1	READY	$\overline{\text{READY}}$ Pin. This read-only bit reflects the inverted state of the output pin $\overline{\text{READY}}$ and is cleared on reset.
0	TERACT	Terminal Active Pin. Assertion of this bit indicates that the SMT is presently processing a message. This read-only bit reflects the inverted state of output pin $\overline{\text{TERACT}}$ and is cleared on reset.

4.1.3 Current Command Register (Read-only) - Register 2

This register contains the last valid command that was transmitted over the 1553 bus. In an RT-RT transfer, this register will update as each of the two commands are received by the SMT.

Bit Number	Mnemonic	Description
15-0	CC(15:0)	Current Command. These bits contain the latest 1553 word that was received by the SMT.

4.1.4 Interrupt Mask Register (Read/Write) - Register 3

The SMT interrupt architecture allows the host or subsystem to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked if the corresponding bit of this register is set to logic zero.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail Interrupt.
14-13	N/A	Not Applicable.
12	BITF	BIT Fail Interrupt.
11	MERR	Message Error Interrupt.
10-1	N/A	Not Applicable.
0	MBC	Monitor Block Counter Interrupt.

4.1.5 Pending Interrupt Register (Read-only) - Register 4

The pending interrupt register is used to identify which of the interrupts occurred during operation. Note that all register bits are cleared on a host read.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail Interrupt. Once the SμMMIT XT has issued the $\overline{\text{DMAR}}$ signal, an internal timer is started. If all DMA activity has not been completed, the interrupt is generated (if not masked). In the SMT mode, the $\overline{\text{YF\_INT}}$ interrupt is generated, current command processing will end, and the SMT will remain on-line.
14-13	N/A	Not Applicable.
12	BITF	BIT Fail Interrupt. Assertion of this bit indicates a BIT failure. Interrogate bits 11 and 10 of the BIT Word Register to determine the specific channel that failed. $\overline{\text{YF\_INT}}$ interrupt generated, operation continues.
11	MERR	Message Error Interrupt. This bit is set if a message error occurs. The SMT can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and interrupt generated after message processing is complete. $\overline{\text{MSG\_INT}}$ interrupt generated.
10-1	N/A	Not Applicable.
0	MBC	Monitor Block Counter Interrupt. This bit is set if the SMT's monitor block counter reaches zero (transition from 1 to 0). It should be noted that the SMT does not discriminate between error-free messages and those messages with errors. $\overline{\text{MSG\_INT}}$ interrupt generated.

Note: In the 8-bit mode of operation a single read to the Register 4 clears the entire register.

4.1.6 Interrupt Log List Pointer Register (Read/Write) - Register 5

This register indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts. The SμMMIT XT architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 32K memory space. Initialize the lower five-bits of this register to a logic zero. The SμMMIT XT controls the lower five-bits to implement the ring-buffer architecture. The host or subsystem reads this register to determine the location and number of interrupts within the Interrupt Log List (least significant five-bits).

Bit Number	Mnemonic	Description
15-0	INTA(15:0)	Interrupt Log List Pointer Bits. These bits indicate the starting location of the Interrupt Log List.

4.1.7 BIT Word Register (Read/Write)- Register 6

This register contains information on the current health of the SMT. The lower 8 bits of this register are user-defined.

Bit Number	Mnemonic	Description
15	DMAF	DMA Fail. This bit is set if all DMA activity is not been completed between the time $\overline{\text{DMAR}}$ asserts and when the timer decrements to zero (i.e., 7μs).
14-13	N/A	Not Applicable.
12	BITF	BIT Fail. Assertion of this bit indicates a BIT failure. Interrogate bits 11 and 10 to determine the specific channel that failed.
11	CHAF	Channel A Fail. Assertion of this bit indicates a BIT test failure in Channel A.
10	CHBF	Channel B Fail. Assertion of this bit indicates a BIT test failure in Channel B.
9	MSBF	Memory Test Fail. Most significant memory byte failure.
8	LSBF	Memory Test Fail. Least significant memory byte failure.
7-0	UDB(7:0)	User-Defined Bits.

4.1.8 Time-Tag Register (Read/Write) - Register 7

This register reflects the state of a 16-bit free running ring counter in the SRT and SMT modes. This counter will remain a free running counter as long as the device is not in $\overline{\text{MRST}}$ or in a software reset mode. The resolution of this counter is user-defined via input TCLK or fixed at 64μs/bit. The Time-Tag counter begins operation on the rising edge to $\overline{\text{MRST}}$.

Bit Number	Mnemonic	Description
15-0	TT(15:0)	Time-Tag Counter Bits. These bits indicate the state of the 16-bit internal counter.

4.1.9 Initial Monitor Block Pointer Register (Read/Write) - Register 11

This register contains the starting location of the Monitor Blocks.

Note: It is recommended that this register not be changed while the SMT is active (i.e., Register 1, bit 3 = 1).

Bit Number	Mnemonic	Description
15-0	MBA(15:0)	Initial Monitor Block Address. These bits indicate the starting location of the Monitor Block.

4.1.10 Initial Monitor Data Pointer Register (Read/Write) - Register 12
This register contains the starting location of the Monitor Data.

Note: It is recommended that this register not be changed while the SMT is active (i.e., Register 1, bit 3 = 1).

Bit Number	Mnemonic	Description
15-0	MDA(15:0)	Initial Monitor Data Address. These bits indicate the starting location of the Monitor Data.

4.1.11 Monitor Block Counter Register (Read/Write) - Register 13
This register contains the number of Monitor Blocks the user wishes to log. After execution begins, this register automatically decrements as commands are logged. When this register is decremented from one to zero, an interrupt will be generated, if enabled. The SMT will start over at the initial pointers as identified in Registers 11 and 12.

Note: It is recommended that this register not be changed while the SMT is active (i.e., Register 1, bit 3 = 1).

Bit Number	Mnemonic	Description
15-0	MBC(15:0)	Monitor Block Count. These bits indicate the number of Monitor Blocks to log.

4.1.12 Monitor Filter Register (Read/Write) - Register 14
This register determines which RTs (RT 31 through RT 16) the SMT will monitor.

Bit Number	Mnemonic	Description
15-0	MF(31:16)	Monitor Filter. These bits determine which RT to monitor.

4.1.13 Monitor Filter Register (Read/Write) - Register 15
This register determines which RTs (RT 15 through RT 0) the SMT will monitor.

Bit Number	Mnemonic	Description
15-0	MF(15:0)	Monitor Filter. These bits determine which RT to monitor.

4.2 SMT Architecture

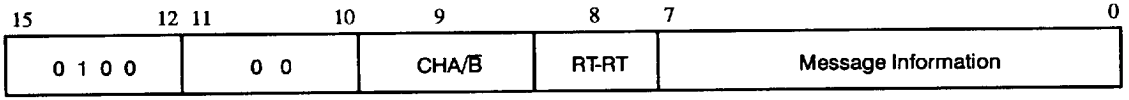
To meet the MIL-STD-1553 monitor requirements, the SMT utilizes a Monitor Block architecture that takes advantage of both internal registers and external memory. The Monitor Block, which is located in external contiguous memory, requires eight locations for each message. These eight locations include a message information word, two command word locations, a data pointer, two status word locations, a time-tag location, and an unused location.

The host, or ROM for autonomous operation, must initialize the starting locations of the Monitor Block, the Data Pointer, Block Counter, and the Interrupt Log Pointer. From then on, the SMT will build a Monitor Block for each message it receives over the 1553 bus. Figure 10 shows a diagram of the Monitor Block followed by a description of each location associated with the Monitor Block.

The first memory location of each Monitor Block contains the message information word. Each message information word contains the opcode, retry number, bus definition, RT-RT messages, and the message information.

Message Information Word
Command Word 1
Command Word 2
Data Pointer
Status Word 1
Status Word 2
Time-Tag
Unused

Figure 10. Monitor Block Diagram



4.2.1 Message Information Word

Bit Number	Description
15-12	Default. With the Monitor Block architecture resembling the SBC Command Block architecture, these bits default to a "0100" state (which is the Execute and Continue opcode) in case the monitor must switch to the BC mode of operation.
11-10	Default. With the Monitor Block architecture resembling the SBC, these bits default to a "00" state. If the monitor must switch to the BC, the retries will be set at four per message.
9	Channel A/$\overline{B}$. This bit defines on which of the two buses the command was received. (Logic 1 = Bus A, Logic 0 = Bus B).
8	RT-RT Transfer. This bit defines whether or not the message associated with this Monitor Block was an RT-RT transfer and whether the SMT saved the second command word. This bit will be set only if the SMT is instructed to monitor the Receive RT.
7-0	Message Information. These bits define the conditions of the message received by the SMT for that particular Monitor Block. Each of the message information bits is defined in the following section.

MT

4.2.1.1 Message Information Bits

Message information bits are provided as a means to supply more data on the message. In an RT-RT transfer, the information applies to the complete message. Each message information bit is defined below.

Bit Number	Description
7	Message Error. This bit will be set if the monitor detects an error in either the command word, data words, or the RT's status.
6	Mode Code without Data. This bit will be set if the monitor detects that the command being processed is a mode code without data words.
5	Broadcast. This bit will be set if the monitor detects that the command being processed is a broadcast message.
4	Reserved.
3	Time-out Error. This bit will be set if the SRT did not receive the proper number of data words, e.g., the number of data words received was less than the word count specified in the command word.
2	Overrun Error. This bit will be set if the SRT received a word when none were expected or the number of data words received was greater than expected.
1	Parity Error. This bit will be set if a parity error has occurred on the data words or the RT's status word.
0	Manchester Error. This bit will be set if a Manchester error has occurred on either the data words or the RT's status word.

4.2.2 Command Words

The next two locations in the SMT Monitor Block are for command words. In non-RT-RT 1553 messages, only the first command word will be stored. However, in an RT-RT transfer, the first command word is the Receive Command and the second command word is the Transmit Command.

4.2.3 Data Pointer

The fourth location in the SMT Monitor Block is the data pointer. This pointer points to the first memory location to store the data words associated with the message for this block. Note that the data associated with each individual message will be stored contiguously. This data structure allows the SMT to store the specified number of data words. (Note: In an RT-RT transfer, the SMT uses the data pointer as the location in memory to store the transmitting data in the transfer.)

4.2.4 Status Words

The next two locations in the SMT Monitor Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. However, in an RT-RT transfer, the first status word will be the status of the Transmitting RT while the second status word will be the status of the Receiving RT.

4.2.5 Time-Tag

The seventh location in the SMT Monitor Block is the time-tag associated with the message. The time-tag is stored into this location at the end of message processing (i.e., captured after the command is validated).

4.2.6 Unused

The last location in the SMT Monitor Block is unused.

4.3 Monitor Block Chaining

The host determines the first Monitor Block by setting the start address in the Initial Monitor Block Pointer Register (Register 11). Figure 11 shows the SMT Monitor Blocks as the blocks execute in a contiguous fashion.

4.4 Memory Architecture

The configuration shows the Monitor Blocks, data locations, and the Interrupt Log List as separate entities. Figure 12 shows that the first block of memory is allocated for the Monitor Blocks. Notice that Register 11 points to the initial Monitor Block location, Register 12 points to the initial Data location, Register 5 points to the Interrupt Log, and Register 13 contains the Monitor Block count. After execution begins, the SMT will build command blocks and store data words until the count reaches zero. When the count reaches zero, the SMT will simply wrap back to the initial values and start again.

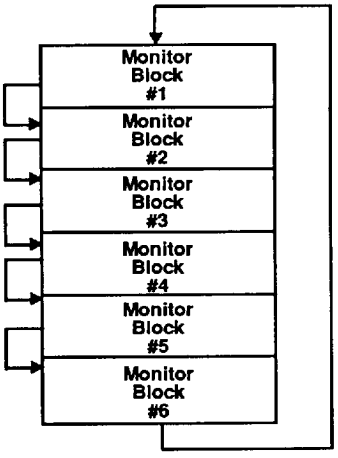


Figure 11. Monitor Block Structuring

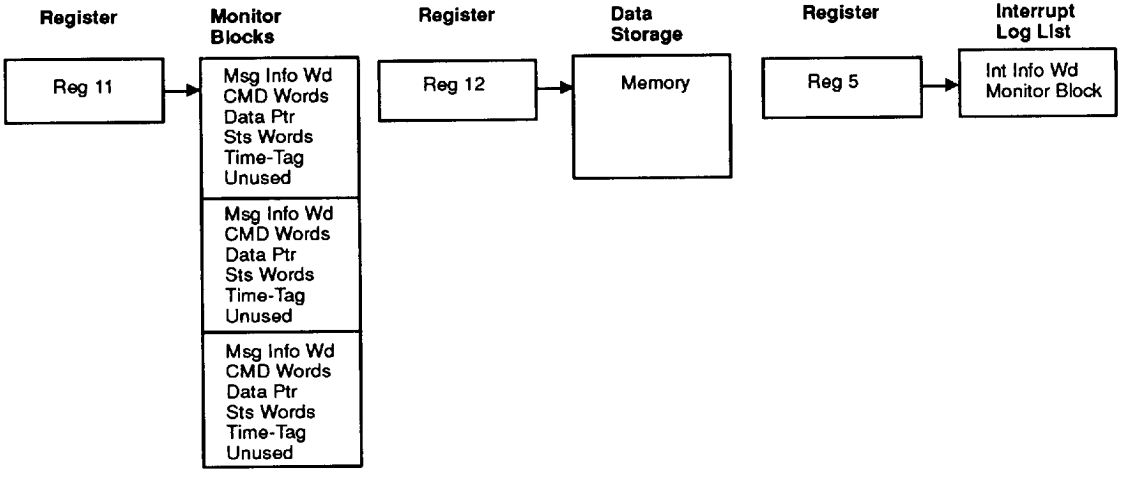


Figure 12. Memory Architecture for Monitor Mode

4.5 Message Processing

To process messages, the SMT uses data supplied in the internal registers along with external memory. The SMT uses seven external memory locations for each message called a monitor block. The monitor block is updated at the end of command processing. The following paragraphs discuss the command block in detail.

The SμMMIT XT features two different modes of transferring data to RAM: Buffer and Non-Buffer. The user selects the Buffer or Non-Buffer transfer mode by setting the BUFR bit (bit 6) in the Control Register.

The host or subsystem controlling the SMT allocates memory spaces for each monitor block. The top of the monitor blocks can reside at any address location. Initialized by the host, the SMT is linked to the Monitor Block via the Initial Monitor Block Pointer Register and the Monitor Block Counter Register contents. Each monitor block contains a Message Information Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, and Time-Tag. Refer to sections 4.2.1 - 4.2.6 for a full description of each location.

The Message Information word allows the SMT to tell the host or subsystem on which bus the command was received, whether the message was an RT-RT transfer, and conditions associated with the message. The SMT also stores each command word associated with the message into the appropriate location. For normal 1553 commands, only the first command word location will contain data. For RT-RT commands, the second command word location will contain data, and bit 8 in the Message Information word will be set.

For each command, the Data Pointer determines where to store data words. The SMT stores data sequentially from the top memory location. The SMT also stores each status word associated with the message into the appropriate location. For normal 1553 commands, only the first status word location will contain data. For RT-RT commands, the second status word location will contain data.

The SMT begins monitoring after Control Register bit 15=1 (i.e., assertion of $\overline{\text{TERACT}}$ and STEX).

After reception, the SMT begins post-processing. The SMT performs a DMA burst during post-processing. An optional interrupt log entry is performed after a monitor block is entered. Monitor Time-Out:

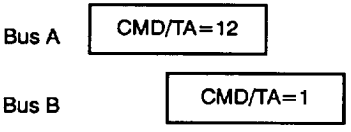
MIL-STD-1553A = 11μs
MIL-STD-1553B = 15μs

4.6 Remote Terminal/Monitor Terminal Operation

For applications that require simultaneous Remote Terminal and Monitor Terminal operations, the SμMMIT XT should be configured as both a remote terminal (SRT) and monitor terminal (SMT). This feature allows the SRT to communicate on the bus for one specific address and the SMT to monitor the bus for other specific addresses. Configuration as both SMT and SRT precludes the SμMMIT XT from monitoring its own remote terminal address.

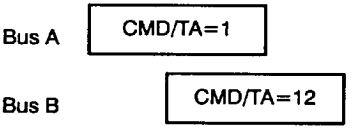
When the SμMMIT XT is configured as both SRT and SMT, the SRT has priority over the SMT. For example, commands to the SRT will always take priority over commands for the SMT. The examples below describe what happens if the SRT is defined as terminal address 1 and the SMT is to monitor terminal address 12.

Example 1:



In this example, the SMT will decode the first command on bus A, realize the message is for terminal address 12, and start monitoring the message. However, as soon as the SRT realizes the second command on bus B is to terminal address 1, the SRT will take priority and begin SRT message processing.

Example 2:



In example 2, the SRT will decode the first command on bus A, realize the message is for terminal address 1, and start message processing. As the message on bus B is received, the SμMMIT XT will realize it is to terminal address 12, but since the SRT has priority the SMT will not switch to the monitor mode.

The above examples also apply to an RT-RT message. For example, if the first command in an RT-RT transfer matches the terminal address of the SRT, the entire message will be stored (Message 1). However, if the first command in an RT-RT transfer matches the terminal address of the SMT and the second command matches the terminal address of the SRT, the SRT will take priority and only the SRT message is stored (Message 2). Below is an RT-RT message example.

Message 1	CMD/TA=1	CMD/TA=12
Message 2	CMD/TA=12	CMD/TA=1

4.7 MIL-STD-1553A Operation

As discussed in section 2.9, the SμMMIT XT may be configured to meet the MIL-STD-1553A protocol.

Table 6. MIL-STD-1553A Operation

A/$\overline{B}$ STD (pin)	$\overline{LOCK}$ (pin)	RESULT
0	1	1553B response, 1553B standard
0	0	1553B response, 1553B standard
1	1	1553A response, 1553A standard
1	0	1553A response, 1553A standard

When configured as a MIL-STD-1553A monitor, the SμMMIT XT will operate as follows:

- looks for the RT response within 11μs;
- ignores the T/$\overline{R}$ bit for all mode codes;
- defines all mode codes without data;
- defines subaddress 00000 as a mode code.

5.0 Interrupt Architecture

The SμMMIT XT's interrupt architecture involves three internal registers, an Interrupt Log List, two interrupt outputs, and two interrupt acknowledges. The three internal registers include a Pending Interrupt Register, Interrupt Mask Register, and Interrupt Log List Register. The Pending Interrupt Register contains information that identifies the events generating the interrupts. The Interrupt Mask Register allows the user to mask or disable the generation of interrupts. The Interrupt Log List Register contains the base address of a 32-word interrupt ring buffer. Two interrupt outputs signal the occurrence of an interrupt event. The interrupt architecture differentiates interrupts as either a hardware interrupt ($\overline{YF\_INT}$) or message interrupt ($\overline{MSG\_INT}$). The user programs the interrupt outputs as either pulsed outputs or level outputs depending on system requirements.

Assertion of the $\overline{YF\_INT}$ interrupt signals a hardware failure condition. Failures include DMA time-out, wrap-around self-test, terminal address parity, or built-in test (BIT). $\overline{YF\_INT}$ failures are reflected in the four most significant bits of the Pending Interrupt Register. The $\overline{YF\_INT}$ output asserts on the occurrence of a failure.

Assertion of the $\overline{MSG\_INT}$ interrupt, signals a message related event has occurred. $\overline{MSG\_INT}$ events are reflected in the 12 least significant bits of the Pending Interrupt Register. The $\overline{MSG\_INT}$ asserts after message processing is complete.

The interrupt architecture allows for the entry of 16 interrupts into a 32-word ring buffer (see figure 14). The SμMMIT XT automatically handles the interrupt logging overhead. Each interrupt generates two words of information to help the host or subsystem perform interrupt processing. The Interrupt Identification Word (IIW) identifies the type(s) of interrupt that occurred. The Interrupt Address Word (IAW) identifies the interrupt source (e.g., subaddress or command block) via a 16-bit address. The SμMMIT XT's interrupt outputs are user programmable. The user can select either pulsed interrupt outputs or level sensitive outputs. In the level mode of operation, assertion of either input (i.e., $\overline{YF\_ACK}$ or $\overline{MSG\_ACK}$) negates the respective interrupt output (i.e., $\overline{YF\_INT}$ or $\overline{MSG\_INT}$). The mode of operation is selected via mode select inputs MSEL(5:0). The state of MSEL(4) selects the mode of operation, Table 7 reviews operation.

All Modes

Table 7. MSEL(4) Operation

MSEL(4)	$\overline{\text{YF\_INT}}$ / $\overline{\text{MSG\_INT}}$	$\overline{\text{YF\_ACK}}$ / $\overline{\text{MSG\_ACK}}$
0	Pulse Output	Tied High
1	Level Output	Active Low

5.1 Interrupt Identification Word (IIW)
The Interrupt Identification Word (IIW) is a 16-bit word identifying the interrupt type. The format is similar to the Pending Interrupt Register. The host or subsystem reads the IIW to determine which interrupt event occurred.

5.2 Interrupt Address Word (IAW)
The Interrupt Address Word (IAW) is a 16-bit word that identifies the interrupt source. Depending on the mode of operation (i.e., SRT, SBC, or SMT), the IAW has different meanings. In the SRT mode of operation, the IAW identifies the subaddress or mode code descriptor that generated the interrupt. For the SBC mode of operation, the IAW points to the command block addressed when the interrupt occurred. In the SMT mode of operation, the IAW marks the monitor counter count when the interrupt occurred. The host uses the IAW with the Initial Monitor Command Block Pointer Register to determine the monitor command block that generates the interrupt.

When the SMT is operating concurrently with the SRT, the host must determine if the IAW contains information for the SRT or SMT. The determination is made by comparing the contents of the IAW base address with the descriptor base address. If a match occurs, then the IAW contains a subaddress or mode code identifier. If no match occurs, the IAW contains monitor counter information.

5.3 Interrupt Log List Address
The interrupt log list resides in a 32-word ring buffer. The host or subsystem defines the location buffer, within a 32K x 16 memory space, via the Interrupt Log List Register (Register 5). Restrict the ring buffer address to a 32-word boundary.

During initialization the host or subsystem writes a value to the Interrupt Log List Pointer Register. Initialize the least significant five-bits to a logic zero. The most significant 11 bits determine the base address of the buffer. The SμMMIT XT increments the ring buffer pointer on the occurrence of the first interrupt, storing the IIW and IAW at locations 00000 and 00001 respectively. The SμMMIT XT logs ensuing interrupts sequentially into the ring buffer until interrupt number 16 occurs. The SμMMIT XT enters interrupt 16's IIW in buffer location 11110 and the IAW at location 11111.

The SμMMIT XT increments the ring buffer pointer as interrupts occur. The least significant five-bits of the Interrupt Log List Pointer Register reflect the ring buffer pointer value. Figure 14 shows the ring buffer architecture.

The host or subsystem reads ring buffer pointer value to determine the number of interrupts that have occurred. By extracting the least significant five bits from the Interrupt Log List Register and logical shifting the data once to the right, the host or subsystem determines the number of interrupt events.

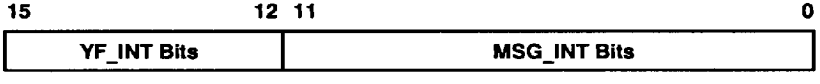


Figure 13. Pending Interrupt and Mask Register

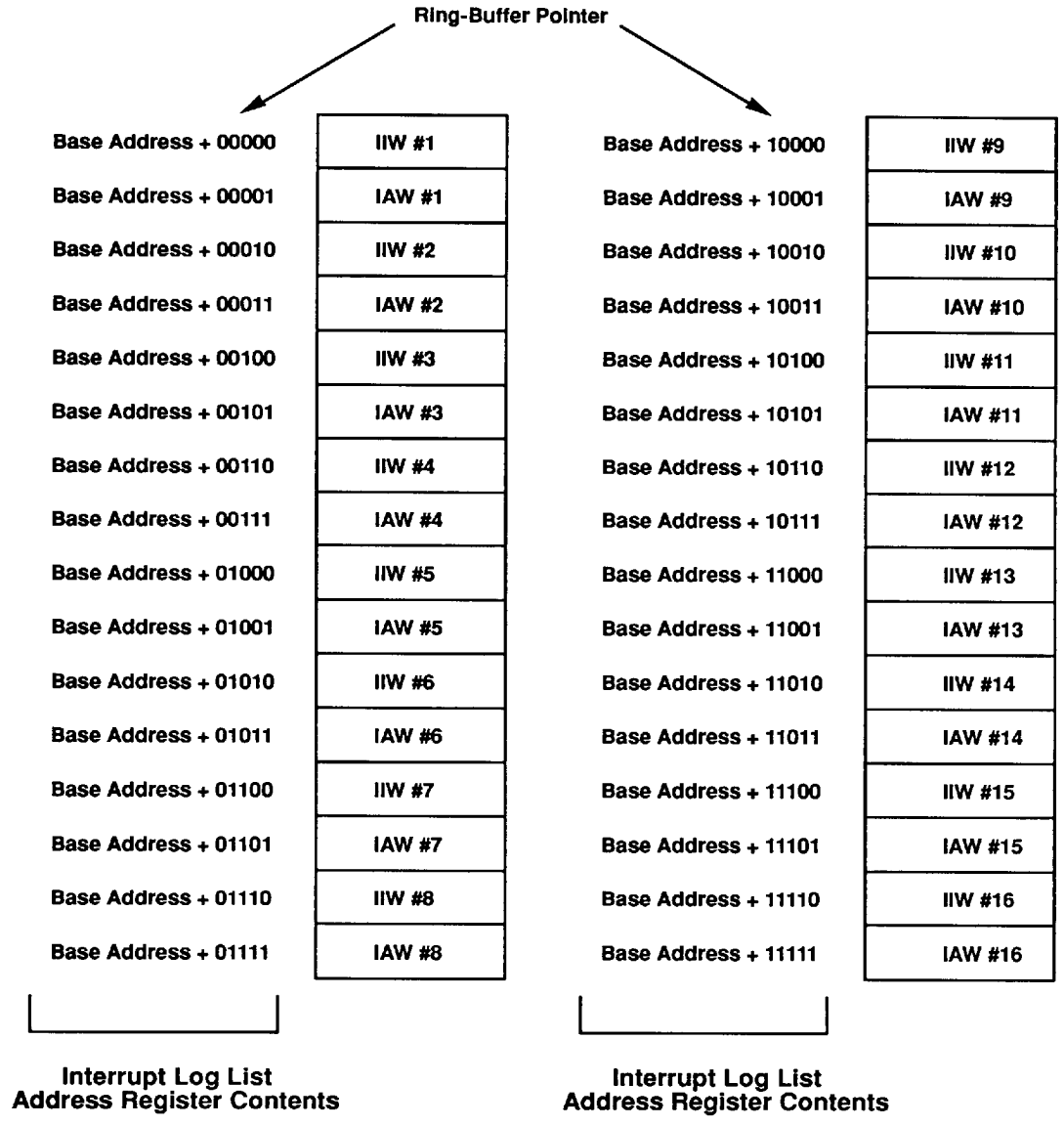


Figure 14. Interrupt Ring Buffer

Interrupt Information Word

Bit Number	Mnemonic	Description
15-12	N/A	Not Applicable.
11	MERR	Message Error Interrupt (All modes).
10	SUBAD	Subaddress Accessed Interrupt (SRT).
9	BDRCV	Broadcast Command Received Interrupt (SRT).
8	IXEQ0	Index Equal Zero Interrupt (SRT).
7	ILCMD	Illegal Command Interrupt (SRT).
6	N/A	Not Applicable.
5	EOL	End of List (SBC).
4	ILLCMD	Illogical Command (SBC).
3	ILLOP	Illogical Opcode (SBC).
2	RTF	Retry Fail (SBC).
1	CBA	Command Block Accessed (SBC).
0	MBC	Monitor Block Count Equal Zero (SMT).

6.0 AUTO-INITIALIZATION

The SμMMIT XT auto-initialization feature allows autonomous operation. The SμMMIT XT will automatically configure itself for operation from nonvolatile memory (PROM). The configuration sequence begins after the negation of input pin $\overline{\text{MRST}}$, if $\overline{\text{AUTOEN}}$ is enabled. For each mode of operation, the auto-initialization function is different. The following section outlines the auto-initialization feature for each mode of operation.

6.1 SRT Auto-Initialization

During auto-initialization, the SμMMIT XT loads all internal registers and transfers the descriptor space into RAM. Initialize registers not used during SRT operation to 0000 (hex). The SRT must have 32 memory locations allocated for register data.

Following register initialization, the SμMMIT XT reads the descriptor from ROM and enters the descriptor into RAM. The starting address for the descriptor is read from the Descriptor Pointer Register. The SμMMIT XT internally generates all address information required for auto-initialization.

The SμMMIT XT requires 544 consecutive ROM locations for initialization. The 544 memory locations include: 32 for internal register information, 256 for subaddress descriptor information, and 256 for mode code descriptor information. Unused descriptor blocks should be initialized to four words of 0000 (hex).

The SRT accesses 544 consecutive memory locations in 32-word blocks. Once access is granted, the SRT reads words from ROM, then transfers the information into RAM. The SRT does not respond to MIL-STD-1553B commands until initialization is complete, the start execution bit has been set, and the RT parity has been verified. After initialization, the SRT can respond to MIL-STD-1553 commands.

6.2 SMT Auto-Initialization

SMT auto-initialization requires only the loading of internal registers. Registers not used during SMT operation should be initialized to 0000 (hex). The SMT requires allocation of 32 memory locations for register data. The SμMMIT XT internally generates all address information for auto-initialization.

When operating as a concurrent SRT and SMT, the SμMMIT XT loads all internal registers for both SRT and SMT modes of operation. The device then transfers the descriptor from ROM to RAM.

6.3 SBC Auto-Initialization

During auto-initialization the SμMMIT XT loads all internal registers and transfers the command block(s) into RAM. Registers not used during SBC operation should be initialized to 0000 (hex). The SBC requires the allocation of 32 memory locations for register data.

Following register initialization, the SμMMIT XT reads command block(s) information from ROM and enters them into RAM. The starting address for the command block(s) is read from the Command Block Pointer Register. The SμMMIT XT internally generates all address information for auto-initialization.

The SBC continues to read command blocks from ROM until the Command Block Initialization Count Register decrements to zero.

6.4 Auto-Initialization Hardware

An external auto-initialization bus allows configuration of SμMMIT XT without host intervention. Auto-initialization is ideal for low cost remote sensing applications where a host microprocessor or microcontroller is not required.

To enable the auto-initialization function, assert the $\overline{\text{AUTOEN}}$ pin prior to the rising edge of $\overline{\text{MRST}}$. The assertion of $\overline{\text{MRST}}$ signals the beginning of the auto-initialization sequence. The SμMMIT XT enables the boot memory by asserting the $\overline{\text{ECS}}$ output. The SμMMIT XT accesses up to 8K x 8 words via the auto-initialization bus. Table 8 reviews the memory requirements for SμMMIT XT auto-initialization.

Table 8. Auto-Initialization Memory Requirements

Mode	Memory (x8)
SRT	1088
SRT	64
SBC	32 + [N x (8)] [1]

Note:
1. N equals the number of commands.

To interface to slower non-volatile memory the auto-initialization read cycle period is programmable. The user can select between zero and seven wait states per read. A wait state is equal to 82ns. The user programs the read cycle duration via inputs EC(2:0). The SμMMIT XT latches inputs EC(2:0) on the rising edge of $\overline{\text{MRST}}$. Table 9 reviews the possible combinations of wait-states. Figure 15b shows typical auto-initialization read cycles along with a system configuration. Following completion of an auto-initialization sequence the SμMMIT XT asserts the $\overline{\text{READY}}$ output.

Table 9. Programmable Wait-State

$EC(2:0)_2$	Number of Wait-States
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

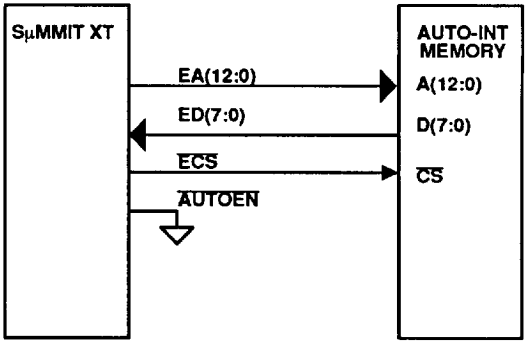
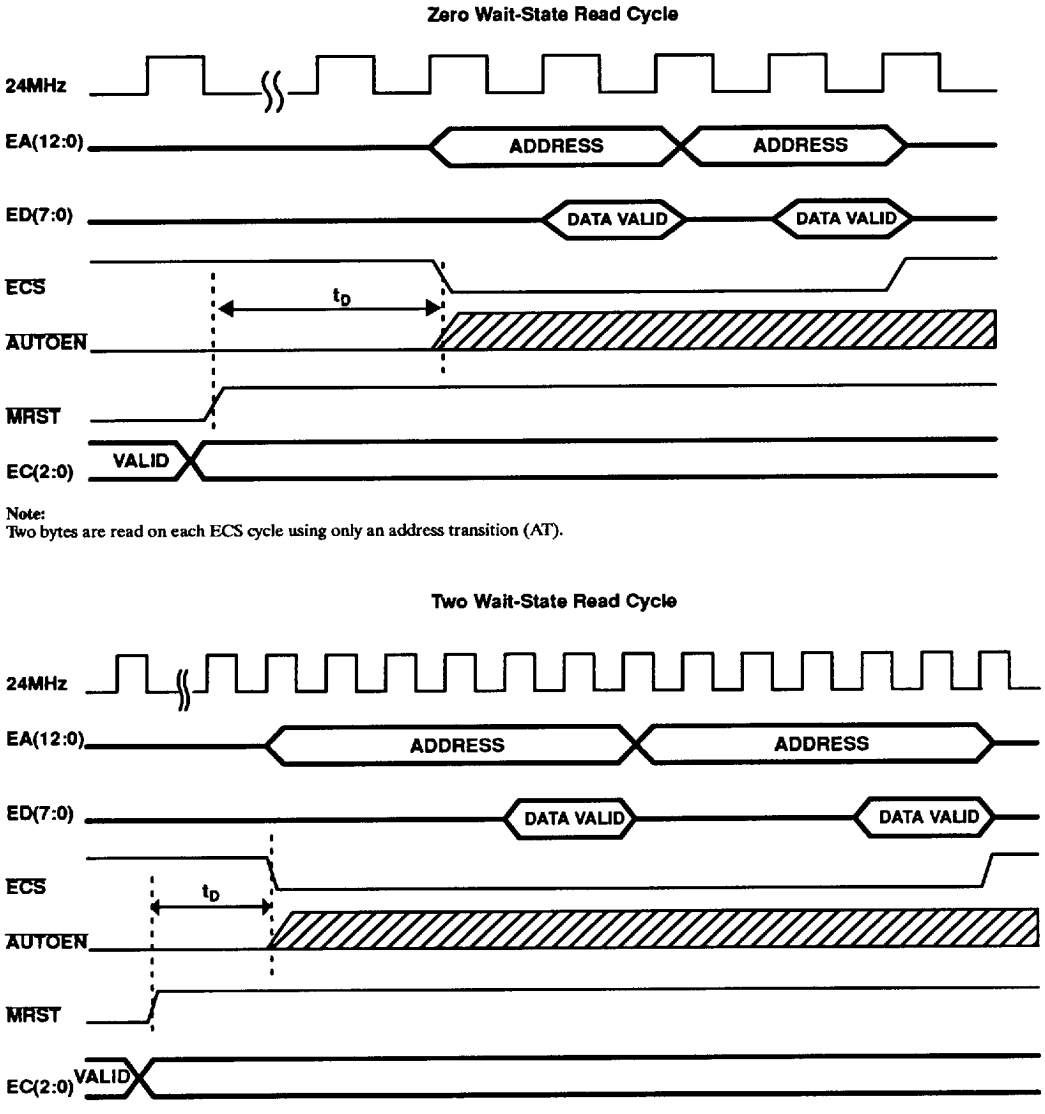


Figure 15a. Auto-Initialization System Configuration

All Modes



Note:
Two bytes are read on each ECS cycle using only an address transition (AT).

Figure 15b. Auto-Initialization Read Cycle

7.0 TESTABILITY

In military systems, design complexity demands some type of testing mechanism to ensure operational reliability. The SμMMIT XT provides two separate testing features: JTAG and Built-In-Test. Each testing feature is described below.

7.1 JTAG

To enhance board testing, the SμMMIT XT supports the following IEEE Standard 1149.1 (JTAG) instructions.

BYPASS	1111
SAMPLE/PRELOAD	0010
EXTEST	0000
INTEST	0001
RUNBIST	0111
IDCODE	0100
INTERNAL-SCAN	0101

IDCODE = 00011100000001010100000000000000

7.2 Internal Built-In-Test (BIT)

The SμMMIT XT provides an internal Built-In-Test (BIT) that may be used at any time to verify functional operation. The BIT is initiated by one of the following four methods listed below. BIT execution takes 1ms.

1. JTAG may initiate BIT using the RUNBIST instruction as defined in the IEEE Standard 1149.1 (JTAG).
2. When configured as an SRT, the SμMMIT XT will perform BIT upon receipt of a MIL-STD-1553B Mode Code (Initiate Self-Test).
3. When configured as an SBC, the SμMMIT XT will perform BIT if the BIT opcode is used in the Command Block.
4. Regardless of the configuration, the SμMMIT XT will perform BIT when instructed to do so by the host processor. To initiate BIT, the host writes a logic one to bit 14 (SBIT) of the Control Register.

7.3 Memory Test

The MMU has a memory test which takes 70ms. The memory test is initiated through the MMU's JTAG port with the instruction 1000 or through method #4 described in section 7.2, item 4. Before initiating memory test reset the SμMMIT XT by asserting $\overline{\text{MRST}}$.

8.0 SYSTEM CONFIGURATION

The SμMMIT XT supplies hardware designers with a flexible interface to meet the needs of state-of-the-art MIL-STD-1553 interfaces. The SμMMIT XT contains internal SRAM and a memory management unit, interfaces to either 8-bit or 16-bit subsystems, supports multiplexed and non-multiplexed interfaces, and has user selectable control signals.

8.1 Memory Map

The SμMMIT XT contains 512Kbits of memory for message storage and system data storage. MSEL(5) determines the organization of the memory as either x16 or x8. When organized x16 (i.e., MSEL(5) = 0) the SμMMIT XT' s internal memory looks like 32K x 16 of SRAM. For x8 applications (MSEL(5) = 1) the SμMMIT XT's internal memory looks like 64K x 8 of SRAM. The host reads or writes SRAM using the timing diagrams shown in figures 16a-d. Table 10 shows the memory organization for either 8-bit or 16-bit operation.

8.2 Internal Registers

The SμMMIT XT contains 32 internal registers that control and report on message activity and operation. The 32 registers are memory mapped into the subsystem memory. Table 10 reviews the registers and identifies the mode of operation they are applicable. The host reads or writes these registers using the timing diagrams shown in figures 16a-d.

All Modes

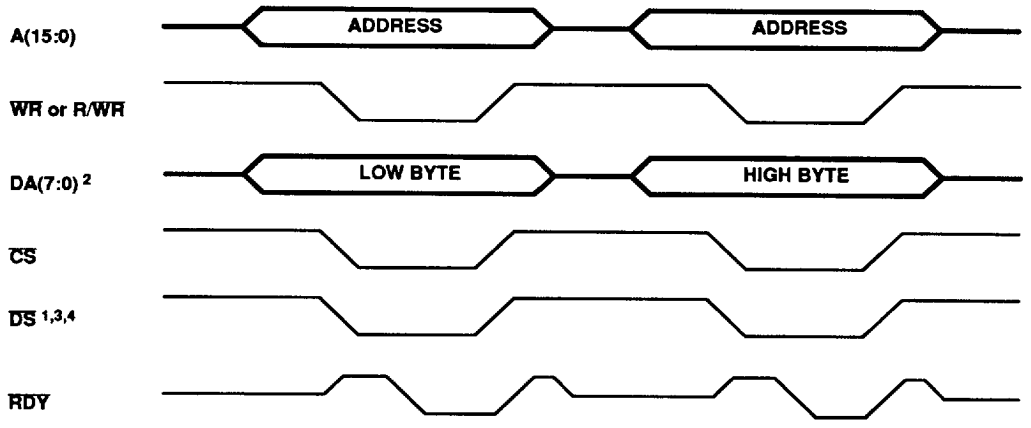
Table 10. Memory Organization

Mode	Memory Organization	Register Location	Memory Range
8-bit	64K x 8	0000 (hex) to 003F (hex)	0040 (hex) to FFFF (hex)
16-bit	32K x 16	0000 (hex) to 001F (hex)	0020 (hex) to 7FFF (hex)

Table 11. Internal Register Utilization

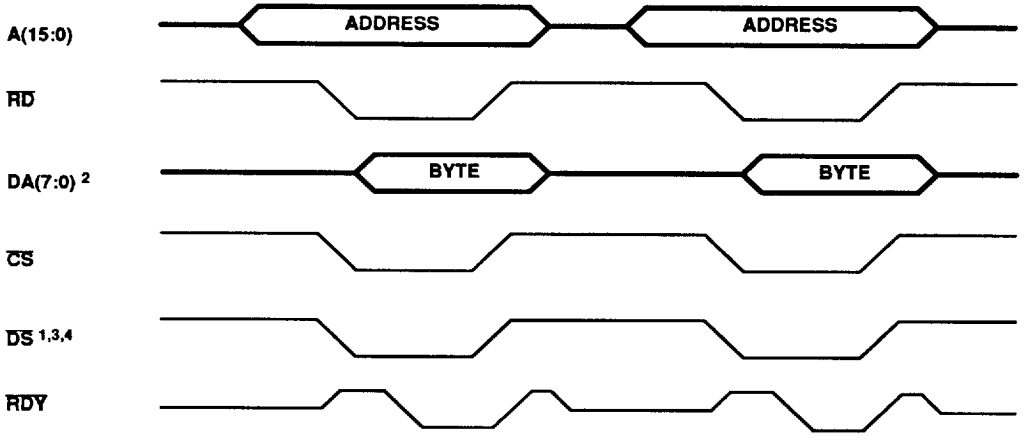
Register Number	Register	SRT	SBC	SMT
0	Control	✓	✓	✓
1	Operational Status	✓	✓	✓
2	Current Command	✓	✓	✓
3	Interrupt Mask	✓	✓	✓
4	Pending Interrupt	✓	✓	✓
5	Interrupt Log List	✓	✓	✓
6	BIT Word	✓	✓	✓
7	Time Tag (SRT and SMT) Miner Frame Timer (SBC)	✓	✓	✓
8	SRT Descriptor Pointer (SRT) Command Block Pointer (SBC)	✓	✓	
9	1553 Status Word Bits			
A	Command Block Initialization Count (BC)		✓	
B	Initial Monitor Command Block Pointer			✓
C	Initial Monitor Data Pointer			✓
D	Monitor Block Count			✓
E	Monitor Filter			✓
F	Monitor Filter			✓
10 to 1F	Illegalization	✓ (16)		
	Total	27	10	13

Non-Multiplexed Memory/Register Write Access (8-bit Mode)



Notes:
1. DS asserts to signal that data is valid on the bus.
2. Tie DA(15:8) to V_{DD} via a 10K resistor.
3. ALE must be tied high.
4. Logical "and" of CS, DS, WR starts memory cycle.

Non-Multiplexed Memory/Register Read Access (8-bit Mode)

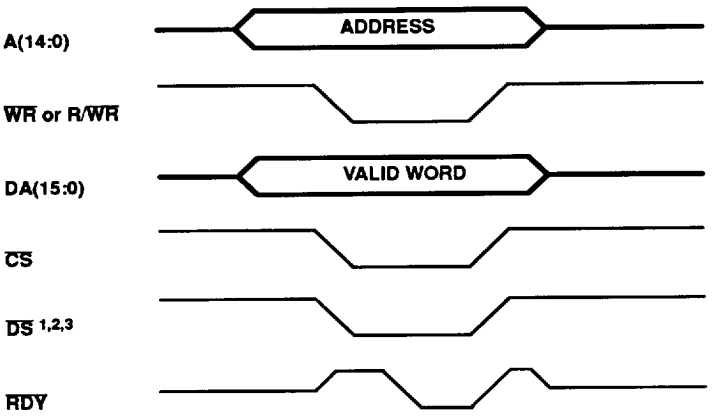


Notes:
1. DS asserts to signal the SμMMIT XT to place data on the bus.
2. Tie DA(15:8) to V_{DD} via a 10K resistor.
3. ALE must be tied high.
4 Logical "and" of CS, DS, RD starts memory cycle.

Figure 16a. 8-bit Memory and Register Access

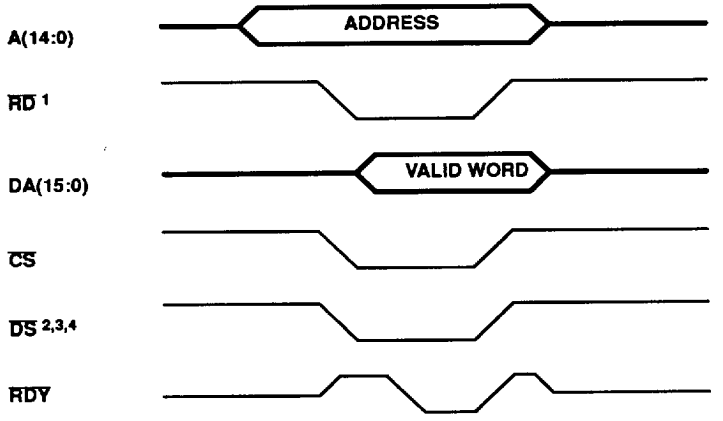
All Modes

Non-Multiplexed Memory/Register Write Access (16-bit Mode)



Notes:
1. DS asserts to signal that data is valid on the bus.
2. ALE must be tied high.
3. Logical "and" of CS, DS, WR starts memory cycle.

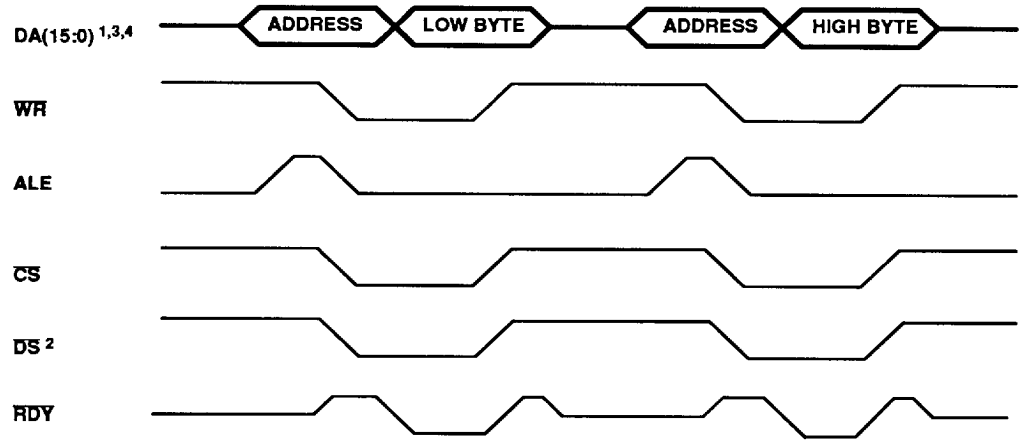
Non-Multiplexed Memory/Register Read Access (16-bit Mode)



Notes:
1. When using R/WR as an input signal tie RD to a logical one. During the read cycle R/WR remains a logic 1.
2. DS asserts to signal the SμMMIT XT to place data on the bus.
3. ALE must be tied high.
4. Logical "and" of CS, DS, RD starts memory cycle.

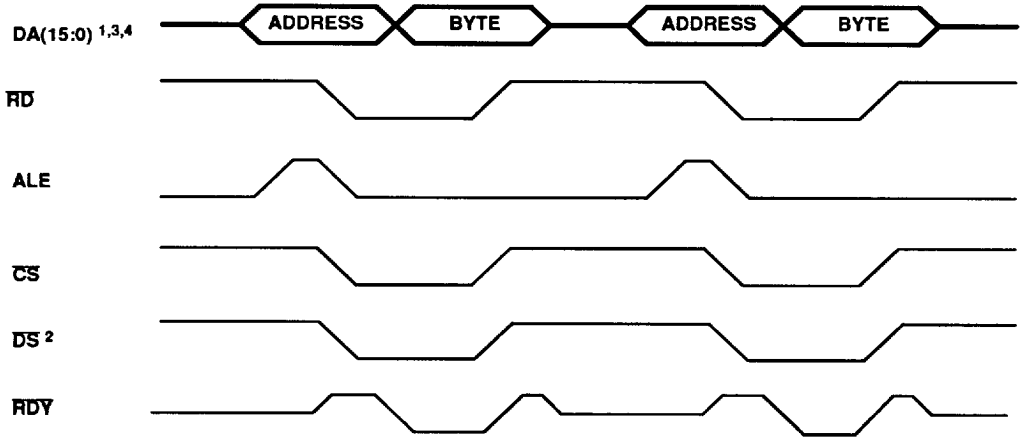
Figure 16b. 16-bit Memory and Register Access

Multiplexed Memory/Register Write Access (8-bit Mode)



Notes:
1. For multiplexed address and data interfaces ALE latches the address into the SμMMIT XT. Data is applied to inputs DA(7:0), tie A(15:0) to either a logical one or zero.
2. $\overline{DS}$ asserts to signal that data is valid on the bus.
3. Logical "and" of $\overline{CS}$, $\overline{DS}$, $\overline{WR}$ starts memory cycle.
4. Tie DA(15:8) to V_{SS} via a 10K resistor.

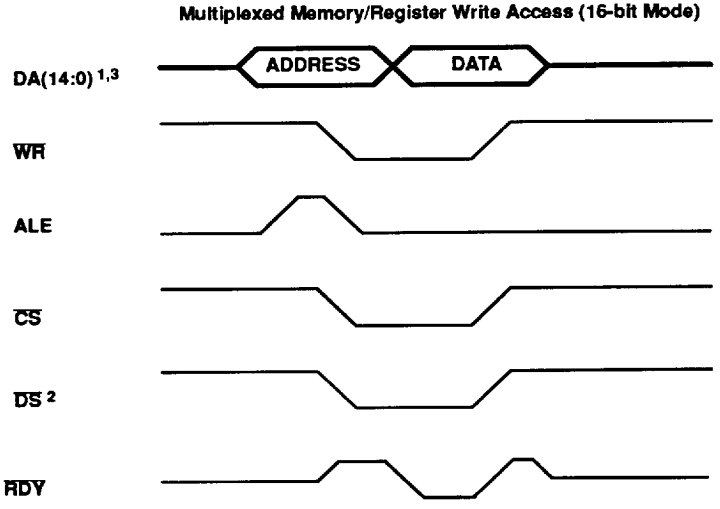
Multiplexed Memory/Register Read Access (8-bit Mode)



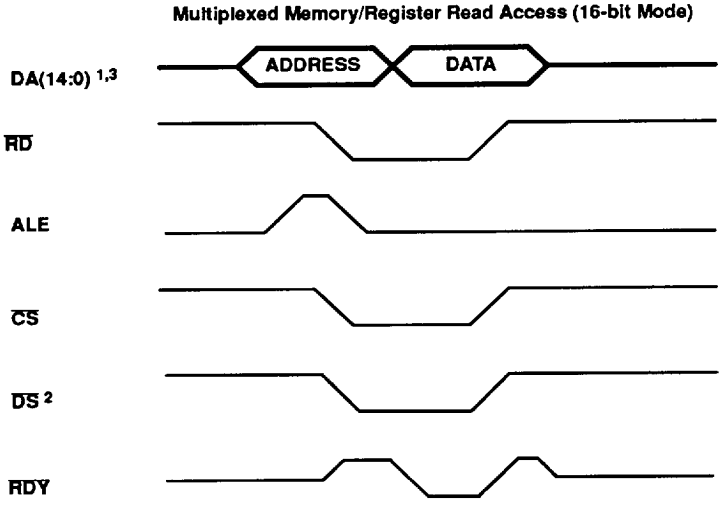
Notes:
1. For multiplexed address and data interfaces ALE latches the address into the SμMMIT XT. Data is read from outputs DA(7:0), tie A(15:0) to either a logical one or zero.
2. $\overline{DS}$ asserts to signal the SμMMIT XT to place data on the bus.
3. Logical "and" of $\overline{CS}$, $\overline{DS}$, $\overline{RD}$ starts memory cycle.
4. Tie DA(15:8) to V_{SS} via a 10K resistor.

Figure 16c. Multiplexed 8-bit Memory and Register Access

All Modes



Notes:
1. For multiplexed address and data interfaces ALE latches the address into the SμMMIT XT. Data is applied to inputs DA(15:0), tie A(15:0) to either a logical one or zero.
2. $\overline{DS}$ asserts to signal that data is valid on the bus.
3. Logical "and" of $\overline{CS}$, $\overline{DS}$, $\overline{WR}$ starts memory cycle.



Notes:
1. For multiplexed address and data interfaces ALE latches the address into the SμMMIT XT. Data is read from outputs DA(15:0), tie A(15:0) to either a logical one or zero.
2. $\overline{DS}$ asserts to signal the SμMMIT XT to place data on the bus.
3. Logical "and" of $\overline{CS}$, $\overline{DS}$, $\overline{RD}$ starts memory cycle.

Figure 16d. Multiplexed 16-bit Memory and Register Access

8.3 Hardware Interface

The SμMMIT XT offers hardware designers a flexible interface to commonly found embedded computers. The hardware designer selects control signals, bus widths, and bus functionality (i.e., non-multiplexed versus multiplexed) to meet their interface requirements. Table 12 reviews how the user selects the SμMMIT XT's operation that best meets their interface requirements.

Figures 17a, 17b, 18a, and 18b show typical system interfaces and use of the mode select inputs to configure the SμMMIT XT to interface to various embedded computers.

Table 12. User-Selectable Control Signals

Function	Input Pin	Logic 1	Logic 0
Control Signal Select	MSEL(2)	R/$\overline{WR}$, $\overline{CS}$, $\overline{DS}$, $\overline{RDY}$	$\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RDY}$, $\overline{DS}$
Bus Functionality Select	MSEL(3)	Non-Multiplexed Address and Data	Multiplexed Address and Data, ALE
Interrupt Select	MSEL(4)	Level ($\overline{YF\_INT}$, $\overline{MSG\_INT}$, $\overline{YF\_ACK}$, and $\overline{MSG\_ACK}$)	Pulse ($\overline{YF\_INT}$ and $\overline{MSG\_INT}$)
Bus Width Select	MSEL(5)	8-bit	16-bit

All Modes

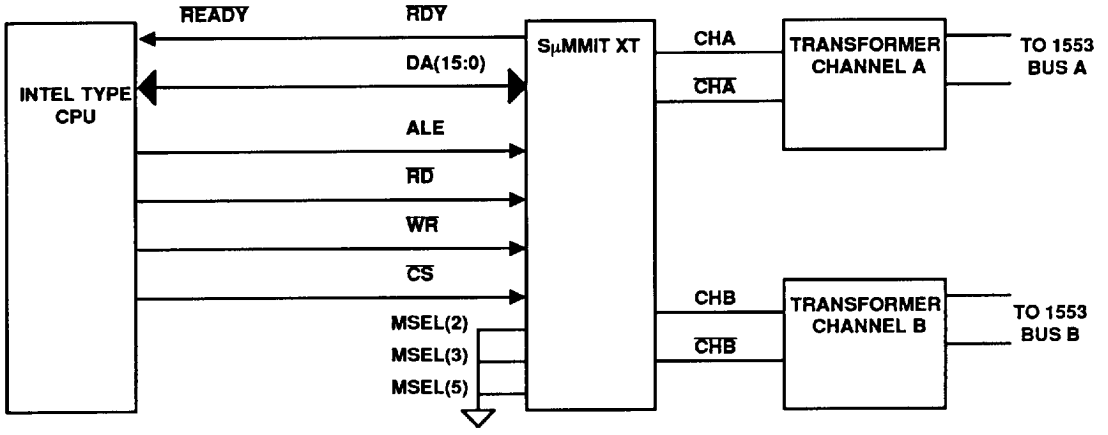


Figure 17a. 16-bit Interface (Intel Type)

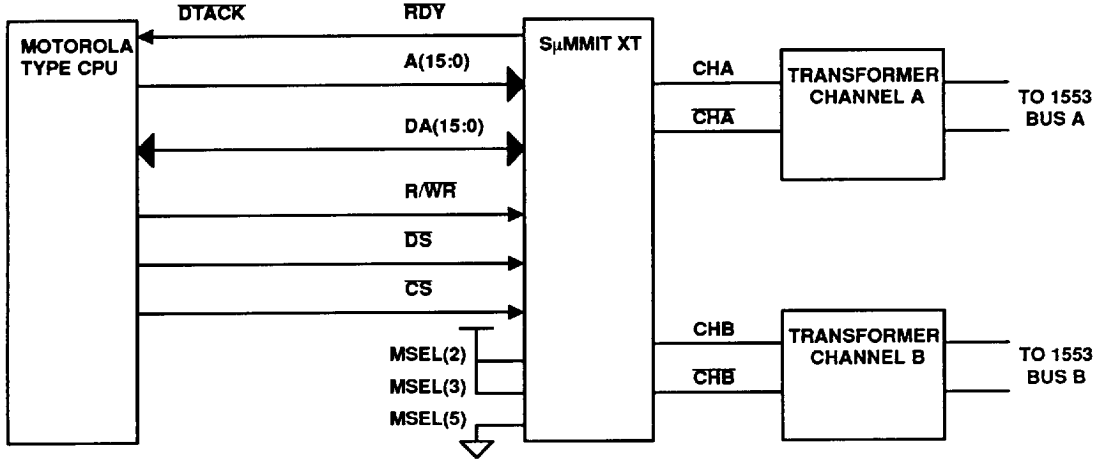


Figure 17b. 16-bit Interface (Motorola Type)

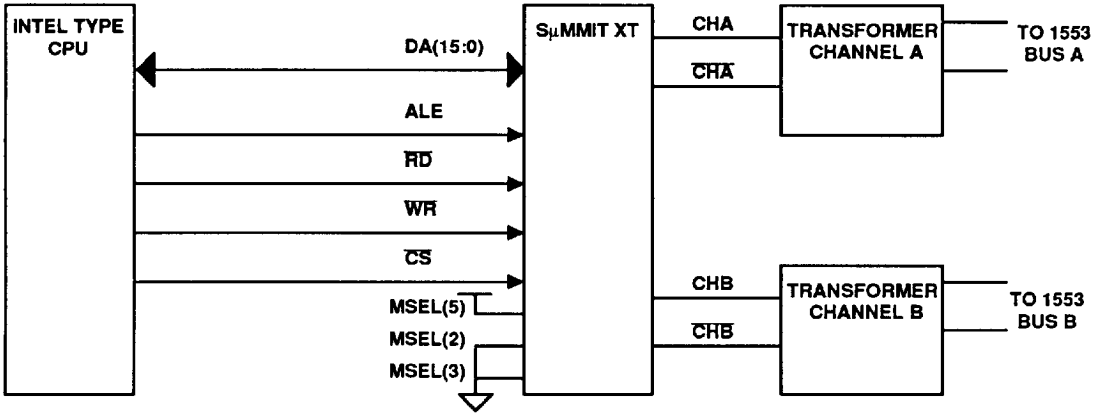


Figure 18a. 8-bit Interface (Intel Type)

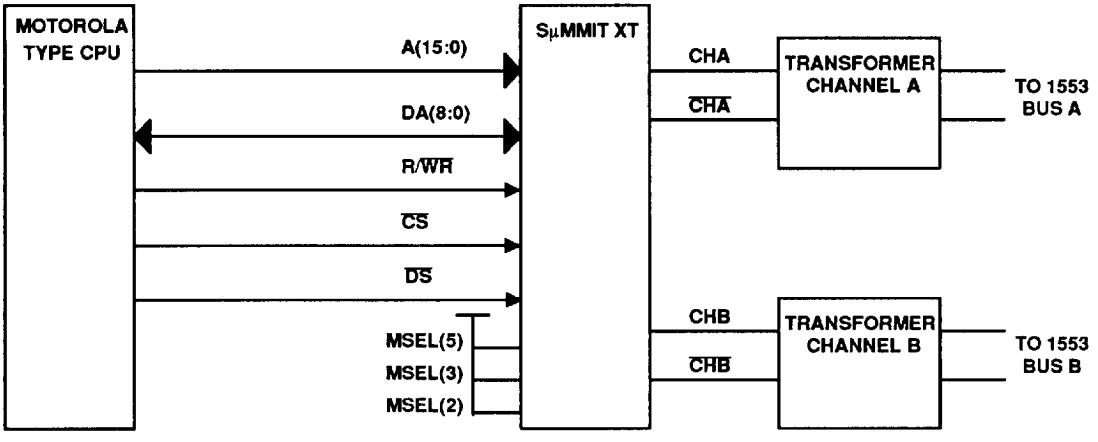


Figure 18b. 8-bit Interface (Motorola Type)

9.0 Data Bus Interface

The SμMMIT XT's Manchester encoder/decoder interfaces directly to the MIL-STD-1553 bus via transformers, using CHA-$\overline{\text{CHA}}$ and CHB-$\overline{\text{CHB}}$. The designer can connect the SμMMIT XT to the data bus via a short-stub (direct-coupling) connection or a long-stub (transformer-coupling) connection. Use a short-stub connection when the distance from the isolation transformer to the data bus does not exceed a one-foot maximum. Use a long-stub connection when the distance from the isolation transformer exceeds the one-foot maximum and is less than twenty feet. Figures 19a, 19b, and 19c show various examples of bus coupling configurations. The SμMMIT XT is designed to function with MIL-STD-1553A and 1553B compatible transformers.

9.1 Transmitter

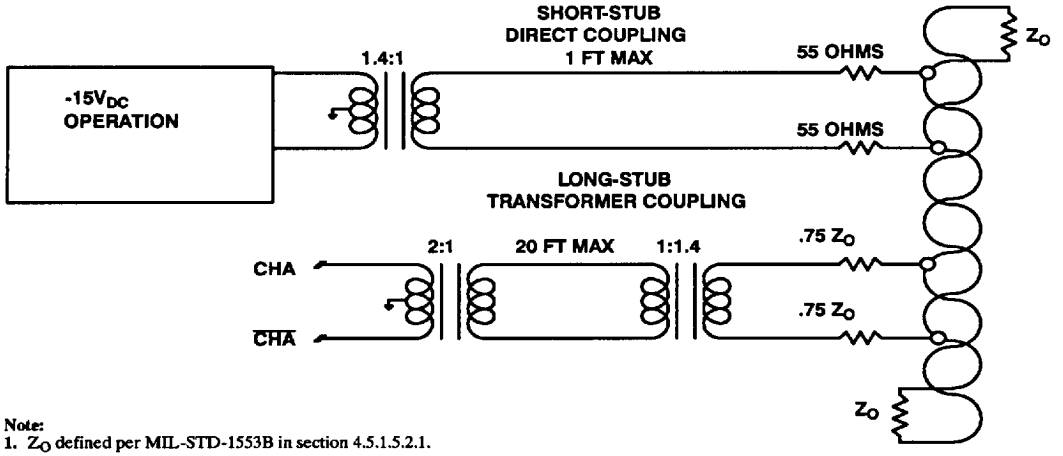
The transmitter section accepts Manchester II biphase TTL data and converts this data into differential phase-modulated current drive. Transmitter current drivers are coupled to a MIL-STD-1553 data bus via a transformer driven from the CHA (CHB) and $\overline{\text{CHA}}$ ($\overline{\text{CHB}}$) terminals. The SμMMIT XT internally generates a signal to the transceiver for the MIL-STD-1553 fail-safe timer requirement.

9.2 Receiver

The receiver section accepts biphase differential data from a MIL-STD-1553 data bus at its CHA (CHB) and $\overline{\text{CHA}}$ ($\overline{\text{CHB}}$) inputs. The receiver converts input data to biphase Manchester II TTL format at internal RXOUT and $\overline{\text{RXOUT}}$ terminals. The internal outputs RXOUT and $\overline{\text{RXOUT}}$ represent positive and negative excursions (respectively) of the inputs CHA (CHB) and $\overline{\text{CHA}}$ ($\overline{\text{CHB}}$).

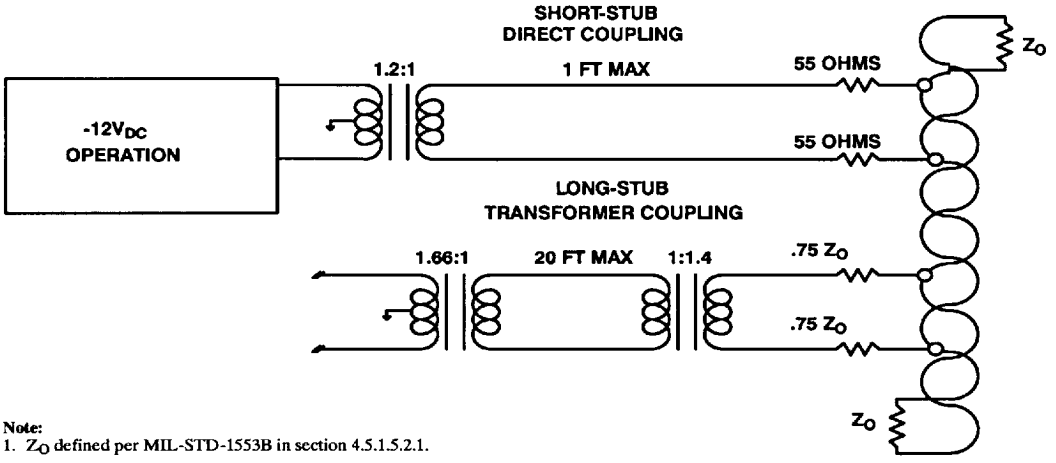
9.3 Recommended Thermal Protection

All packages should mount to or contact a heat removal rail located in the printed circuit board. To insure proper heat transfer between the package and the heat removal rail, use a thermally-conductive material between the package and the heat removal rail. Use a material such as Mereco XLN-589 or equivalent to insure heat transfer between the package and heat removal rail.



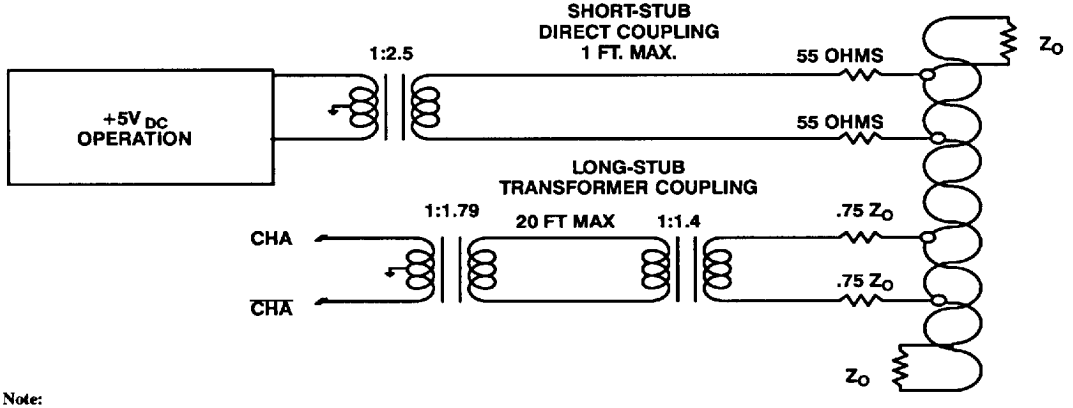
Note:
1. Z_O defined per MIL-STD-1553B in section 4.5.1.5.2.1.

Figure 19a. XT15 Bus Coupling Configuration



Note:
1. Z_O defined per MIL-STD-1553B in section 4.5.1.5.2.1.

Figure 19b. XT12 Bus Coupling Configuration



Note:
1. Z_O defined per MIL-STD-1553B in section 4.5.1.5.2.1.

Figure 19c. XT5 Bus Coupling Configuration

All Modes

Table 13. Transformer Requirements Versus Power Supplies

COUPLING TECHNIQUE	-12V$_{DC}$	-15V$_{DC}$	+5V$_{DC}$
DIRECT-COUPLED: Isolation	1.2:1	1.4:1	1:2.5
TRANSFORMER-COUPLED: Isolation Transformer Ratio	1.66:1	2:1	1:1.79
Coupling Transformer Ratio	1:1.4	1:1.4	1:1.4

10.0 PIN IDENTIFICATION AND DESCRIPTION

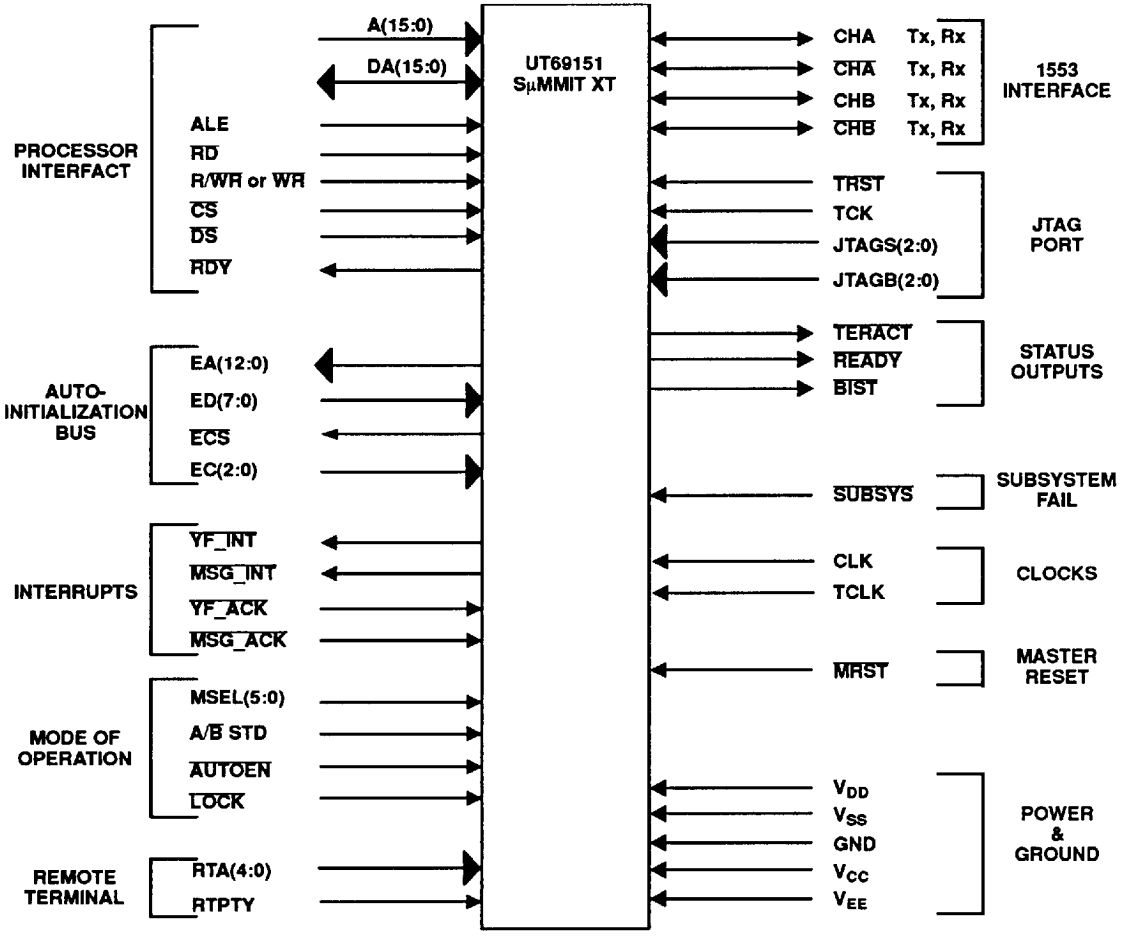


Figure 20. SμMMIT XT Functional Pin Diagram

10.1 Functional Description

Legend for fields:
TO = TTL output
TTB = Three-state TTL bidirectional
CI = CMOS input
TUI = TTL input (internally pulled high)
AH = Active high
AL = Active low
TI = TTL input
TTO = Three-state TTL output
PGA = Pingrid Array
FP = Flatpack
DIO = Differential input/output

10.1.1 Data Bus DA (15:0)

Bit Number	Type	Active	Pin Number		Description
			FP	PGA	
15	TTB	--	TBD	N11	Bit 15 (MSB) of the bidirectional Data bus.
14	TTB	--	TBD	L10	Bit 14 of the bidirectional Data bus.
13	TTB	--	TBD	M11	Bit 13 of the bidirectional Data bus.
12	TTB	--	TBD	L11	Bit 12 of the bidirectional Data bus.
11	TTB	--	TBD	N12	Bit 11 of the bidirectional Data bus.
10	TTB	--	TBD	M12	Bit 10 of the bidirectional Data bus.
9	TTB	--	TBD	L12	Bit 9 of the bidirectional Data bus.
8	TTB	--	TBD	L13	Bit 8 of the bidirectional Data bus.
7	TTB	--	TBD	M13	Bit 7 of the bidirectional Data bus.
6	TTB	--	TBD	L14	Bit 6 of the bidirectional Data bus.
5	TTB	--	TBD	K11	Bit 5 of the bidirectional Data bus.
4	TTB	--	TBD	K13	Bit 4 of the bidirectional Data bus.
3	TTB	--	TBD	K12	Bit 3 of the bidirectional Data bus.
2	TTB	--	TBD	J11	Bit 2 of the bidirectional Data bus.
1	TTB	--	TBD	J12	Bit 1 of the bidirectional Data bus.
0	TTB	--	TBD	J13	Bit 0 (LSB) of the bidirectional Data bus.

All Modes

10.1.2 Address Bus A(15:0)

Bit Number	Type	Active	Pin Number FP	Pin Number PGA	Description
15	TI	--	TBD	J14	Bit 15 (MSB) of the Address bus.
14	TI	--	TBD	H11	Bit 14 of the Address bus.
13	TI	--	TBD	H12	Bit 13 of the Address bus.
12	TI	--	TBD	H13	Bit 12 of the Address bus.
11	TI	--	TBD	G11	Bit 11 of the Address bus.
10	TI	--	TBD	G12	Bit 10 of the Address bus.
9	TI	--	TBD	G13	Bit 9 of the Address bus.
8	TI	--	TBD	G14	Bit 8 of the Address bus.
7	TI	--	TBD	F11	Bit 7 of the Address bus.
6	TI	--	TBD	F12	Bit 6 of the Address bus.
5	TI	--	TBD	F13	Bit 5 of the Address bus.
4	TI	--	TBD	D13	Bit 4 of the Address bus.
3	TI	--	TBD	E13	Bit 3 of the Address bus.
2	TI	--	TBD	C13	Bit 2 of the Address bus.
1	TI	--	TBD	E14	Bit 1 of the Address bus.
0	TI	--	TBD	C14	Bit 0 (LSB) of the Address bus.

10.1.3 Auto-initialization Address Bus EA(12:0)

Bit Number	Type	Active	Pin Number FP	Pin Number PGA	Description
12	TO	--	TBD	F9	Bit 12 (MSB) of the auto-init Address bus.
11	TO	--	TBD	F10	Bit 11 of the auto-init Address bus.
10	TO	--	TBD	G10	Bit 10 of the auto-init Address bus.
9	TO	--	TBD	C11	Bit 9 of the auto-init Address bus.
8	TO	--	TBD	G9	Bit 8 of the auto-init Address bus.
7	TO	--	TBD	E11	Bit 7 of the auto-init Address bus.
6	TO	--	TBD	E10	Bit 6 of the auto-init Address bus.
5	TO	--	TBD	E9	Bit 5 of the auto-init Address bus.
4	TO	--	TBD	G8	Bit 4 of the auto-init Address bus.
3	TO	--	TBD	H8	Bit 3 of the auto-init Address bus.
2	TO	--	TBD	J7	Bit 2 of the auto-init Address bus.
1	TO	--	TBD	J9	Bit 1 of the auto-init Address bus.
0	TO	--	TBD	J10	Bit 0 (LSB) of the auto-init Address bus.

10.1.4 Auto-initialization Address Bus ED(7:0)

Bit Number	Type	Active	Pin Number		Description
			FP	PGA	
7	TUI	--	TBD	K10	Bit 7 (MSB) of the auto-init data.
6	TUI	--	TBD	M7	Bit 6 of the auto-init data.
5	TUI	--	TBD	N3	Bit 5 of the auto-init data.
4	TUI	--	TBD	N8	Bit 4 of the auto-init data.
3	TUI	--	TBD	M8	Bit 3 of the auto-init data.
2	TUI	--	TBD	L8	Bit 2 of the auto-init data.
1	TUI	--	TBD	N9	Bit 1 of the auto-init data.
0	TUI	--	TBD	M9	Bit 0 (LSB) of the data.

10.1.5 Remote Terminal Address Inputs

Name	Type	Active	Pin Number		Description
			FP	PGA	
RTA4	TUI	--	TBD	E2	Remote Terminal Address 4. This is the most significant bit for the RT address.
RTA3	TUI	--	TBD	G3	Remote Terminal Address 3. This is bit 3 of the RT address.
RTA2	TUI	--	TBD	F3	Remote Terminal Address 2. This is bit 2 of the RT address.
RTA1	TUI	--	TBD	G2	Remote Terminal Address 1. This is bit 1 of the RT address.
RTA0	TUI	--	TBD	F2	Remote Terminal Address 0. This input is the least significant bit of the RT address.
RTPTY	TUI	--	TBD	G1	Remote Terminal Parity. This is an odd parity input for the RT address.

10.1.6 JTAG Testability Pins

Name	Type	Active	Pin Number		Description
			FP	PGA	
TDOM	TTO	--	TBD	N10	Memory Management Unit (MMU) TDO. This input performs the operation of Test Data Output as defined in IEEE Standard 1149.1.
TDIM	TUI	--	TBD	L9	MMU TDI. This input performs the operation of Test Data Input as defined in IEEE Standard 1149.1.
TMSM	TUI	--	TBD	M10	MMU TMS. This input performs the operation of Test Mode Select as defined in IEEE Standard 1149.1.
TDOS	TTO	--	TBD	K3	SμMMIT TDO. This input performs the operation of Test Data Output as defined in IEEE Standard 1149.1.
TDIS	TUI	--	TBD	K2	SμMMIT TDI. This input performs the operation of Test Data Input as defined in IEEE Standard 1149.1.
TMSS	TUI	--	TBD	J2	SμMMIT TMS. This input performs the operation of Test Mode Select as defined in IEEE Standard 1149.1.
TCK	TI	--	TBD	L2	TCK. This input performs the operation of Test Clock as defined in IEEE Standard 1149.1.
$\overline{\text{TRST}}$	TUI	AL	TBD	L3	$\overline{\text{TRST}}$. This input provides the RESET to the TAP controller as defined in the IEEE Standard 1149.1.

10.1.7 Biphase Inputs/Outputs

Name	Type	Active	Pin Number		Description
			FP	PGA	
CHA	DIO	--	TBD	B7	Transmit Channel A (True). This is the Manchester-encoded true signal for Channel A.
$\overline{\text{CHA}}$	DIO	--	TBD	A7	Transmit Channel A (Complement). This is the Manchester-encoded complement signal for Channel A.
CHB	DIO	--	TBD	A3	Transmit Channel B (True). This is the Manchester-encoded true signal for Channel B.
$\overline{\text{CHB}}$	DIO	--	TBD	A2	Transmit Channel B (Complement). This is the Manchester-encoded complement signal for Channel B.

10.1.8 Control Signals

Name	Type	Active	Pin Number FP	Pin Number PGA	Description
$\overline{CS}$	TI	AL	TBD	A10	Chip Select. This pin selects the SμMMIT XT's internal memory and registers.
$\overline{DS}$	TI	AL	TBD	A12	Data Strobe. During a write cycle, assert $\overline{DS}$ to indicate that data is valid on the data bus. During a read cycle assert $\overline{DS}$ to signal the SμMMIT XT to drive the data bus.
$\overline{RD}$	TI	AL	TBD	K8	Read Strobe. During a read cycle, assert $\overline{RD}$ to signal the SμMMIT XT to drive the data bus.
R/$\overline{WR}$ or $\overline{WR}$	TI	--	TBD	K7	Read/Write or Write Strobe. During a write cycle assert $\overline{WR}$ to signal the SμMMIT XT that data is valid on the data bus. R/$\overline{WR}$ indicates the direction of data flow with respect to the SμMMIT XT. R/$\overline{WR}$ high indicates the SμMMIT XT will drive the data bus. R/$\overline{WR}$ low indicates an outside source will drive the data bus.
MSEL(5)	TUI	--	TBD	D12	Mode Select 5. A logical zero enables the SμMMIT XT's 16-bit interface. A logical one enables the 8-bit interface. Latched on the rising edge of $\overline{MRST}$.
MSEL(4)	TUI	--	TBD	B13	Mode Select 4. A logical zero enables a pulsed interrupt output. A logical one enables a level interrupt output. Latched on the rising edge of $\overline{MRST}$.
MSEL(3)	TUI	--	TBD	C12	Mode Select 3. A logical zero enables the SμMMIT XT's multiplexed address and data bus interface. A logical one enables the non-multiplexed interface. Latched on the rising edge of $\overline{MRST}$.
MSEL(2)	TUI	--	TBD	A11	Mode Select 2. A logical zero selects control signals $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{DS}$, and $\overline{RDY}$. A logical one selects control signals R/$\overline{WR}$, $\overline{CS}$, $\overline{DS}$, and $\overline{RDY}$. Latched on the rising edge of $\overline{MRST}$.
MSEL(1)	TI	--	TBD	J3	Mode Select 1. This pin in conjunction with MSEL(0) selects the SμMMIT XT's mode of operation. Latched on the rising edge of $\overline{MRST}$. MSEL(1) MSEL(0) Mode of Operation 0 0 Bus Controller 0 1 Remote Terminal 1 0 Monitor Terminal 1 1 Remote Terminal & Monitor
MSEL(0)	TI	--	TBD	J1	Mode Select 0. This pin in conjunction with MSEL(1) selects the SμMMIT XT's mode of operation.
EC(2)	TUI	--	TBD	B10	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.
EC(1)	TUI	--	TBD	D11	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.
EC(0)	TUI	--	TBD	B12	Latched on the rising edge of $\overline{MRST}$ this input sizes the auto-initialization cycle.

All Modes

Name	Type	Active	Pin Number		Description
			FP	PGA	
24 MHz	CI	--	TBD	N7	24 MHz Clock. The 24MHz input clock requires a 50% ±10% duty cycle with an accuracy of ±0.01%.
$\overline{\text{MRST}}$	TUI	AL	TBD	J8	Master Reset. This input pin resets the internal encoder, decoder, all registers, and associated logic.
ALE	TI	AH	TBD	E12	Address Latch Enable. The falling edge of this strobe latches address information into the SμMMIT XT when operating with a multiplexed address and data bus.
TCLK	TI	--	TBD	L7	Timer Clock. The internal timer is a 16-bit counter with a 64μs resolution when using the 24MHz input clock. For applications requiring a different resolution, the user may input a clock from 0 to 60MHz to establish the timer resolution. (Duty cycle equals 50% ±10%).
A/$\overline{\text{B}}$ STD	TUI	--	TBD	H2	A/$\overline{\text{B}}$. Military Standard A or B. This pin defines whether the SμMMIT XT operates per MIL-STD-1553A or MIL-STD-1553B. Input is latched on the rising edge of $\overline{\text{MRST}}$.
$\overline{\text{LOCK}}$	TUI	AL	TBD	H3	Lock. A logical one applied to this pin prevents software from changing the RT address. A/$\overline{\text{B}}$ STD, or mode of operation. Input is latched on the rising edge of $\overline{\text{MRST}}$.
$\overline{\text{AUTOEN}}$	TUI	AL	TBD	M2	Auto Enable. When active this pin enables the SμMMIT XT's auto-initialization function. Input is latched on the rising edge of $\overline{\text{MRST}}$.
$\overline{\text{YF\_ACK}}$	TUI	AL	TBD	H9	You Failed Interrupt Acknowledge. Assertion of this input resets interrupt output $\overline{\text{YF\_INT}}$ when operating in the level mode.
$\overline{\text{MSG\_ACK}}$	TUI	AL	TBD	K9	Message Interrupt Acknowledge. Assertion of this input resets interrupt output $\overline{\text{MSG\_INT}}$ when operating in the level mode.
$\overline{\text{SSYSF}}$	TUI	AL	TBD	D1	Subsystem Fail. Upon assertion, this signal propagates directly to the RT's 1553 Status Word.

10.1.9 Status Signals

Name	Type	Active	Pin Number FP	Pin Number PGA	Description
$\overline{YF\_INT}$	TTO	AL	TBD	M3	You Failed Interrupt. This pin asserts upon the occurrence of interrupt events which are not masked. Either a level output or pulse output.
$\overline{MSG\_INT}$	TTO	AL	TBD	L1	Message Interrupt. This pin asserts upon the occurrence of interrupt events which are not masked. Either a level output or pulse output.
$\overline{READY}$	TO	AL	TBD	D9	$\overline{READY}$. Assertion of this output indicates the SμMMIT XT has completed initialization or BIT, and regular operation may begin.
$\overline{ECS}$	TO	AL	TBD	B11	Chip Select. Auto-initialization device select.
$\overline{RDY}$	TTO	AL	TBD	H10	Access Ready. Assertion of this output indicates that the host can complete the SμMMIT XT access.
$\overline{TERACT}$	TO	AL	TBD	F7	$\overline{TERACT}$. This output indicates that the terminal is actively processing a 1553 command.
$\overline{BIST}$	TO	AL	TBD	D10	Built-In Test. Assertion of this output indicates the SμMMIT XT is performing an internal memory test.

10.1.10 Power/Ground

The following shows the package location of all power and ground pins associated with the SμMMIT XT.

Pin Number	Pin Number FP	Pin Number PGA	Description
V_{DD}	TBD	A8, B3, B14, F1, G7, K1, K14, N2, N13, F14	+5 Volt Logic Power (± 10%)
V_{CC}	TBD	C1, C9, C10, D3, E8, F8	+5 Volt Transceiver Power (+10%,-5%)
V_{EE}	TBD	C2, D2, D7, D8	-12 or -15 Volt Transceiver Power (± 5%)
V_{SS}	TBD	A9, A13, B2, B8, D14, H1, H7, H14, M1, M14	Digital Ground
GND	TBD	B1, B9, C3, C7, C8, E1, E3, E7	Transceiver Ground

All Modes

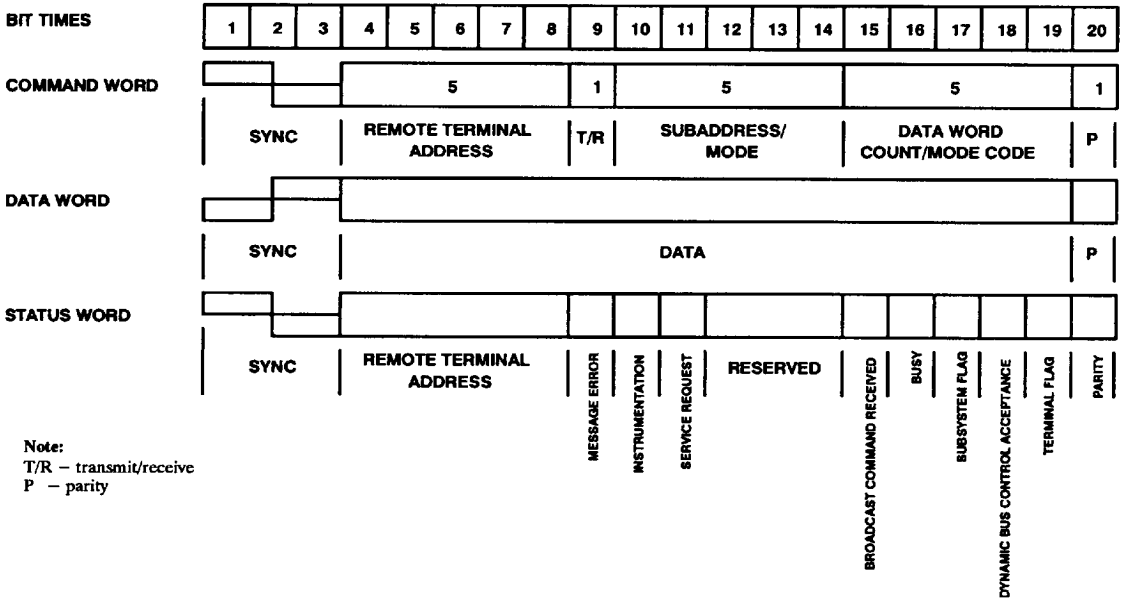


Figure 21. MIL-STD-1553B Word Formats

11.0 Absolute Maximum Ratings [1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMIT	UNIT
V_{DD}	Logic supply voltage	-0.3 to 7.0	V
P_D	Maximum power dissipation	5	W
V_{EE}	Transceiver supply voltage XT15 & XT12	-22	V
V_{CC}	Transceiver supply voltage XT5	-0.3 to 7.0	V
V_{DR}	Input voltage range (receiver) XT15 & XT12 XT5	 42 12	 $V_{P, L-L}$ $V_{P, L-L}$
$V_{I/O}$	Logic voltage on any pin	-.3 to V_{DD} +.3	V
I_{LU}	Latchup immunity	± 150	mA
I_I	Logic input current	± 10	mA
I_O	Peak output current (transmitter) XT15 & XT12 XT5	 190 1000	 mA mA
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Maximum junction temperature XT15 & XT12 XT5	 +150 +135	 °C
T_S	Lead temperature (soldering, 5 seconds)	+300	°C
T_C	Operating temperature case	-55 to + 125	°C
Θ_{JC}	Thermal resistance, junction-to-case [2]	7	°C/W
V_{IC}	Receiver common mode input voltage range XT15 & XT12 XT5	 -11 to +11 -5 to +5	 V V

Note:

1. Stress outside the listed absolute maximum rating may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Mounting per MIL-STD-883, Method 1012.

All Modes

12.0 Recommended Operating Conditions

SYMBOL	PARAMETER	LIMIT	UNIT
V_{CC}	Transceiver supply voltage range	4.75 to +5.25	V
V_{DD}	Logic supply voltage	4.5 to 5.5	V
V_{EE}	Transceiver supply voltage range XT15 & XT12	-12 or -15 (± 5%)	V
V_{DR}	Receiver differential voltage XT15 & XT12 XT5	 40 8.0	V_{P-P}
V_{IN}	Logic DC input voltage	0 to V_{DD}	V
V_{IC}	Receiver common mode input voltage range XT15 & XT12 XT5	 ± 10 ± 5.0	V
I_O	Driver peak output current XT15 & XT12 XT5	 180 700	mA
S_D	Serial data rate	0 to 1	MHz
D_C	Clock Duty cycle	50 ± 5	%
T_C	Case operating temperature range	-55 to + 125	°C
T_C	Temperature range	-55 to +125	°C
F_{IN}	Operating frequency	24 ± .01%	MHz

13.0 DC Electrical Characteristics

13.1 SμMMIT XT DC Electrical Characteristics

V_{DD} = 5.0V ± 10%
V_{CC} = 5.0V +10%, -5%
V_{EE} = -12.0V or -15.0V ± 5% (XT15 & XT12)

V_{SS} = 0V
GND = 0V
-55°C < Tc < +125°C

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage			.8	V
V_{IH}	High-level input voltage		2.2		V
V_{ILC}	Low-level input voltage [5]			$.3V_{DD}$	V
V_{IHC}	High-level input voltage [5]		$.7V_{DD}$		V
I_{IN}	Input leakage current TTL input Inputs with pull-up resistors	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$	 -10 -900	 +10 -150	μA
V_{OL}	Low-level output voltage TTL outputs Single-drive buffer CMOS outputs	 I_{OL} = 4.0mA I_{OL} = 1.0μA		 .4 0.05	V
V_{OH}	High-level output voltage TTL outputs Single-drive buffer CMOS outputs	 I_{OH} = 4.0mA I_{OH} = 1.0μA	 2.4 V_{DD}-0.05		V
I_{OZ}	Three-state output leakage current TTL outputs Single-drive buffer	 $I_O = V_{DD}$ or V_{SS}	 -10	 +10	μA
I_{OS}	Short-circuit output current [2,3] TTL outputs Single-drive buffer	V_{DD} = 5.5V, V_O = 0V V_{DD} = 5.5V, $V_O = V_{DD}$	 -100	 +100	mA
C_{IN}	Input capacitance [4]	f = 1MHz @ 0V		45	pF
C_{OUT}	Output capacitance [4] Single-drive buffer	f = 1MHz @ 0V		45	pF
C_{IO}	Bidirectional capacitance [4,6]	f = 1MHz @ 0V		45	pF

Notes:
1. Maximum allowable relative shift = 50mV.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Capacitance measured for initial qualification or design changes which may affect the value.
5. CMOS input only.
6. For all pins except CHA, $\overline{\text{CHA}}$, CHB, and $\overline{\text{CHB}}$.

All Modes

13.2 SμMMIT XT (15 & 12) DC Electrical Characteristics [1,2]

V_{DD} = 5.0V ± 10%
V_{CC} = 5.0V +10%, -5%
V_{EE} = -12.0V or -15.0V ± 5%
V_{SS} = 0V
GND = 0V
-55°C < Tc < +125°C

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
I_{CC}	V_{CC} supply current	V_{EE} = -12V V_{CC} = 5V			
		0% duty cycle (non-transmitting)		140	mA
		50% duty cycle (f = 1MHz)		140	mA
		100% duty cycle (f = 1MHz)		140	mA
		V_{EE} = -15V V_{CC} = 5V			
		V_{CCA} = +5V to +15V			
		0% duty cycle (non-transmitting)		140	mA
		50% duty cycle (f = 1MHz)		140	mA
		100% duty cycle (f = 1MHz)		140	mA
I_{EE}	I_{EE} supply current	V_{EE} = -12V V_{CC} = 5V			
		0% duty cycle (non-transmitting)		80	mA
		50% duty cycle (f = 1MHz)		180	mA
		100% duty cycle (f = 1MHz)		270	mA
		V_{EE} = -15V V_{CC} = 5V			
		0% duty cycle (non-transmitting)		80	mA
		50% duty cycle (f = 1MHz)		180	mA
		100% duty cycle (f = 1MHz)		270	mA
Q_{IDD}	Quiescent current [3]	f = 0MHz		10	mA
S_{IDD}	Standby operating current	f = 24MHz		40	mA

Notes:
1. All tests guaranteed per test figure 31.
2. As specified in test conditions.
3. All inputs tied to V_{DD}.

13.3 SμMMIT XT (5) DC Electrical Characteristics [1,2]

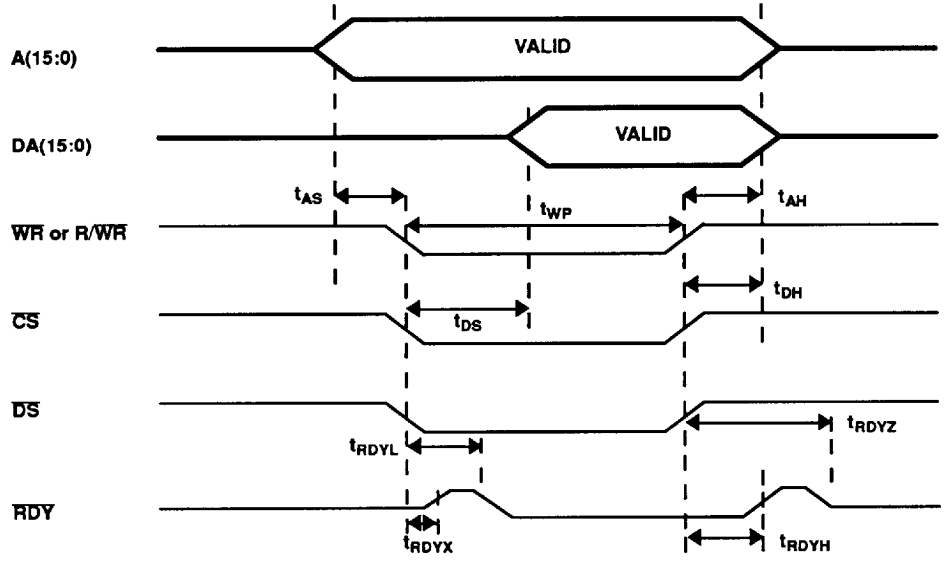
V_{DD} = 5.0V ± 10%
V_{CC} = 5.0V +10%, -5%
V_{SS} = 0V
GND = 0V
-55°C < Tc < +125°C

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
I_{CC}	V_{CC} supply current	0% duty cycle (non-transmitting)		110	mA
		25% duty cycle (f = 1MHz) [3]		355	mA
		50% duty cycle (f = 1MHz) [3]		555	mA
		80% duty cycle (f = 1MHz) [3]		855	mA
		100% duty cycle (f = 1MHz)		855	mA
Q_{IDD}	Quiescent current [2]	f = 0MHz		10	mA
S_{IDD}	Standby operating current	f = 24MHz		40	mA

Notes:
1 All tests guaranteed per test figure 31.
2. All inputs tied to V_{DD}.
3. Guaranteed by characterization, not tested.

14.0 AC Electrical Characteristics

(f = 24MHz ±.01%, Duty Cycle 50% ±5%)

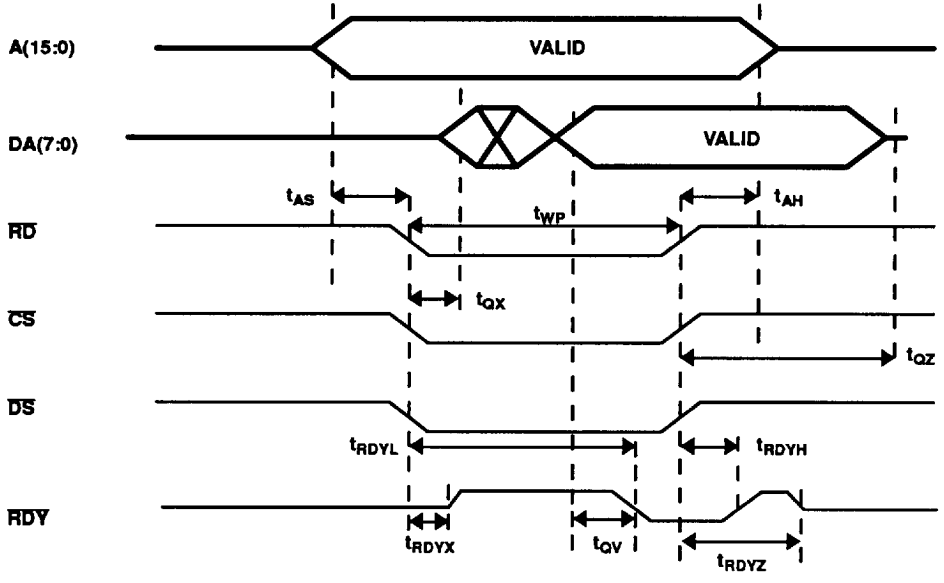


SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	5	--	ns
t_{DS}	Data setup time	--	0	ns
t_{WP}	Write pulse width	230	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{DH}	Data hold time	5	--	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns

All Modes

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.

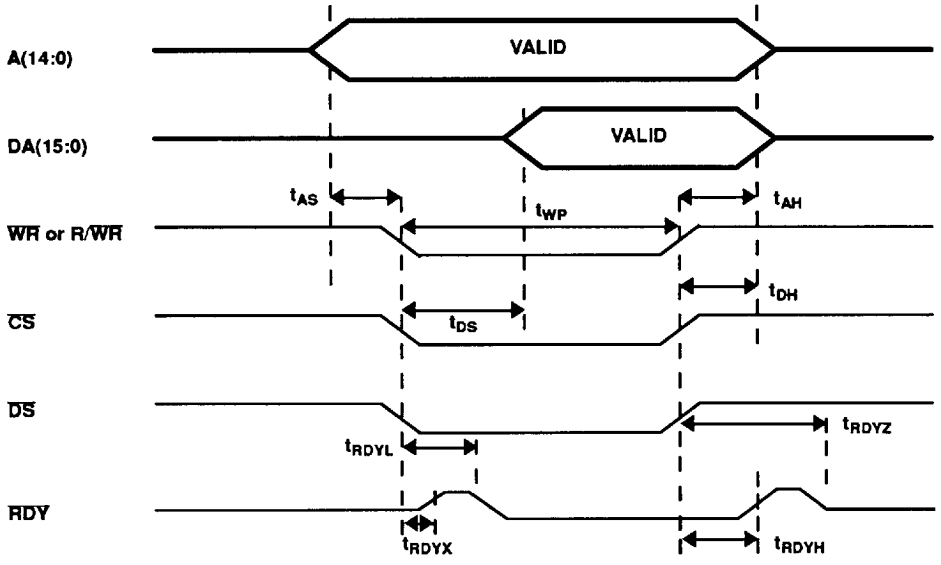
Figure 22. Non-Multiplexed Memory/Register Write (8-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	5	--	ns
t_{QX}	Data low Z	0	30	ns
t_{WP}	Write pulse width	230	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{QV}	Data valid	12	--	ns
t_{QZ}	Data high Z	0	25	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns

Note:
1. Non-buffered mode of operation.

Figure 23. Non-Multiplexed Memory/Register Read (8-Bit)

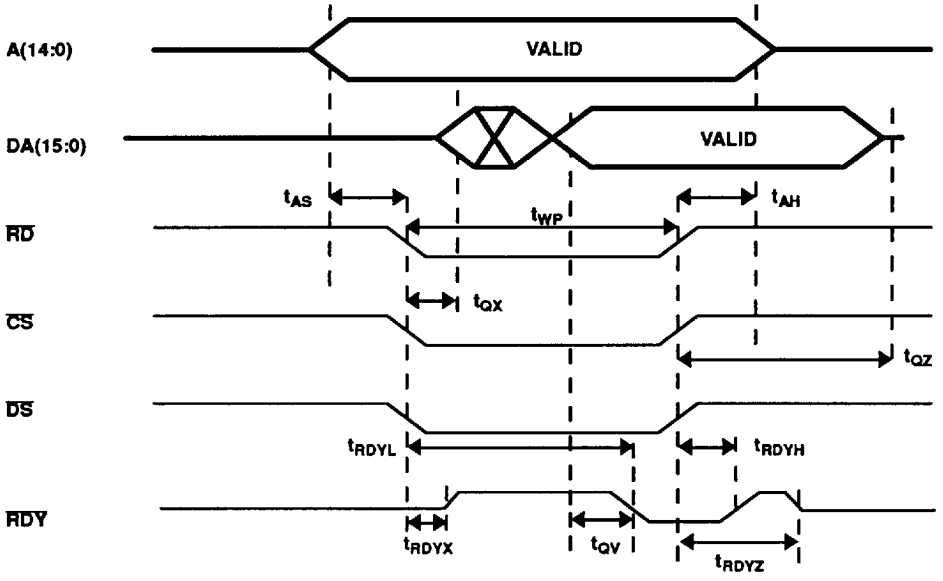


SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	5	--	ns
t_{DS}	Data setup time	--	20	ns
t_{WP}	Write pulse width	230	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{DH}	Data hold time	5	--	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.

All Modes

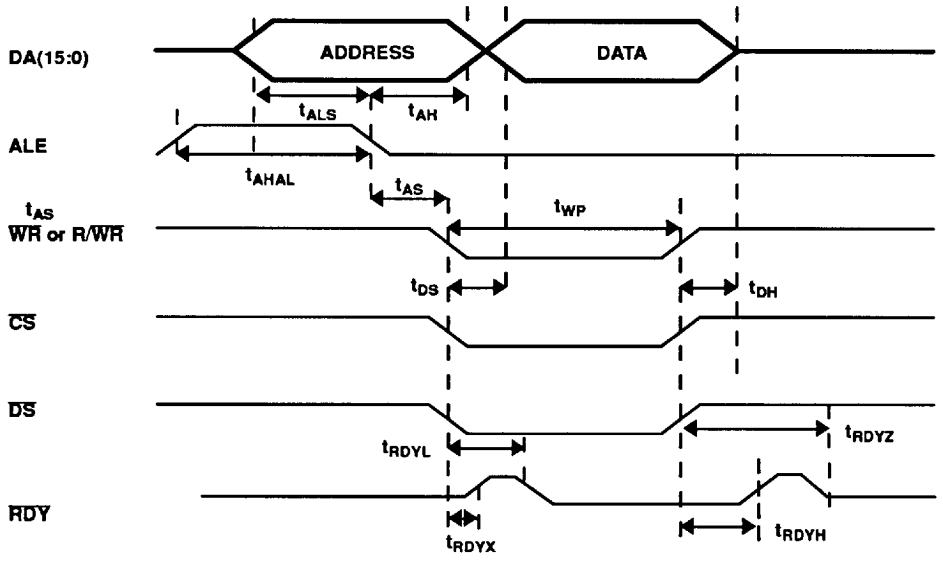
Figure 24. Non-Multiplexed Memory/Register Write (16-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	5	--	ns
t_{QX}	Data low Z	0	30	ns
t_{WP}	Write pulse width	--	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{QV}	Data valid	20	--	ns
t_{QZ}	Data high Z	0	25	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.

Figure 25. Non-Multiplexed Memory/Register Read (16-Bit)

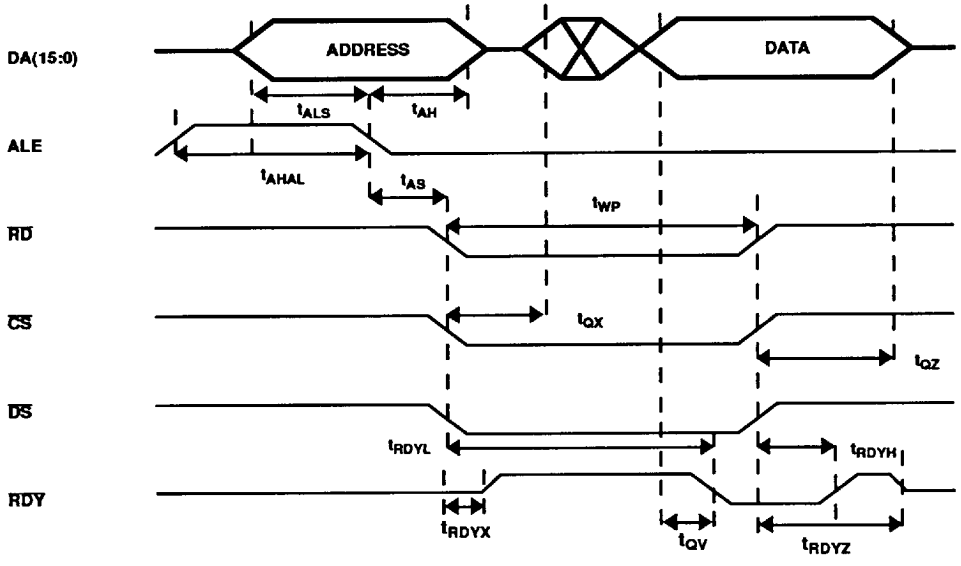


SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	0	--	ns
t_{AHAL}	ALE pulse width	20	--	ns
t_{DS}	Data setup time	--	0	ns
t_{WP}	Write pulse width	230	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{DH}	Data hold time	5	--	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns
t_{ALS}	Address latch setup time	10	--	ns

All Modes

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.

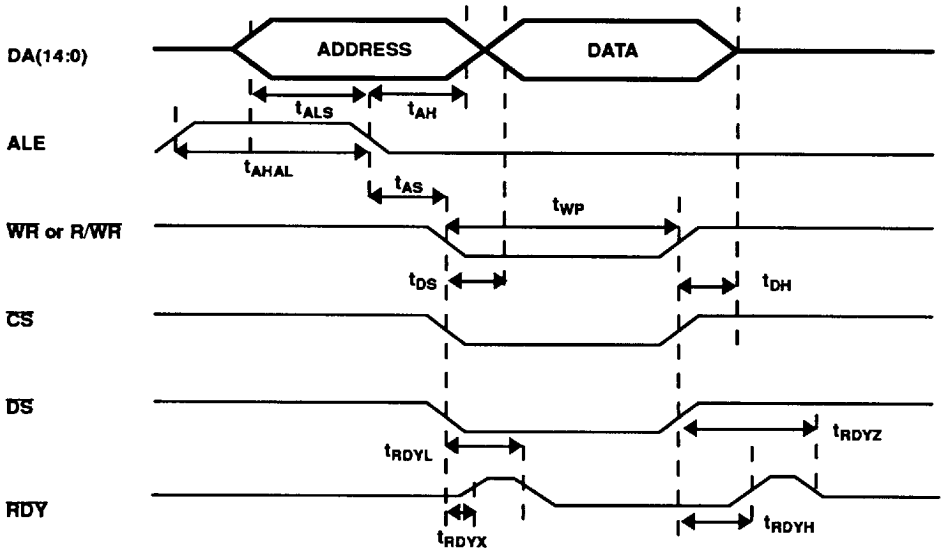
Figure 26. Multiplexed Memory/Register Write (8-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	0	--	ns
t_{AHAL}	ALE pulse width	20	--	ns
t_{QX}	Data low Z	0	30	ns
t_{WP}	Write pulse width	230	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{QV}	Data valid	12	--	ns
t_{QZ}	Data high Z	3	25	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns
t_{ALS}	Address latch setup time	10	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.

Figure 27. Multiplexed Memory/Register Read (8-Bit)

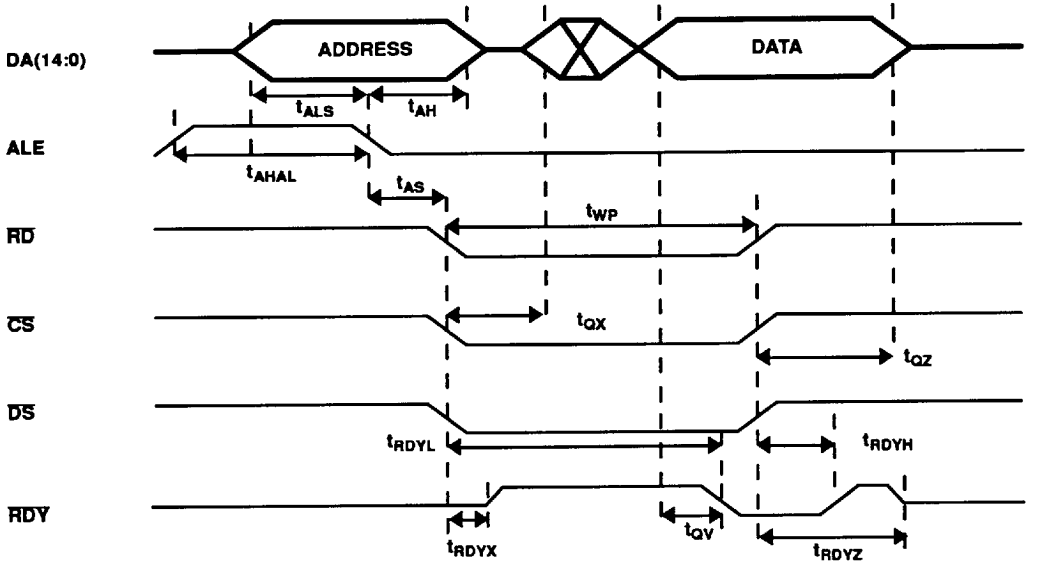


SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	0	--	ns
t_{AHAL}	ALE pulse width	20	--	ns
t_{DS}	Data setup time	--	20	ns
t_{WP}	Write pulse width	230	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{DH}	Data hold time	5	--	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns
t_{ALS}	Address latch setup time	10	--	ns

All Modes

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$, and $\overline{WR}$ or R/$\overline{WR}$.
3. Non-buffered mode of operation.

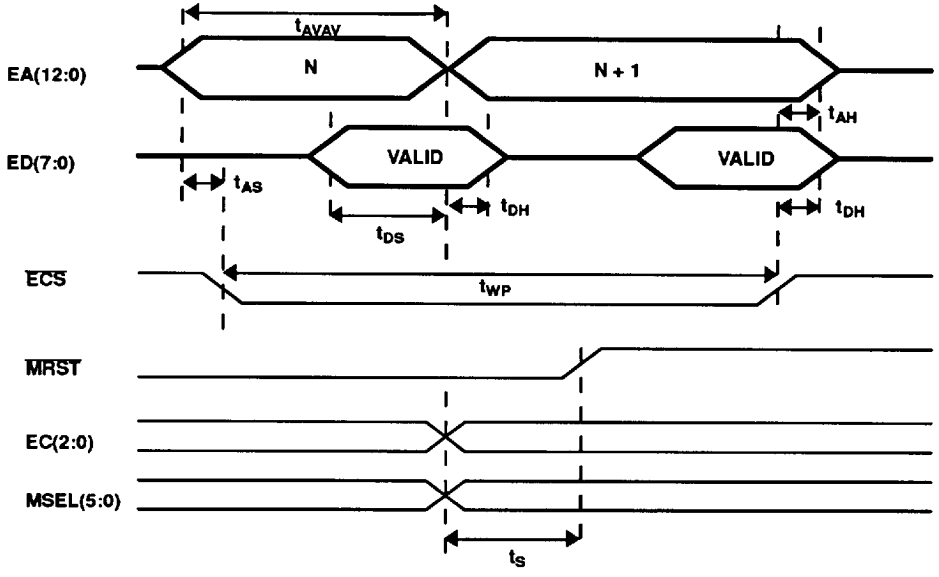
Figure 28. Multiplexed Memory/Register Write (16-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	0	--	ns
t_{AHAL}	ALE pulse width	20	--	ns
t_{QX}	Data low Z	0	30	ns
t_{WP}	Write pulse width	230	1700 [3]	ns
t_{AH}	Address hold time	0	--	ns
t_{QV}	Data valid	12	15	ns
t_{QZ}	Data high Z	3	25	ns
t_{RDYL}	$\overline{RDY}$ low time	150	225	ns
t_{RDYH}	$\overline{RDY}$ high time	0	25	ns
t_{RDYX}	$\overline{RDY}$ low Z	3	--	ns
t_{RDYZ}	$\overline{RDY}$ high Z	--	33	ns
t_{ALS}	Address latch setup time	10	--	ns

Notes:
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$, and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$, and $\overline{RD}$
3. Non-buffered mode of operation.

Figure 29. Multiplexed Memory/Register Read (16-Bit)



SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
t_{AS}	Address setup time	35	--	ns
t_{AH}	Address hold time	35	--	ns
t_{DS}	Data setup time	41	--	ns
t_{DH}	Data hold time	5	--	ns
t_{WP}	Write pulse width	160	--	ns
t_S	Setup time	45	--	ns

Figure 30. Auto-Initialization Read Cycle

All Modes

15.0 Receiver Electrical Characteristics

15.1 SμMMIT XT (15 & 12) Receiver Electrical Characteristics

V_{DD} = 5.0V ± 10%
V_{CC} = 5.0V +10%, -5%
V_{EE} = -12.0V or -15.0V ± 5%
V_{SS} = 0V
GND = 0V
-55°C < Tc < +125°C

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
R_{IZ} [1]	Differential (receiver) input impedance	Input f = 1MHz (no transformer in circuit)	15		Kohms
V_{IC} [1]	Common mode input voltage	Direct-coupled stub; input 1.2V_{PP} 200ns rise/fall time ±25ns, f = 1MHz	-10	+10	V
V_{TH} [1]	Input threshold voltage (no response)	Transformer-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)		0.20	$V_{PP,L-L}$
	Input threshold voltage (no response)	Direct-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)		0.28	$V_{PP,L-L}$
[1]	Input threshold voltage (response)	Transformer-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)	0.86	14.0	$V_{PP,L-L}$
	Input threshold voltage (response)	Direct-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)	1.20	20.0 [1]	$V_{PP,L-L}$
CMRR [1]	Common mode rejection ratio		Pass/Fail [2]		N/A

Notes:
1. Guaranteed by device characterization, not tested.
2. Pass/fail criteria per the test method described in MIL-HDBK-1553 Appendix A, RT Validation Test Plan, Section 5.1.2.2, Common Mode Rejection.

15.2 SμMMIT XT (5) Receiver Electrical Characteristics

V_{DD} = 5.0V ± 10% GND = 0V
V_{CC} = 5.0V +10%, -5% -55°C < T_C < +125°C
V_{SS} = 0V

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IC} [1]	Common mode input voltage	Direct-coupled stub; input 1.2V_{PB} 200ns rise/fall time ±25ns, f = 1MHz	-5	5	V
V_{TH} [1]	Input threshold voltage (no response)	Transformer-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)		0.20	V_{P-P}
	Input threshold voltage (no response)	Direct-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)		0.28	V_{P-P}
1	Input threshold voltage (response)	Transformer-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)	0.86	14.0	V_{P-P}
1	Input threshold voltage (response)	Direct-coupled stub; input at f = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)	1.20	20.0	V_{P-P}
CMRR [1,2]	Common mode rejection ratio		Pass/Fail		N/A
V_{IDR}	Differential input voltage level		--	8.0	V_{P-P}

Notes:
1. Guaranteed by device characterization, not tested.
2. Pass/fail criteria per the test method described in MIL-HDBK-1553 Appendix A, RT Validation Test Plan, Section 5.1.2.2, Common Mode Rejection.

All Modes

16.0 Transmitter Electrical Characteristics

16.1 SμMMIT XT (15 & 12) Transmitter Electrical Characteristics

V_{DD} = 5.0V ± 10% V_{SS} = 0V
V_{CC} = 5.0V +10%, -5% GND = 0V
V_{EE} = -12.0V or -15.0V ± 5% -55°C < Tc < +125°C

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
V_O	Output voltage swing per MIL-STD-1553B [1] (see figure 32)	18	27	$V_{PP,L-L}$	Transformer-coupled stub, figure 31, Point A; input f = 1MHz, R_L = 70 ohms
	per MIL-STD-1553B (see figure 32)	6.0	9	$V_{PP,L-L}$	Direct-coupled stub, figure 31, Point A; input f = 1MHz, R_L = 35 ohms
	per MIL-STD-1553A [1] (see figure 32)	6.0	20	$V_{PP,L-L}$	Figure 31, Point A; input f = 1MHz, RL = 35 ohms
V_{NS} [1]	Output noise voltage differential (see figure 32)		14	mV-RMS L-L	Transformer-coupled stub, figure 31, Point A; input f = DC to 10MHz, RL = 70 ohms
			5	mV-RMS L-L	Direct-coupled stub, figure 31, Point A; input f = DC to 10MHz, R_L = 35 ohms
V_{OS} [1]	Output symmetry (see figure 32)	-250	+250	$mV_{PP,L-L}$	Transformer-coupled stub, figure 31, Point A; RL = 70 ohms, measurement taken 2.5μs after end of transmission
		-90	+90	$mV_{PP,L-L}$	Direct-coupled stub, figure 31, Point A; R_L = 35 ohms, measurement taken 2.5μs after end of transmission
V_{DIS} [1]	Output voltage distortion (overshoot or ring) (see figure 32)	-900	+900	$mV_{peak,L-L}$	Transformer-coupled stub, figure 31, Point A; R_L = 70 ohms
		-300	+300	$mV_{peak,L-L}$	Direct-coupled stub, figure 31, Point A; R_L = 35 ohms
T_{IZ} [1]	Terminal input impedance	1		Kohm	Transformer-coupled stub, figure 31, Point A; input f = 75KHz to 1MHZ (power on or power off; non-transmitting, R_L removed from circuit).
		2		Kohm	Direct-coupled stub, figure 31, Point A; input f = 75KHz to 1MHZ (power on or power off; non-transmitting, R_L removed from circuit).

Note:
1. Guaranteed by device characterization, not tested.

16.2 SμMMIT XT (5) Transmitter Electrical Characteristics

V_{DD} = 5.0V ± 10% GND = 0V
V_{CC} = 5.0V +10%, -5% -55°C < Tc < +125°C
V_{SS} = 0V

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
V_O	Output voltage swing per MIL-STD-1553B [1] (see figure 32)	18	27	$V_{PP,L-L}$	Transformer-coupled stub, figure 31, Point A; input f = 1MHz, R_L = 70 ohms
	per MIL-STD-1553B (see figure 32)	6.0	9	$V_{PP,L-L}$	Direct-coupled stub, figure 31, Point A; input f = 1MHz, R_L = 35 ohms
	per MIL-STD-1553A [1] (see figure 32)	6.0	20	$V_{PP,L-L}$	
V_{NS} [1]	Output noise voltage differential (see figure 32)		14	mV-RMS L-L	Transformer-coupled stub, figure 31, Point A; input f = DC to 10MHz, RL = 70 ohms
			10	mV-RMS L-L	Direct-coupled stub, figure 31, Point A; input f = DC to 10MHz, R_L = 35 ohms
V_{OS} [1]	Output symmetry (see figure 32)	-360	+360	$mV_{PP,L-L}$	Transformer-coupled stub, figure 31, Point A; R_L = 70 ohms, measurement taken 2.5μs after end of transmission
		-90	+90	$mV_{PP,L-L}$	Direct-coupled stub, figure 31, Point A; R_L = 35 ohms, measurement taken 2.5μs after end of transmission
V_{DIS} [1]	Output voltage distortion (overshoot or ring) (see figure 32)	-2	+2	$V_{peak,L-L}$	Transformer-coupled stub, figure 31, Point A; R_L = 70 ohms
		-1.0	+1.0	$V_{peak,L-L}$	Direct-coupled stub, figure 31, Point A; R_L = 35 ohms
T_{IZ} [1]	Terminal input impedance	1		Kohm	Transformer-coupled stub, figure 31, Point A; input f = 75KHz to 1MHZ (power on or power off; non-transmitting, R_L removed from circuit).
		2		Kohm	Direct-coupled stub, figure 31, Point A; input f = 75KHz to 1MHZ (power on or power off; non-transmitting, R_L removed from circuit).
T_{OZ}	Differential output impedance	10		Kohm	Input f = 1 MHz (no transformer in circuit)

Note:
1. Guaranteed by device characterization, not tested.

All Modes

17.0 AC Electrical Characteristics

17.1 SμMMIT XT (15 & 12) AC Electrical Characteristics

V_{DD} = 5.0V ± 10% V_{SS} = 0V
V_{CC} = 5.0V +10%, -5% GND = 0V
V_{EE} = -12.0V or -15.0V ± 5% -55°C < T_C < +125°C

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
t_R, t_F	Transmitter output rise/ fall time (see figure 33)	100	300	ns	Input f = 1MHz 50% duty cycle: direct-coupled RL = 35 ohms output at 10% through 90% points TXOUT, $\overline{\text{TXOUT}}$. Figure 33.
t_{RZCD}	Zero crossing distortion (see figure 34)	-150	150	ns	Direct-coupled stub; input f = 1MHz, 3 V_{PP} (skew INPUT ±150ns), rise/fall time 200ns.
t_{TZCS}	Zero crossing stability (see figure 34)	-25	25	ns	Input TXIN and $\overline{\text{TXIN}}$ should create Transmitter output zero crossings at 500ns, 1000ns, 1500ns, and 2000ns. These zero crossings should not deviate more than ±25ns.

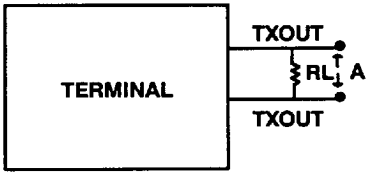
Note:
1. Guaranteed by device characterization, not tested.

17.2 SμMMIT XT (5) AC Electrical Characteristics

V_{DD} = 5.0V ± 10% GND = 0V
V_{CC} = 5.0V +10%, -5% -55°C < T_C < +125°C
V_{SS} = 0V

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
t_R, t_F	Transmitter output rise/ fall time (see figure 33)	100	300	ns	Input f = 1MHz 50% duty cycle: direct-coupled RL = 35 ohms output at 10% through 90% points TXOUT, $\overline{\text{TXOUT}}$. Figure 33.
t_{RZCD}	Zero crossing distortion (see figure 34)	-150	150	ns	Direct-coupled stub; input f = 1MHz, 3 V_{PP} (skew INPUT ±150ns), rise/fall time 200ns.
t_{TZCS}	Zero crossing stability (see figure 34)	-25	25	ns	Input TXIN and $\overline{\text{TXIN}}$ should create Transmitter output zero crossings at 500ns, 1000ns, 1500ns, and 2000ns. These zero crossings should not deviate more than ±25ns.

Note:
1. Guaranteed by device characterization, not tested.



Notes:
1. Transformer Coupled Stub:
   Terminal is defined as transceiver plus isolation transformer.
2. Direct Coupled Stub:
   Terminal is defined as transceiver plus isolation transformer and fault resistors.

Figure 31. Transceiver Test Circuit MIL-STD-1553B

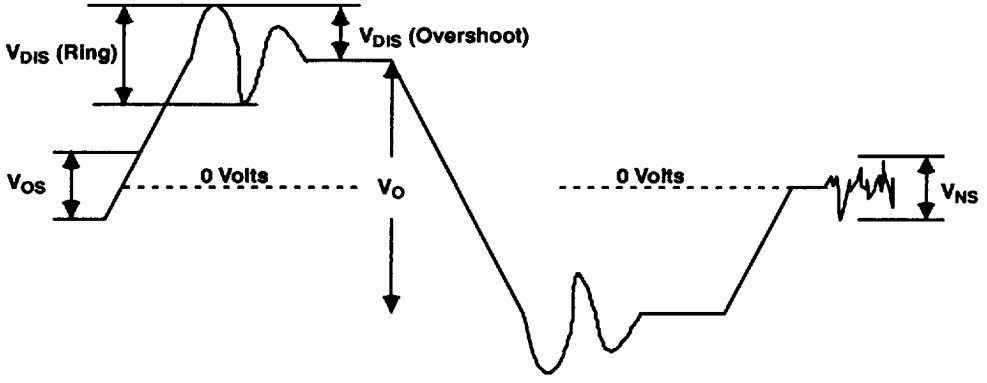


Figure 32. Transmitter Output Characteristics (V_{DIS}, V_{OS}, V_{NS}, V_O)

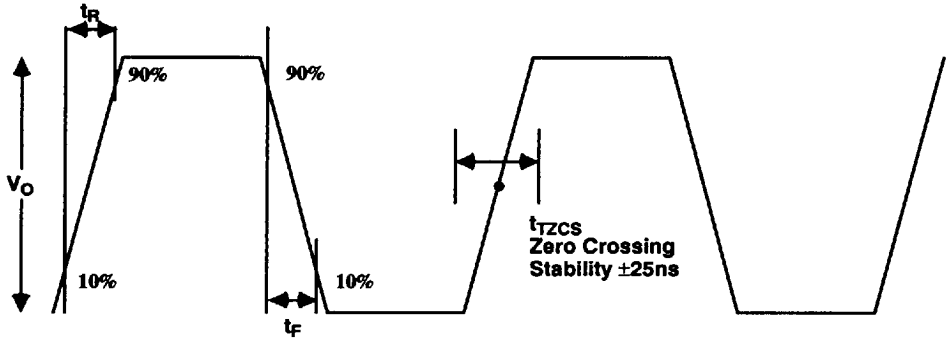


Figure 33. Transmitter Output Zero Crossing Stability (t_{TZCS}, t_R, t_F)

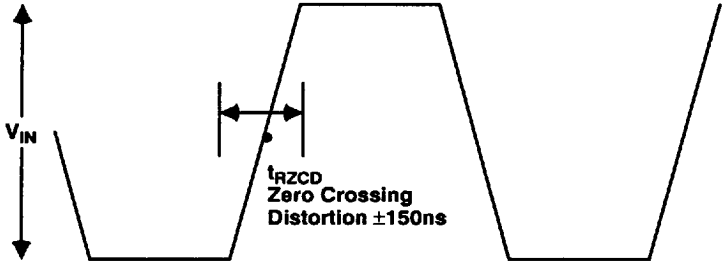
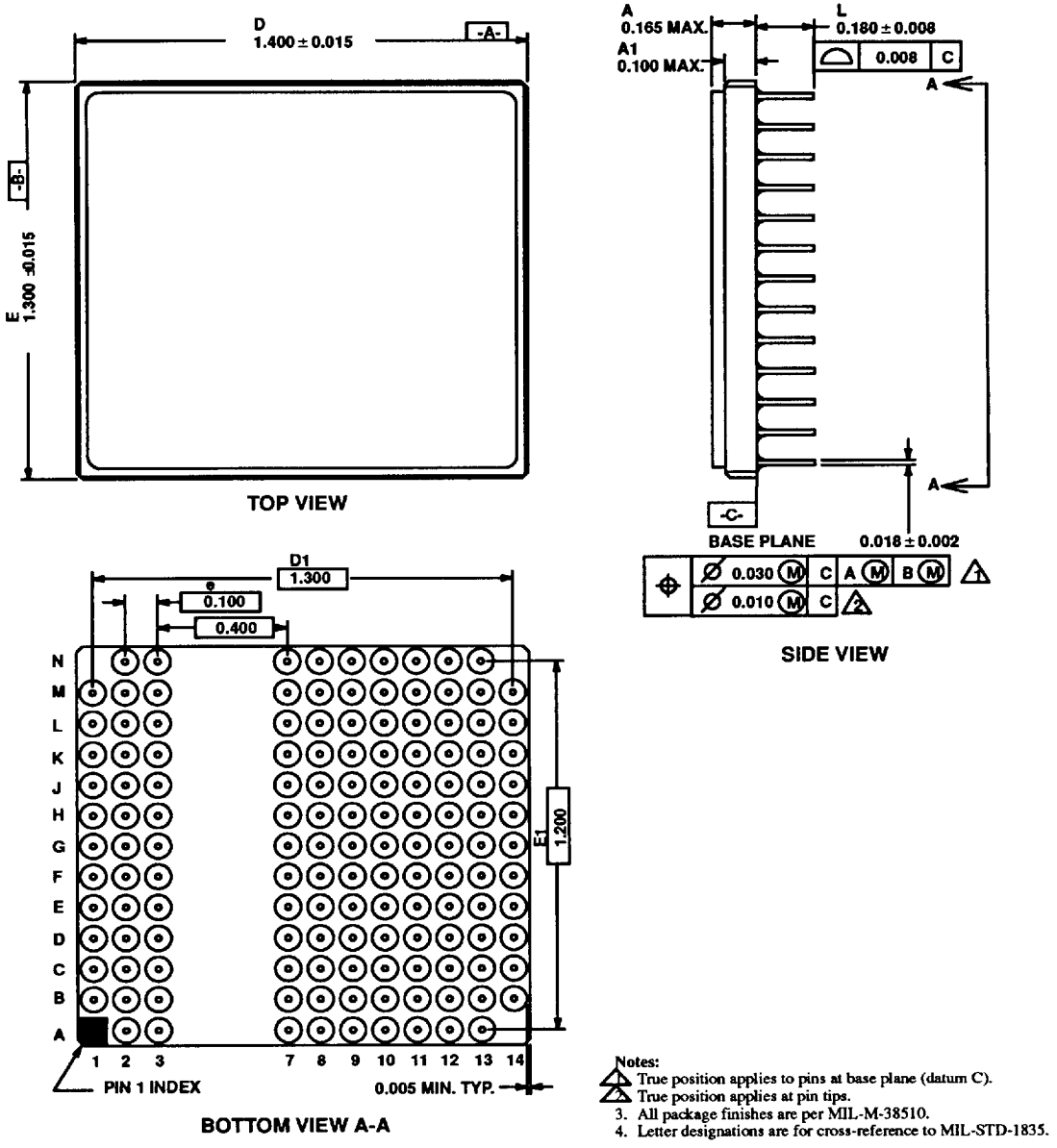


Figure 34. Receiver Input Zero Crossing Distortion (t_{RZCD})

18.0 PACKAGING



Notes:
1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All package finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-STD-1835.

Figure 35. 139-Pin Pingrid Array

19.0 Ordering Information

SμMMIT XT: Prototypes and reduced High-Reliability

UT 69151 ** - * * ***

Lead Finish: [1]
(A) = Hot solder dipped
(C) = Gold
(X) = Factory option [2]

Screening:
(M) = The SμMMIT XT will be available in an SMD version (3Q94). Please contact UTMC for the correct part number and ordering information.
(C) = Reduced High-Reliability flow [3]
(P) = Prototype flow [4]

Package Type:
(G) = 139-pin ceramic Pingrid Array (PGA)
(W) = 140-lead ceramic top-brazed flatpack (0.025" lead pitch)

Device Type Modifier:
(XT12) = +5V/-12V operation
(XT15) = +5V/-15V operation
(XT5) = +5V operation

Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Reduced High-Reliability flow per *UTMC Manufacturing Flows Technical Description*. Devices have 48 hours of burn-in and are tested at -55°C, room temperature, and 125°C.
4. Prototype flow per *UTMC Manufacturing Flows Technical Description*. Devices have prototype assembly and are tested at 25°C only. Lead finish is at UTMC's option and an "X" must be specified when ordering.
5. The SμMMIT XT product offering is not available with radiation hardening.