Features

- High speed
  - Maximum access times of 15, 20, 25 and 35 ns
- Fast Output Enable pin for ease of application
- Output Enable time as fast as 8 ns
- Fully static operation
  - No clock or refresh required
- TTL compatible inputs and outputs
- Low Power Consumption
  - Standard Power (typ)
    Active 400 mW
    Standby 10 mW
  - Low Power (typ)
    Active 400 mW
    Standby 500 µW
- JEDEC Standard pinout
- 28-pin DIP and SOJ packages for V63C70
- 24-pin DIP and SOJ packages for V63C71

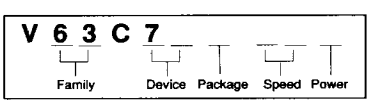
Description

The V63C70 and V63C71 are high speed, low power, 65,536 word by 8 bit static RAMs fabricated using Vitelic's high performance CMOS technology. This high reliability process, coupled with innovative circuit design techniques, yields access times as low as 15 ns maximum.

The V63C70 has both Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) for enhanced system flexibility. Either input, when high, will force the outputs to high impedance. The V63C71 has only the Chip Enable pin. When $\overline{CE}$ is high, the device assumes a low-power standby mode in which device power dissipation is reduced. Operation is from a single 5V (±10%) power supply. A low-power (L) version is also offered with standby current as low as 0.1 mA.

The V63C70 is available in space-saving 300 mil, 28 pin plastic DIP and 300 mil SOJ packages. The V63C71 is available in 24 pin DIP and SOJ packages.

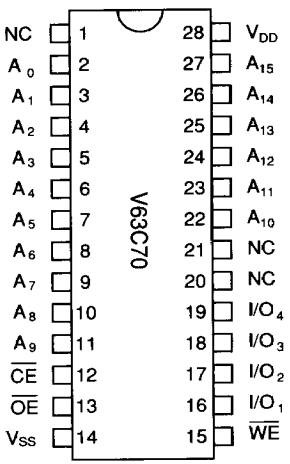
Part No.	Package	Sym	Pin Count
V63C70	Plastic DIP	S	28
V63C70	Plastic SOJ	K	28
V63C71	Plastic DIP	S	24
V63C71	Plastic SOJ	K	24



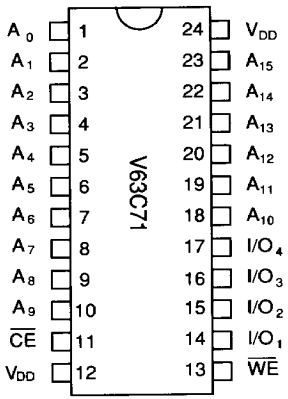
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	S	K	15	20	25	35	Std.	Low	
0°C to 70°C	•	•	•	•	•	•	•	•	Blank

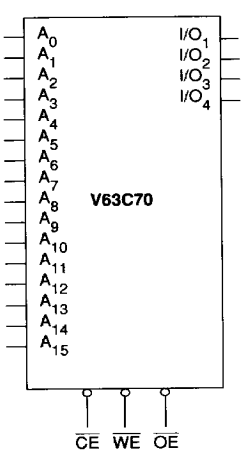
DIP/SOJ
PIN CONFIGURATION
Top View

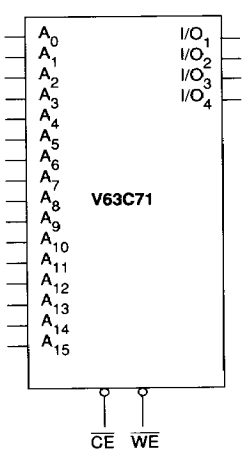


DIP/SOJ
PIN CONFIGURATION
Top View



Logic Symbols

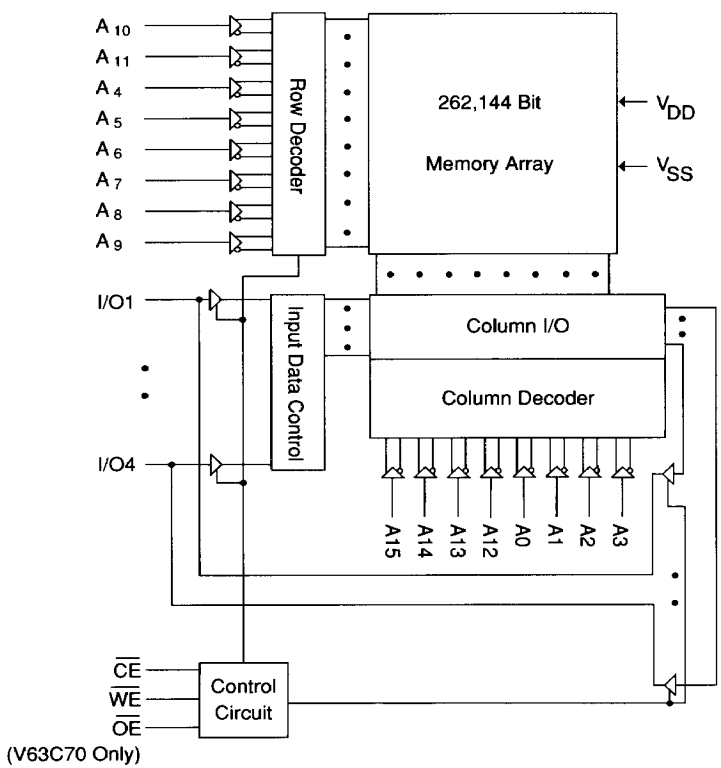




Truth Table

Mode	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	I/O	I_{DD}
Not Selected Power Down	X	H	X	High-Z	Standby
Outputs Disabled	H	L	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	X	L	L	D_{IN}	Active

Block Diagram



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Absolute Maximum Ratings*

Storage Temperature ..... -55°C to +125°C
Ambient Temperature
Under Bias ..... -55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... -0.5 to +7.0V
...Maximum V_{DD} Voltage..... 7.0V
Data Out Current 20mA
Power Dissipation 1.0W

* **NOTE:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions

(T_A = 0° to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{DD}	V
V_{IL}	Input Low Voltage	–0.5		0.8	V

Capacitance*

(T_A = 25°C, f = 1 MHz, V_{DD} = 0 V)

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	5	pF
$C_{I/O}$	I/O Capacitance	—	7	pF

* Capacitance is sampled and not 100% tested.

AC Test Conditions

Input pulse levels ..... 0 to 3.0V*
Input rise/fall time ..... 5 ns max.*
Input/Output timing levels 1.5V
Output Load—As specified in Figure 2 or Figure 3 (includes jig and/or scope capacitance)
*Refer to Figure 1

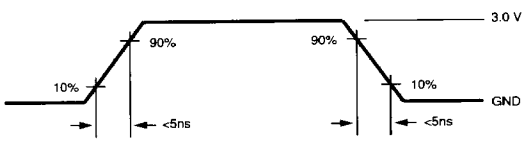


Figure 1. Input Pulse Specification for AC Testing

Pin Names

$A_0 - A_{15}$	Address Inputs
$I/O_1 - I/O_4$	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$ (V63C70 only)	Output Enable
V_{DD}	+5V Power Supply
V_{SS}	Ground

AC Test Conditions

Signal transition of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0 to 3.0V, output loading as shown in diagrams below.

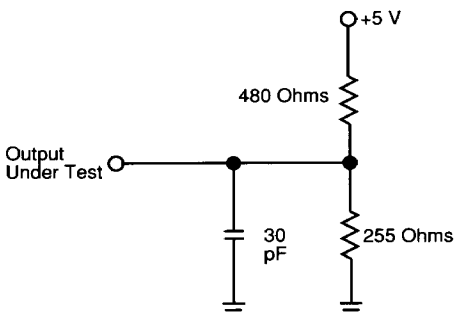


Figure 2. AC Test Load

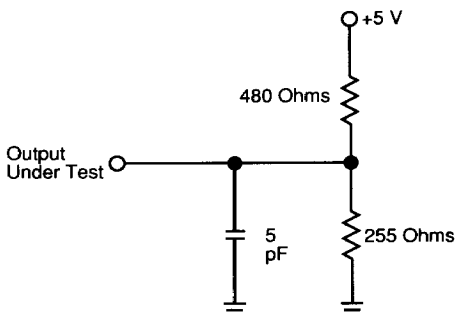


Figure 3. AC Test Load

D.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	V63C70/V63C71			V63C70L/V63C71L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$	-10		10	-10		10	µA
I_{LO}	I/O Leakage Current	$V_{SS} \le D_{OUT} \le V_{DD}$ Outputs Disabled	-10		10	-10		10	µA
I_{SB1}	TTL Standby Current	V_{DD} = 5.5 V, $\overline{CE} \ge V_{IH}$		15	25		15	25	mA
I_{SB2}	CMOS Standby Current	V_{DD} = 5.5V, $\overline{CE} > V_{DD}$ -0.3		2	20		0.1	2	mA
V_{OH}	Output High Voltage	V_{DD} = 4.5 V I_{OH} = -4.0 mA	2.4			2.4			V
V_{OL}	Output Low Voltage	V_{DD} = 4.5 V I_{OL} = 8.0 mA		0.4				0.4	V

Symbol	Parameter	Test Conditions	V63C70/V63C71				V63C70L/V63C71L				Unit
			15	20	25	35	15	20	25	35	
I_{DD1}	Static Power Supply Current	V_{DD} = 5.5V I_{OUT} = 0, f = 0 Hz	70	70	70	70	50	50	50	50	mA
I_{DD2}	Dynamic Operating Current	V_{DD} = 5.5V f = f_{MAX}, I_{OUT} = 0	100	100	80	80	80	80	80	80	mA

AC Characteristics (1)

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise specified.

Read Cycle

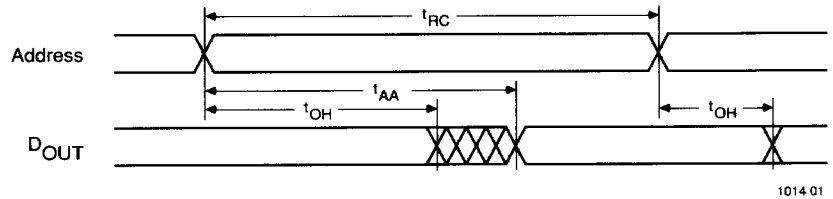
Symbol	Parameter	15		20		25		35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Read Cycle Time	15		20		25		35		ns	
t_{AA}	Address Access Time		15		20		25		35	ns	
t_{OH}	Output Hold Time	3		5		5		5		ns	
t_{ACE}	$\overline{CE}$ Access Time		15		20		25		45	ns	
t_{OE}	$\overline{OE}$ Access Time (V63C70)		8		9		10		12	ns	
t_{LZ}	$\overline{OE}$ to Low-Z Output (V63C70)		3		3		3		3	ns	
t_{HZ}	$\overline{OE}$ to High-Z Output (V63C70)		8		9		10		12	ns	2
t_{LZCE}	$\overline{CE}$ to Low-Z Output	5		5		5		5		ns	3
t_{CHZ}	$\overline{CE}$ to High-Z Output		10		11		12		15	ns	
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		0		ns	2, 3
t_{PD}	$\overline{CE}$ to Power Down		15		20		25		35	ns	

Write Cycle (4)

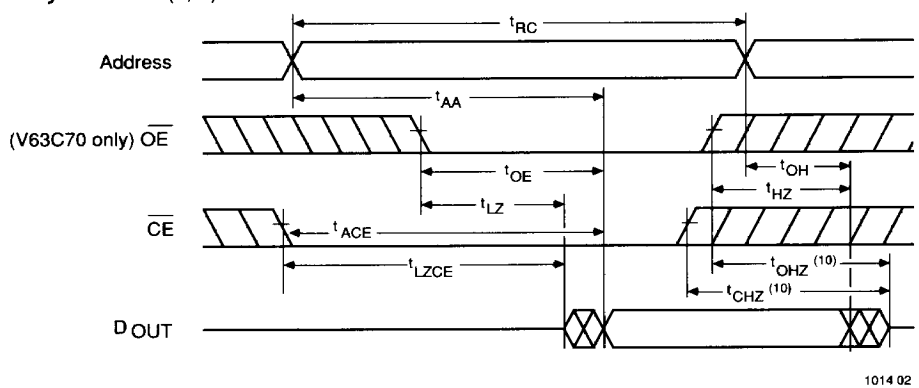
At recommended operating conditions, unless otherwise specified.

Symbol	Parameter	15		20		25		35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WC}	Write Cycle Time	15		20		25		35		ns	
t_{SCE}	$\overline{CE}$ to End of Write	12		15		20		25		ns	
t_{AW}	Address Setup to End of Write	12		15		20		25		ns	
t_{AH}	Address Hold from End of Write	0		0		0		0		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{WP}	Write Pulse Width	10		12		15		20		ns	5
t_{DS}	Data Setup to End of Write	8		10		12		15		ns	
t_{DH}	Data Hold from End of Write	0		0		0		0		ns	
t_{WHZ}	$\overline{WE}$ Low to High-Z Outputs		12		13		13		13	ns	2
t_{WLZ}	$\overline{WE}$ High to Low-Z Outputs	0		0		0		0		ns	
t_{WR}	Write Recovery Time	0		0		0		0		ns	
t_{OW}	Output Active from End of Write	5		5		5		5		ns	

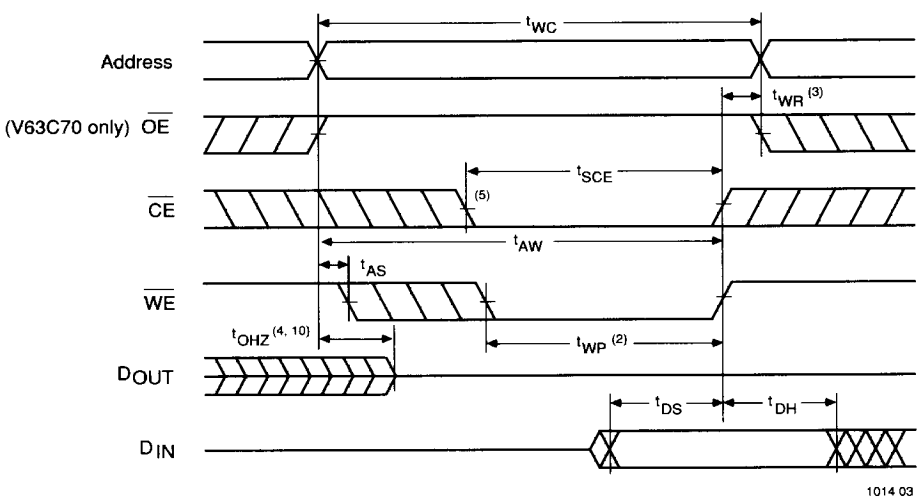
Read Cycle No. 1 (7, 8)



Read Cycle No. 2 (6, 8)



Write Cycle No. 1 (WE Controlled) (4, 9)



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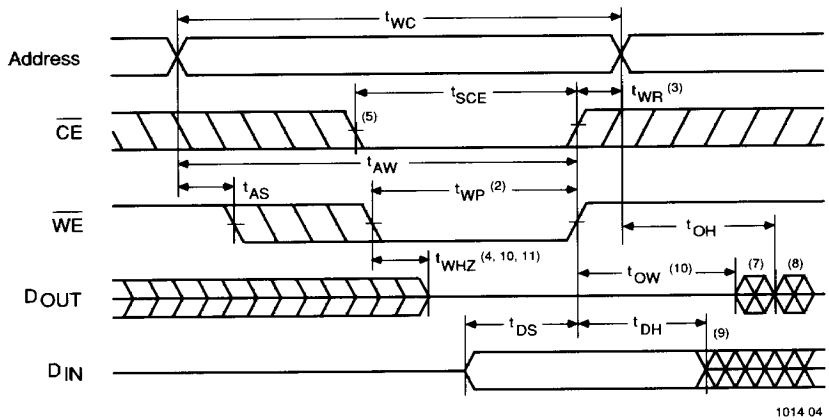
Write Cycle No. 2 ($\overline{CE}$ Controlled) (4, 9)



NOTES:

(1) Test Conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, Input pulse levels of 0 to 3.0V and output loading specified in Figure 2.

(2) t_{HZOE}, t_{HZCE} and t_{HZWE} are tested with the load in Figure 3. Transition is measured ±500 mV from steady state voltage.

(3) At any given temperature and voltage conditions t_{HZCE} is less than t_{LZE} for all devices. These parameters are sampled and not 100% tested.

(4) The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. All signals must be in their valid state to initiate a Write and any of the three signals can terminate the Write by going false. The Data Input Setup and Hold timing are referenced to the rising edge of the signal that terminates the Write.

(5) Tested with $\overline{OE}$ high (only for V63C70).

(6) $\overline{WE}$ is high for a Read cycle.

(7) The device is continuously selected when $\overline{OE}$, $\overline{CE}$ = V_{IL} (only for V63C70).

(8) Address is valid prior to or coincident with $\overline{CE}$ low and $\overline{CE}$ high transitions.

(9) I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$ (only for V63C70).