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VP531E/VP551E

NTSC/PAL Digital Video Encoder

Advance Information

Supersedes DS4573 1.4 May 1997 edition

DS4573 - 2.3 October1998

The VP531/VP551 converts digital Y, Cr, Cb, data into analog NTSC/PAL composite video and S-video signals The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device accepts data inputs complying with CCIR Recommendation 601 and 656. The data is time multiplexed on an 8 bit bus at 27MHz and is formatted as Cb, Y, Cr, Y (i.e. 4:2:2). The video blanking and sync information from REC 656 is included in the data stream when the VP531 is working in slave mode.

The output pixel rate is 27MHz and the input pixel rate is half this frequency, i.e. 13.5MHz.

All necessary synchronisation signals are generated internally when the device is operating in master mode. In slave mode the device will lock to the TRS codes or the HS and VS inputs.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Two 9 bit digital to analog converters (DACs) are used to convert the digital luminance and chrominance data into analog signals. An inverted composite video signal is generated by summing the complementary current outputs of each DAC. An internally generated reference voltage provides the biasing for the DACs.

FEATURES

- Converts Y, Cr, Cb data to analog composite video and S-video
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- SMPTE 170M NTSC or CCIR 624 PAL compatible outputs
- GENLOCK mode
- I^2C bus serial microprocessor interface
- VP531E supports Macrovision anti-taping format REV 6.1 in PAL and REV 7.01 in NTSC

APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- Video games
- Karaoke
- Digital VCRs

ORDERING INFORMATION

VP531E/CG/GP1N
VP551E/CG/GP1N

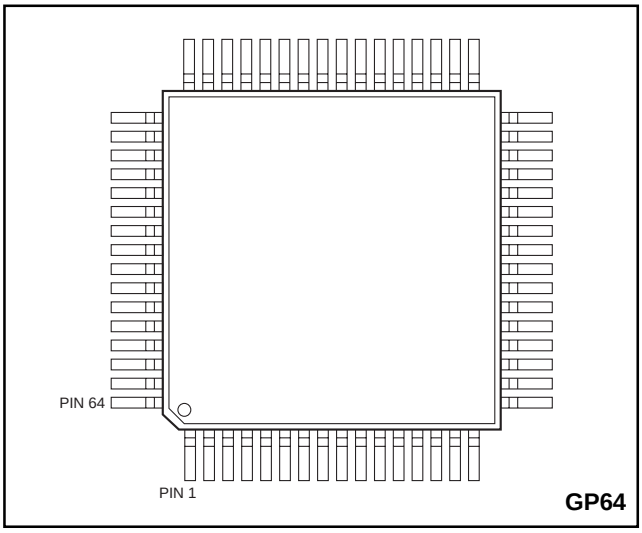

Fig.1 Pin connections (top view)

PIN	FUNCTION	PIN	FUNCTION
1	VDD	33	VDD
2	GND	34	$\overline{\text{RESET}}$
3	D0 (VS I/O)	35	REFSQ
4	D1 (HS I/O)	36	GND
5	D2 (FC0 O/P)	37	VDD
6	D3 (FC1 O/P)	38	GND
7	D4 (FC2 O/P)	39	PD7
8	D5	40	PD6
9	D6 (SCSYNC I/P)	41	PD5
10	D7 (PALID I/P)	42	PD4
11	GND	43	PD3
12	VDD	44	PD2
13	GND	45	PD1
14	GND	46	PD0
15	PXCK	47	GND
16	VDD	48	VDD
17	CLAMP	49	AGND
18	COMPSYNC	50	VREF
19	GND	51	DACGAIN
20	VDD	52	COMP
21	TDO	53	AVDD
22	TDI	54	LUMAOUT
23	TMS	55	$\overline{\text{AGND}}$
24	TCK	56	$\overline{\text{COMPOUT}}$
25	GND	57	AGND
26	SA1	58	CHROMAOUT
27	SA2	59	AVDD
28	SCL	60	N/C
29	VDD	61	N/C
30	SDA	62	AVDD
31	GND	63	AVDD
32	VDD	64	N/C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs TTL compatible (except SDA, SCL)						
Input high voltage		VIN	2.0			V
Input low voltage		VIL			0.8	V
Digital Inputs SDA, SCL						
Input high voltage		VIH	0.7 VDD			V
Input low voltage		VIL			0.3 VDD	V
Input high current	VIN = VDD	IIH			10	µA
Input low current	VIN = VSS	IIL			-10	µA
Digital Outputs CMOS compatible						
Output high voltage	IOH = -1mA	VOH	3.7			V
Output low voltage	IOL = +4mA	VOL			0.4	V
Digital Output SDA						
Output low voltage	IOL = +6mA	VOL			0.6	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC CHARACTERISTICS DACs

Parameter	Symbol	Min.	Typ.	Max.	Units
Accuracy (each DAC)					
Integral linearity error	INL			±1.5	LSB
Diffential linearity error	DNL			±1	LSB
DAC matching error				±5	% grey
Monotonicity			guaranteed		
LSB size			66.83		µA
Internal reference voltage	V_{REF}		1.050		V
Internal reference voltage output impedance	Z_R		27k		Ω
Reference Current (V_{REF}/R_{REF}) R_{REF} = 769Ω	I_{REF}		1.3699		mA
DAC Gain Factor ($V_{OUT} = K_{DAC} \times I_{REF} \times R_L$). V_{OUT} = DAC code 511	K_{DAC}		24.93		
Peak Glitch Energy (see fig.8)			80		pV-s
CVBS (see note), Y and C - NTSC (pedestal enabled)					
Maximum output, relative to sync bottom			33.75		mA
White level relative to black level			17.64		mA
Black level relative to blank level			1.40		mA
Blank level relative to sync level			7.62		mA
Colour burst peak - peak			7.62		mA
DC offset (bottom of sync)			0.40		mA
CVBS, Y and C - PAL					
Maximum output			34.15		mA
White level relative to black level			18.71		mA
Black level relative to sync level			8.02		mA
Colour burst peak - peak			8.02		mA
DC offset (bottom of sync)			0.00		mA

Note: For the inverted CVBS output subtract the above currents from the maximum output (DAC code 511 = 34.12mA).
All figures are for: R_{REF} = 769Ω, R_L = 37.5Ω. When the device is set up in NTSC mode there is a +0.25% error in the PAL levels.
If R_L = 75Ω then R_{REF} = 1538Ω

ABSOLUTE MAXIMUM RATINGS

Supply voltage	VDD, AVDD	-0·3 to 7·0V
Voltage on any non power pin		-0·3 to VDD+0·3V
Ambient operating temperature		0 to 70°C
Storage temperature		-55°C to 150°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VDD, AVDD	4.75	5.00	5.25	V
Power supply current (including analog outputs)	IDD		150		mA
Input clock frequency	PXCK	-50ppm	27.00	+50ppm	MHz
SCL clock frequency	fscl			500	kHz
Analog video output load			37.5		Ω
DAC gain resistor			769		Ω
Ambient operating temperature		0		70	°C

VIDEO CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth			5.5		MHz
Chrominance bandwidth (Extended B/w mode)			1.3		MHz
Chrominance bandwidth (Reduced B/w mode)			650		kHz
Burst frequency (NTSC)			3.57954545		MHz
Burst frequency (PAL-B, D,G, H, I)			4.43361875		MHz
Burst frequency (PAL-N Argentina)			3.58205625		MHz
Burst cycles (NTSC and PAL-N)			9		Fsc cycles
Burst cycles (NTSC and PAL-B, D, G, H,I)			10		Fsc cycles
Burst envelope rise / fall time (NTSC and PAL-B, D, G, H,I)			300		ns
Analog video sync rise / fall time (NTSC and PAL-N)			145		ns
Analog video blank rise / fall time (NTSC and PAL-B, D, G, H,I)			245		ns
Differential gain			1.5		% pk-pk
Differential phase			0.5		° pk-pk
Signal to noise ratio (unmodulated ramp)					dB
Chroma AM signal to noise ratio (100% red field)					dB
Chroma PM signal to noise ratio (100% red field)				-61	dB
Hue accuracy				-56	%
Colour saturation accuracy				-58	%
Residual sub carrier			-60	2.5	dB
Luminance / chrominance delay			10	2.5	ns

ESD COMPLIANCE

Pins	Test	Test Levels	Notes
All pins	Human body model	2kV on 100pF through 1k5Ω	Meets Mil-Std-883 Class 2
All pins	Machine model	200V on 200pF through 0Ω & 500nH	

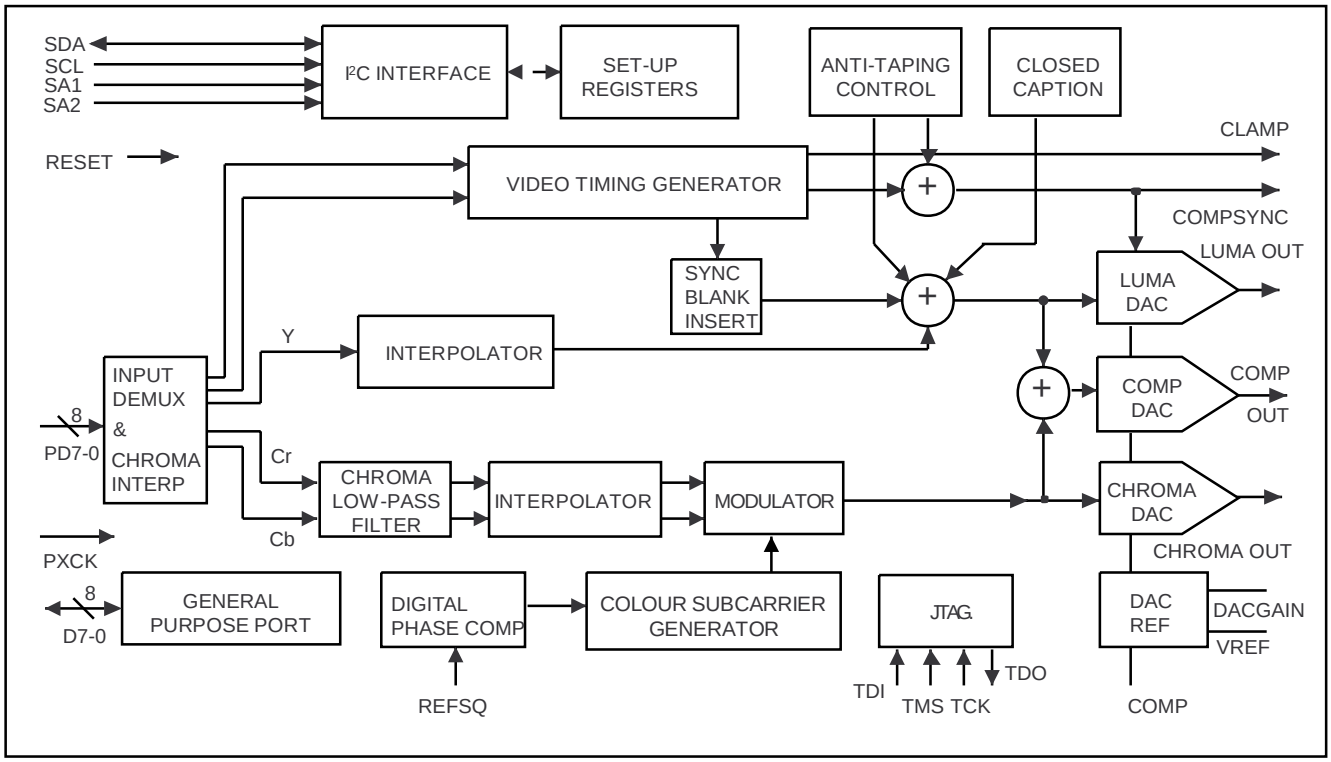

Figure 2 VP531E Functional block diagram, VP551E is identical except there is no Anti-Taping Control

PIN DESCRIPTIONS

Pin Name	Pin No.	Description
PD0-7	39 - 46	8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit, corresponding to Pin 46. These pins are internally pulled low.
D0-7	3 - 10	8 Bit General Purpose Port input/output. D0 is the least significant bit, corresponding to Pin 3. These pins are internally pulled low.
PXCK	15	27MHz Pixel Clock input. The VP531 internally divides PXCK by two to provide the pixel clock.
CLAMP	17	The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC; lines 6-310 and 319-623 for PAL-B,D, G,I,N(Argentina)).
COMPSYNC	18	Composite sync pulse output. This is an active low output signal.
TDO	21	JTAG Data scan output port.
TDI	22	JTAG Data scan input port.
TMS	23	JTAG Scan select input.
TCK	24	JTAG Scan clock input.
SA1	26	Slave address select.
SA2	27	Slave address select.
SCL	28	Standard I^2C bus serial clock input.
SDA	30	Standard I^2C bus serial data input/output.
$\overline{\text{RESET}}$	34	Master reset. This is an asynchronous active low input signal and must be asserted for a minimum of 200ns in order to reset the VP531/VP551.
REFSQ	35	Reference square wave input used only during Genlock mode.
VREF	50	Voltage reference output. This output is nominally 1·055V and should be decoupled with a 100nF capacitor to GND.
DAC GAIN	51	DAC full sacle current control. A resistor connected between this pin and GND sets the magnitude of the video output current. An internal loop amplifier control a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage.
COMP	52	DAC compensation. A 100nF ceramic capacitor must be connected between pin 52 and pin 53.
LUMAOUT	54	True luminance, true chrominance and inverted composite video signal outputs. These are high impedance current source outputs. A DC path to GND must exist from each of these pins
COMPOUT	56	
CHROMAOUT	58	
NOT USED	60, 61, 64	
VDD	1, 12, 16, 20, 29, 32, 33, 37, 48	Positive supply input. All VDD pins must be connected.
AVDD	53, 59 62, 63	Analog positive supply input. All AVDD pins must be connected.
GND	2, 11, 13, 14, 19, 25, 31, 36, 38, 47	Negative supply input. All GND pins must be connected.
AGND	49, 55, 57	Negative supply input. All AGND pins must be connected.

REGISTERS MAP

See Register Details for further explanations.

ADDRESS hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	BAR	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	W	
00	PART ID2	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	R	13
01	PART ID1	ID0F	ID0E	ID0D	ID0C	ID0B	ID0A	ID09	ID08	R	66
02	PART ID0	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00	R	57
03	REV ID	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	R	05
04	GCR	-	-	YCDELAY	RAMPEN	SLH&V -	-	VFS1	VFS0	R/W	00
05	VOCR	-	CLAMPDIS	CHRBW	SYNCDIS	BURDIS	LUMDIS	CHRDIS	PEDEN	R/W	00
06	HANC	-	-	DFI2	DFI1	DFI0	Reserved	Reserved	ACTREN	*	00
07	ANCID	AN7	AN6	AN5	AN4	AN3	AN2	AN1	PARITY	R/W	00
08	SC_ADJ	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	R/W	9C
09	FREQ2	FR17	FR16	FR15	FR14	FR13	FR12	FR11	FR10	R/W	87
0A	FREQ1	FR0F	FR0E	FR0D	FR0C	FR0B	FR0A	FR09	FR08	R/W	C1
0B	FREQ0	FR07	FR06	FR05	FR04	FR03	FR02	FR01	FR00	R/W	F1
0C	SCHPHM	-	-	-	-	-	-	-	SCH8	R/W	00
0D	SCHPHL	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2	SCH1	SCH0	R/W	00
0E to 1F	Reserved										
20	GPPCTL	CTL7	CTL6	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0	W	FF
21	GPPRD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-
22	GPPWR	WR7	WR6	WR5	WR4	WR3	WR2	WR1	WR0	W	00
23 to EF	Not used										
F0 to F7	Reserved										
F8	HSOFFL	HSOFF7	HSOFF6	HSOFF5	HSOFF4	HSOFF3	HSOFF2	HSOFF1	HS0FF0	R/W	7E
F9	HSOFFM	-	-	-	-	-	-	HSOFF9	HSOFF8	R/W	00
FB	SLAVE1	NCORSTD	VBITDIS	VSMODE	F_SWAP	SL_HS1	SL_HS0	HCNT9	HCNT8	R/W	00
FC	SLAVE2	HCNT7	HCNT6	HCNT5	HCNT4	HCNT3	HCNT2	HCNT1	HCNT0	R/W	00
FD	GPSDAC			REGISTER	RESERVED	FOR	TEST			R/W	
FE	GPSTST			REGISTER	RESERVED	FOR	TEST			R/W	
FF	GPSCTL	FSC4SEL	GENDITH	GENLKEN	NOLOCK	PALIDEN	TSURST	CHRMCLIP	TRSEL	R/W	00

Table.1 Register map

NOTE * For register HANC, bits 3, 4 and 5 are read only. Bits 1 and 2 are reserved. N/A = not applicable.
For register PART ID0 the VP551 value is AA

Standard	Lines/ field	Field freq. HZ	Number of pixels/line at 27MHz	Horizontal freq. kHz. f_H	Subcarrier freq. kHz. f_{SC}	f_{SC}/f_H	SC_ADJ register hex	FREQ2-0 registers hex
NTSC (default)	525	59.94	1716	15.734266	3.57954545	(455/2)	xx	87 C1 F1
PAL-B, D, G, H, I	625	50	1728	15.625000	4.43361875	(1135/4+1/625)	9C	A8 26 2B
PAL-N (Argentina)	625	50	1728	15.625000	3.58205625	(917/4+1/625)	57	87 DA 51

Table.2 Line, field and subcarrier standards and register settings

xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = (2^{26} \times f_{SC}/f_H) / (\text{number of pixels/line}) \quad \text{hex}$$

NTSC value is rounded UP from the decimal number. PAL-B, D, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, D, G, H, I, is different to the default state of the register.
In NTSC the NCO is reset at the end of every line, this can be disabled by setting the NCORSTD bit in SLAVE1, this allows the VP531/VP551 to cope with line lengths that are not exactly as specified in REC656.

REGISTER DETAILS

BAR **Base register**
RA7-0 Register address.

PART ID 2-0 **Part number**
ID17-00 Chip part identification (ID) number.

REV ID **Revision number**
REV7-0 Chip revision ID number.

GCR **Global Control**
YCDELAY Luma to Chroma delay.
High = 37ns luma delay, this may be used to compensate for group delay in external filters.
Low = normal operation (default).

RAMPEN Modulated ramp enable.
High = ramp output for differential phase and gain measurements. A 27MHz clock must be applied to PXCK pin.
Low = normal operation (default).

SL_HS_VS 1 = Slave to HS and VS inputs

VFS1-0 Video format select

VFS1	VFS0	
0	0	NTSC (default)
0	1	PAL-B,D,G,H,I,N(Argentina)
1	0	Reserved
1	1	Reserved

VOCR **Video Output Control**
CLAMPDIS High = Clamp signal disable
Low = normal operation with clamp signal enabled (default).

CHRBW Chroma bandwidth select.
High = ±1·3MHz.
Low = ±650kHz (default)

SYNCDIS High = Sync disable (in composite video signal). COMPSYNC is not affected.
Low = normal operation with sync enabled (default).

BURDIS High = Chroma burst disable.
Low = normal operation, with burst enabled (default).

LUMDIS High = Luma input disable - force black level with synchronisation pulses maintained.
Low = normal operation, with Luma input enabled (default).

CHRDIS High = Chroma input disable - force monochrome.
Low = normal operation, with Chroma input enabled (default).

PEDEN High = Pedestal (set-up) enable a 7·5 IRE pedestal on lines 23-262 and 286-525. Valid for NTSC only

HANC **Horizontal Ancillary Data Control**
DFI2-0(read only) Digital Field Identification, 000=Field1
ANCTREN Ancillary timing reference enable. When High use FIELD COUNT from ancillary data stream. When low, data is ignored.

ANCID **Ancillary data ID**
AN7-1 Ancillary data ID
AN0 Parity bit (odd)
Only ancillary data in REC 656 data stream with the same ID as this byte will be decoded by the VP531/VP551 to produce H and V synchronisation and FIELD COUNT.

SC_ADJ **Sub Carrier Adjust**
SC7-0 Sub carrier frequency seed value, see table 2.

FREQ2-0 **Sub carrier frequency**
FR17-00 24 bit Sub carrier frequency programmed via I^2C bus, see table 2. FREQ2 is the most significant byte (MSB).

SCHPHM-L **Sub carrier phase offset**
SCH9-0 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB. The nominal value is zero. This register is used to compensate for delays external to the VP531/VP551.

GPPCTL **General purpose port control**
CTL7-0 Each bit controls port direction
Low = output High = input

GPPRD **General purpose port read data**
RD7-0 I^2C bus read from general purpose port (only INPUTS defined in GPPCTL)

GPPWR **General purpose port write data**
WR7-0 I^2C bus write to general purpose port (only OUTPUTS defined in GPPCTL)

HSOFFM-L **HS offset**
HSOFF9-0 This is a 10 bit number which allows the user to offset the start of digital data input with reference to the pulse HS.

SLAVE1 **H &V Slave mode control register**
NCORSTD 1 = NCO Line Reset Disable (NTSC only)

VBITDIS 0 = Video blanked when Rec601 V bit set
1 = V bit is ignored
F_SWAP The odd and even fields are swapped
SL_HS1-0 Selects pixel sample (1 to 4)
HCNT9-8 As HCNT7-0 but MSBs

SLAVE2 **H &V Slave position register**

HCNT7-0 Adjusts for delay at which pixel data occurs relative to HS

GPSCTL **GPS Control**

FSC4SEL When high, REFSQ = 4xFSC and GPP bit D6 is forced to become an input for a SCSYNC signal (high = reset), which provides a synchronous phase reset for FSC divider. Low = normal operation with REFSQ = 1xFSC. (default).

GENDITH 1 = Gen lock dither added.

GENLKEN High = enable Genlock to REFSQ signal input.
Low = internal subcarrier generation (default).

NOLOCK Genlock status bit (read only)
Low = Genlocked.
High = cannot lock to REFSQ. This bit is cleared by reading and set again if lock cannot be attained.

PALIDEN High = enable external PAL ID phase control and GPP bit D7 is forced to become an input for PAL ID switch signal, (GPP bit D7 - Low = +135°, High = -135°).
Low = normal operation, internal PAL ID phase switch is used (default).

TSURST High = chip soft reset. Registers are NOT reset to default values.
Low = normal operation (default).

CHRMCLIP High = enable clipping of chroma data when luma goes below black level and is clipped.
Low = no chroma clipping (default).

TRSEL High = master mode, GPP bits D0 - 4 are forced to become a video timing port with VS, HS and FIELD outputs.
Low = slave mode, timing from REC656.

I²C BUS CONTROL INTERFACE

I²C bus address

A6	A5	A4	A3	A2	A1	A0	R/ $\overline{W}$
0	0	0	1	1	SA2	SA1	X

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pins SA1 and SA2. This allows the device to respond to one of four addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read / $\overline{\text{write}}$ for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP531/VP551. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP531/VP551 generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following:
NTSC,
PAL B, D, G, H, I, N (Argentina).

TRS - Slave mode

The VP531 has an internal timing generator which produces video timing signals appropriate to the mode of operation. In the default (power up) slave mode, all timing signals are derived from the input clock, PXCK, which must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.

The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal, using timing data (TRS codes) from the Ancillary data stream in the REC656 input signal, (when TRSEL (bit 0 of GPSCTL register) is set low).

Slave H & V mode

H & V slave mode is enabled by setting the SL_H&V bit in the GCR register. In this mode the position of the video syncs is derived from the HS and VS inputs. These GPP pins are automatically configured as inputs when SL_H&V is set to '1'.

This mode requires 262/263 line syncs in NTSC mode (not 262.5/262.5) and 312/313 syncs in PAL. The VSYNC and negative edges HSYNC need to be aligned. When programming the SLH&V bit needs setting first and then the TRSEL bit in reg FF, otherwise there will be a clash of outputs. The VSYNC is input to pin 3 and the HSYNC to pin 4 both at 5V TTL levels.

HCNT

To ensure that the incoming data is sampled correctly a 10 bit binary number (HCNT) has to be programmed into the SLAVE1 and 2 registers. This will allow the device's internal horizontal counter to align with the video data, each bit

represents one 13.5MHz cycle. To calculate this use the formula below:

NTSC/PALM
HCNT = SN + 119 (SN = 0 - 738)
HCNT = SN + 739 (SN = 739 - 857)

PAL
HCNT = SN + 127 (SN = 0 - 738)
HCNT = SN + 737 (SN = 737 - 863)
where SN is Rec. 656/601 sample number on which the negative edge of HSYNC occurs.

SL_HS

A further adjustment is also required to ensure that the correct Cr and Cb sample alignment. The bits SL_HS1-0 allows for four sampling positions in the CbYCrY sequence, failure to set this correctly will mean corruption of the colour or colour being interpreted as luma.

F_SWAP

If the field synchronisation is wrong it can be swapped by setting this bit.

V_SYNC

When set to a '1' this bit allows an odd/even square wave to provide the field synchronisation.

Video Timing - Master sync mode

When TRSEL (bit 0 of GPSCTL register) is set high, the VP531 operates in a MASTER sync mode, all REC656 timing reference codes are ignored and GPP bits D0 - 4 become a video timing port with VS, HS and FIELD outputs. The PXCK signal is, however, still used to generate all internal clocks. When TRSEL is set high, the direction setting of bits 4 - 0 of the GPPCTL register is ignored.

VS is the start of the field sync datum in the middle of the equalisation pulses. HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP531. The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers.

HS offset

The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see figure 4, this is called the pipeline delay and may need adjusting for a particular application. This is done by programming a 10 bit number called HSOFF into the HSOFFM and HSOFFL registers, HSOFFM being the most significant two bits and HSOFFL the least significant eight bits. A default value of 07EH is held in the registers.

The value to program into HSOFF can be looked up in tables 3 &4:

NCK	HSOFF	Comment
0 to 120	126 to 6	HS normal (64 cks)
121 to 138	863 to 801	HS pulse shortened*
184 to 857	800 to 127	HS normal (64 cks)

Table.3 for NTSC

NCK	HSOFF	Comment
0 to 131	137 to 6	HS normal (64 cks)
132 to 194	869 to 807	HS pulse shortened*
195 to 863	806 to 138	HS normal (64 cks)

Table.4 for NTSC and PAL-B, D, G, H, I, N

**HS pulse shortened means that the width of the pulse will be less than the normal 64 13.5MHz clock cycles.*

NCK = number of 13.5MHz clock cycles between the falling edge of HS and Cb0 (first data I/P on PD7-0) see fig. 4. Decreasing HSOFF advances the HS pulse (numbers are in decimal).

The interruption in the sequence of values is because the HS signal is jumping across a line boundary to the previous line as the offset is increased. The register default value is 7EH and this sets Nck to 0, ie. the HS negative edge and Cb0 are co-incident in NTSC mode.

Video Blanking

The VP531/VP551 automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In PAL mode, lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when TRSEL (bit 0 of GPSCTL register) is set low. When in MASTER mode with TRSEL set high the video encoder is still enabled. Therefore if these lines are required to be blank they must have no video signal input.

Interpolator

The luminance and chrominance data are separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Digital to Analog Converters

The VP531/VP551 contains two 9 bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complementary outputs. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.05V (typ.) provides the necessary biasing, if required this can be overridden by an external reference.

The full-scale output currents of the DACs is set by external resistors between the DACGAIN and VSS pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.

By summing the complementary luma and chroma DAC current outputs an inverted composite output is generated. Note that this signal has a DC offset and therefore usually needs to be capacitively coupled. The analog outputs of the VP531/VP551 are capable of directly driving doubly terminated 75Ω co-axial cable. If it is required only to drive a single 75Ω load then DACGAIN resistor is simply doubled.

Luminance, Chrominance and Composite Video Outputs

The Luminance video output (LUMAOUT pin 54) drives a 37.5Ω load at 1.0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level (pedestal) offset can be added during the active video portion of the raster. The pedestal is programmed by PEDEN bit in VOCR register.

The Chrominance video output (CHROMAOUT pin 58) drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5Ω load. Burst is injected with the appropriate timing relative to the luma signal.

The inverted composite video output (COMPOUTB pin 56) will also drive a 37.5Ω loas at 1.0V, sync tip to peak white. It contains both the luminance and chrominance content of the signal plus the composite sync pulses.

Output sinx/x compensation filters are required on all video output, as shown in the typical application diagram, see figs. 6 & 7.

Genlock using REFSQ input

The VP531/VP551 can be Genlocked to another video source by setting GENLKEN high (in GPSCTL register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier. But by setting FSC4SEL high (in GPSCTL register), a 4 x sub carrier frequency signal may be input to REFSQ. In this case, the Genlock circuit can be reset to the required phase of REFSQ, by supplying a pulse to SCSYNC (pin 9). The frequency of SCSYNC can be at sub carrier frequency, but once per line, or once per field could be adequate, depending on the application. When GENLKEN is SET high, the direction setting of bit 6 of the GPPCTL register is ignored.

PALID Input

When in Genlock mode with GENLKEN set high (in GPSCTL register), the VP531 requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input (pin 10), High = -135° and low = +135°. The signal is asynchronous and should be changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GPSCTL register). When GENLKEN is high, the direction setting of bit 7 of the GPPCTL register is ignored

Master Reset

The VP531/VP551 must be initialised with the $\overline{\text{RESET}}$ pin 34. This is an asynchronous active low signal and must be active for a minimum of 200ns in order for the VP531 to be reset. The device resets to line 64, start of horizontal sync (i.e. line blanking active). There is no on-chip power on reset circuitry.

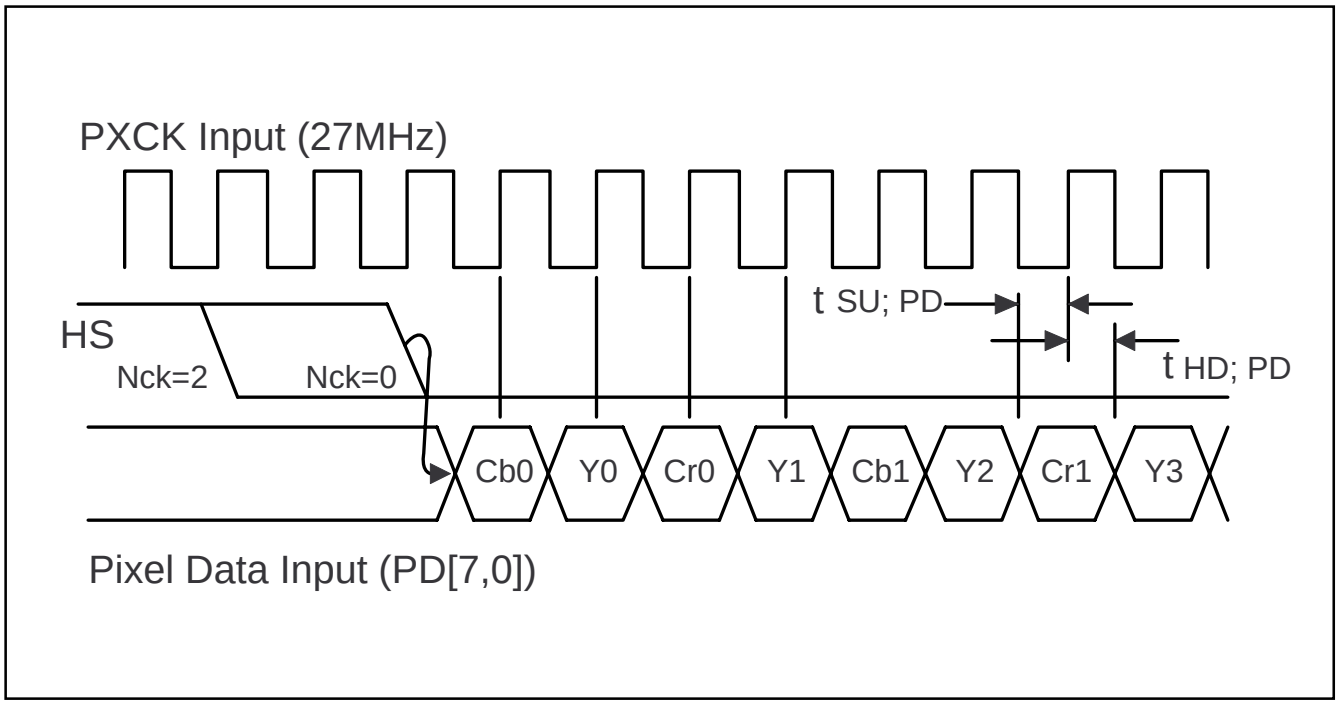

Figure 3 REC 656 interface with HS output timing

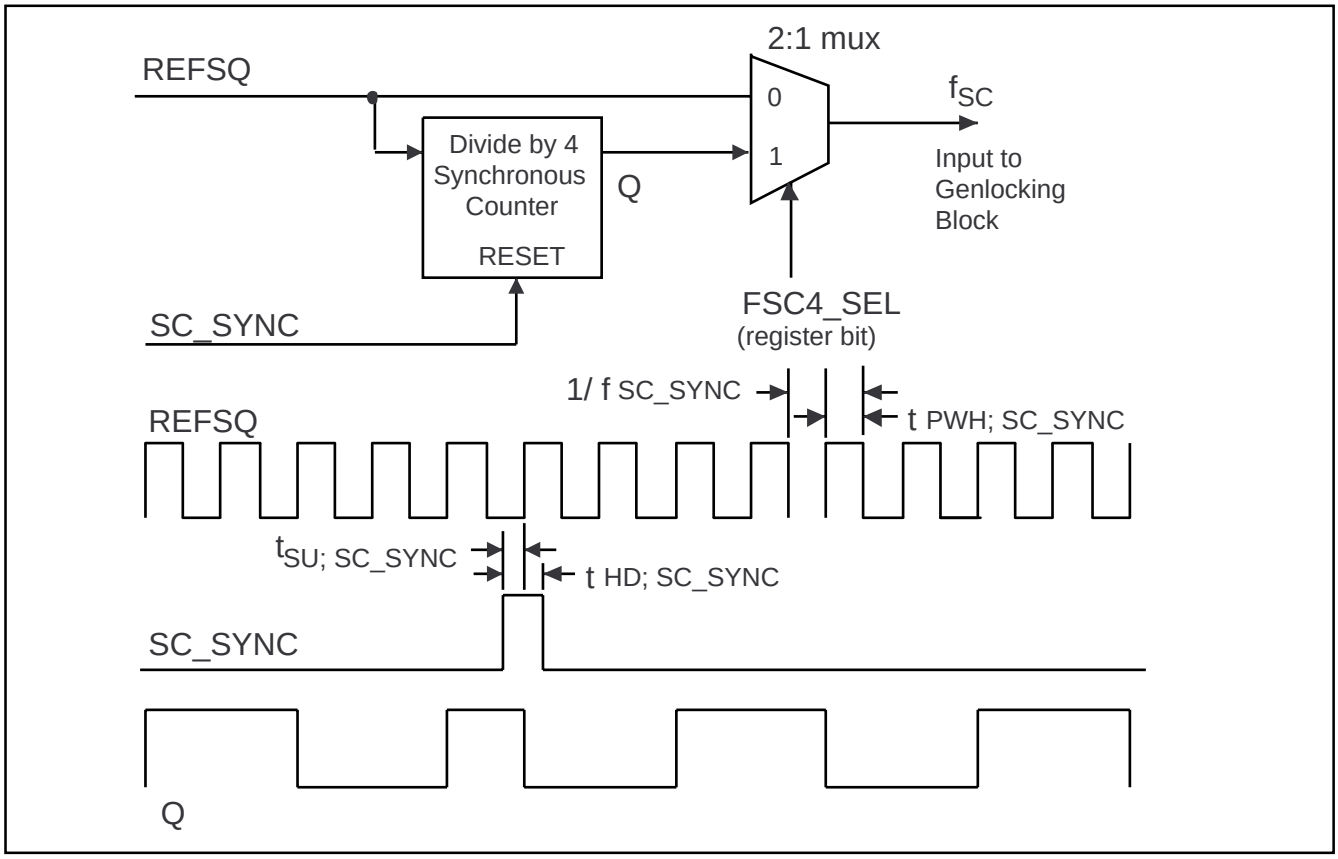

Figure 4 REFSQ and SC_SYNC input timing

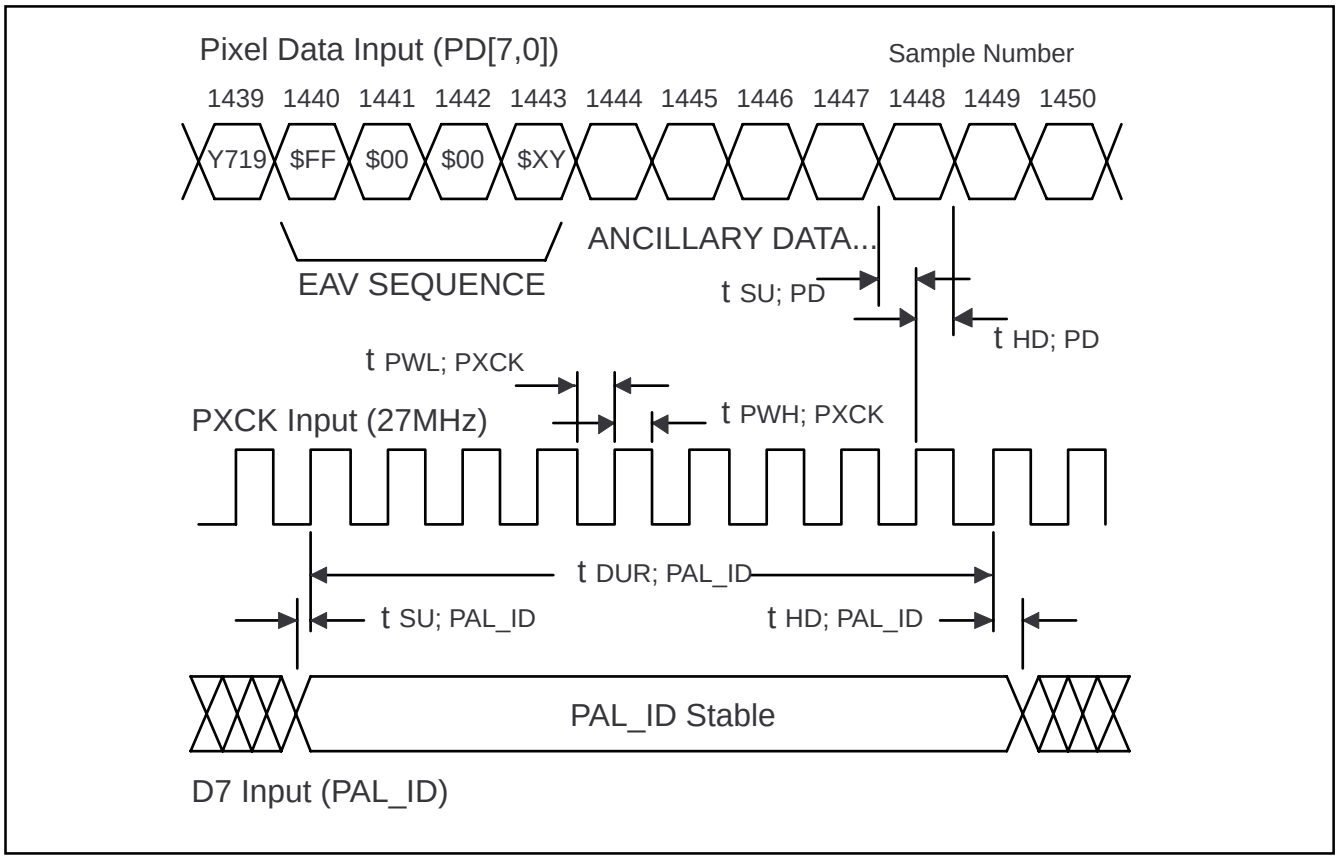

Figure 5 PAL_ID input timing

TIMING INFORMATION

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Units
Master clock frequency (PXCK input)		f_{PXCK}		27.0		MHz
PXCK pulse width, HIGH		$t_{PWH;\ PXCK}$	10			ns
PXCK pulse width, LOW		$t_{PWL;\ PXCK}$	14.5			ns
PXCK rise time	10% to 90% points	t_{RP}			TBD	ns
PXCK fall time	90% to 10% points	t_{FP}			TBD	ns
PD7-0 set up time		$t_{SU;PD}$	10			ns
PD7-0 hold time		$t_{HD;PD}$	5			ns
SC_SYNC set up time		$t_{SU;SC\_SYNC}$	10			ns
SC_SYNC hold time		$t_{HD;SC\_SYNC}$	0			ns
PAL_ID set up time		$t_{SU;PAL\_ID}$	10			ns
PAL_ID hold time		$t_{HD;PAL\_ID}$	0			ns
PAL_ID duration		$t_{DUR;PAL\_ID}$	9			PXCK periods
Output delay	PXCK to COMPSYNC PXCK to CLAMP	t_{DOS}			25	ns

Note: Timing reference points are at the 50% level. Digital C_{LOAD} <40pF.

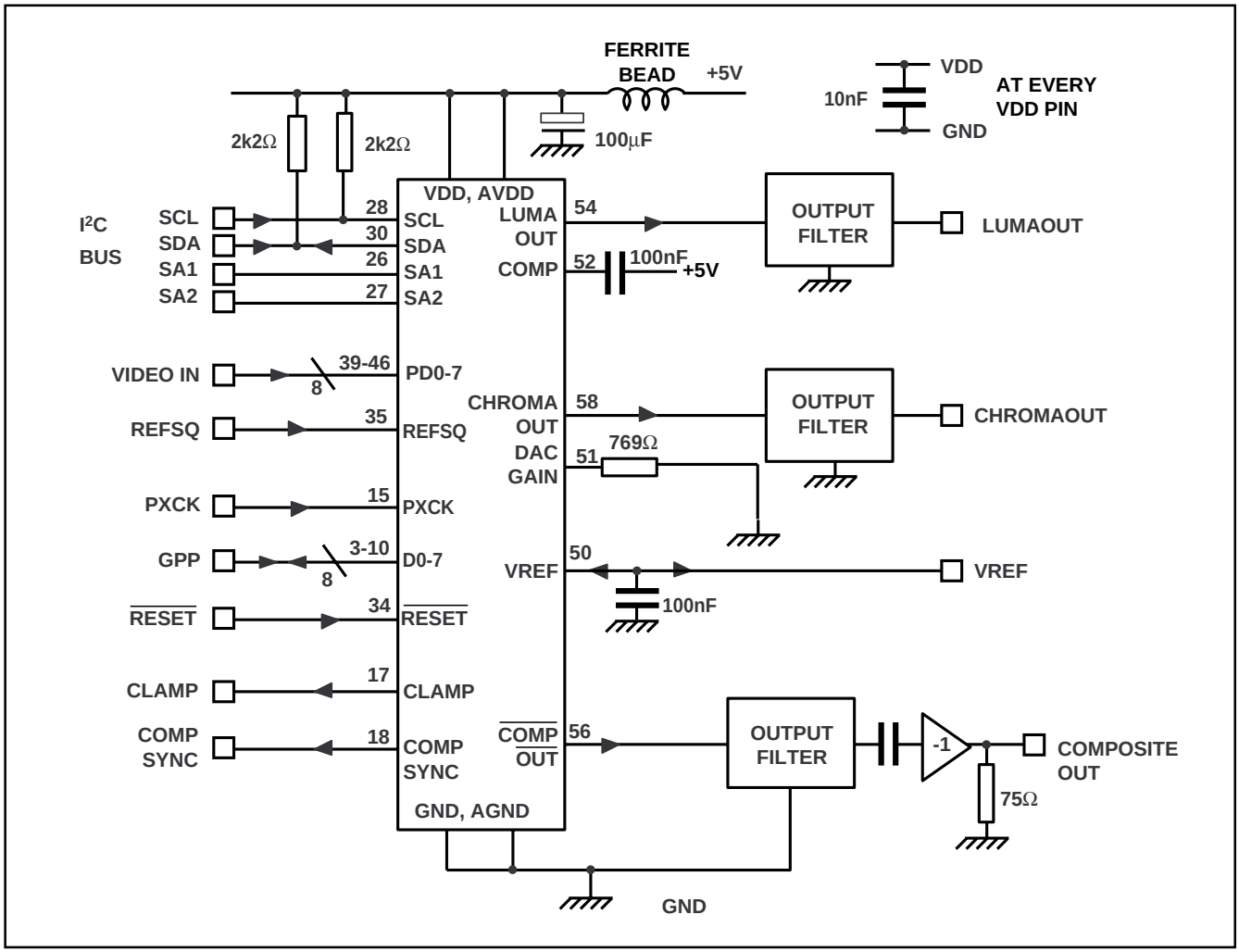

Figure 6 Typical application diagram, SLAVE mode. (Output filter - see Fig.7)

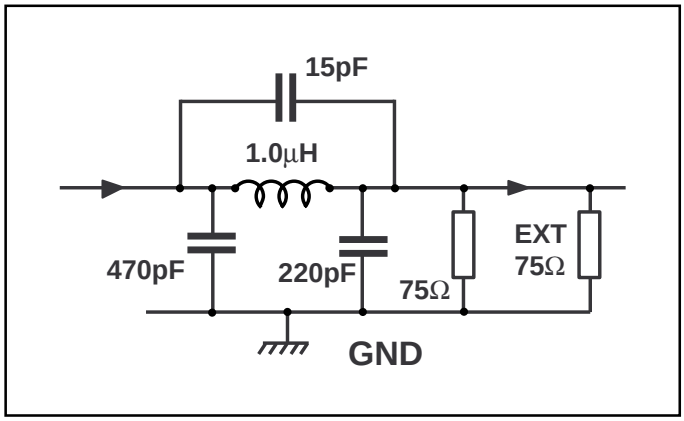

Figure 7 Output reconstruction filter

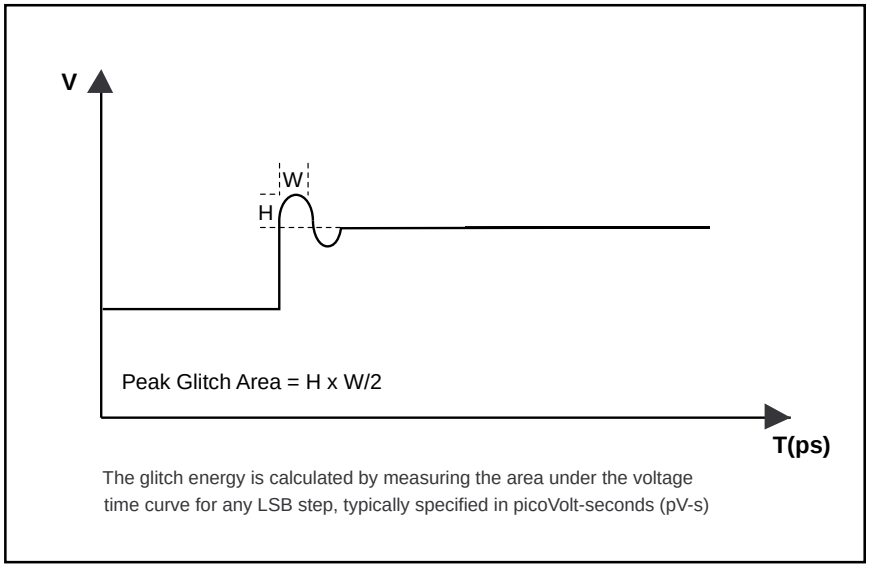

Figure 8 Glitch Energy

Note:
The VP531 is only available to customers with a valid and existing authorisation to purchase issued by MACROVISION CORPORATION.

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