

74HC3GU04

Inverter

Rev. 03 — 11 May 2009

Product data sheet

1. General description

The 74HC3GU04 is a high-speed Si-gate CMOS device. This device provides three inverter gates with unbuffered outputs.

The 74HC3GU04 has CMOS input switching levels and supply voltage range 2 V to 6 V.

2. Features

- Wide supply voltage range from 2.0 V to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low-power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC3GU04DP	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC3GU04DC	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HC3GU04GD	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body $3 \times 2 \times 0.5$ mm	SOT996-2

4. Marking

Table 2. Marking

Type number	Marking code
74HC3GU04DP	HU04
74HC3GU04DC	HU4
74HC3GU04GD	HU4

5. Functional diagram

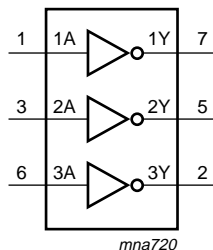


Fig 1. Logic symbol

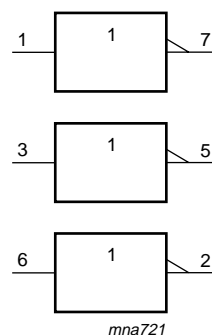


Fig 2. IEC logic symbol

6. Pinning information

6.1 Pinning

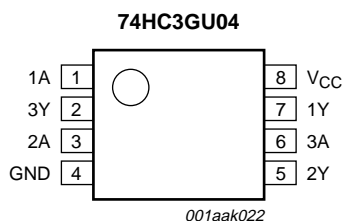


Fig 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

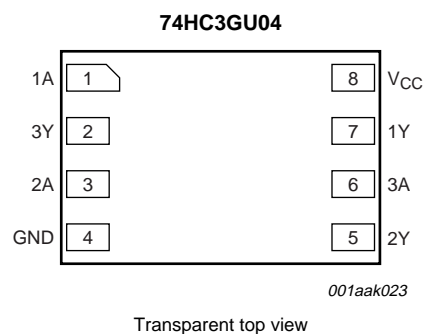


Fig 4. Pin configuration SOT996-2 (XSON8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
1Y, 2Y, 3Y	7, 5, 2	data output
GND	4	ground (0 V)
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table [1]

Input	Output
nA	nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	[1] -	± 25	mA
I_{CC}	quiescent supply current		[1] -	50	mA
I_{GND}	ground current		[1] -50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[2] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
 For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.
 For XSON8U package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.7	1.1	-	1.7	-	V
		V _{CC} = 4.5 V	3.6	2.4	-	3.6	-	V
		V _{CC} = 6.0 V	4.8	3.1	-	4.8	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.9	0.3	-	0.3	V
		V _{CC} = 4.5 V	-	2.1	0.9	-	0.9	V
		V _{CC} = 6.0 V	-	2.9	1.2	-	1.2	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
	I _O = -5.2 mA; V _{CC} = 6.0 V	5.63	5.81	-	5.2	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
	I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V	
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	-	±1.0	μA
I _{CC}	supply current	per input pin; V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	μA
C _I	input capacitance		-	3.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 5 ^[2]						
		V _{CC} = 2.0 V	-	13	75	-	90	ns
		V _{CC} = 4.5 V	-	6	15	-	18	ns
		V _{CC} = 6.0 V	-	5	13	-	15	ns

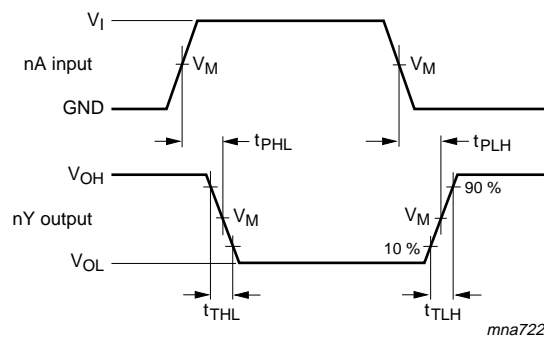
Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_t	transition time	nY; see Figure 5						
		$V_{CC} = 2.0\text{ V}$	-	18	95	-	125	ns
		$V_{CC} = 4.5\text{ V}$	-	6	19	-	25	ns
		$V_{CC} = 6.0\text{ V}$	-	5	16	-	20	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$	-	5	-	-	-	pF

- [1] All typical values are measured at $T_{amb} = 25\text{ °C}$.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_t is the same as t_{TLH} and t_{THL} .
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
- $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
- f_i = input frequency in MHz;
 - f_o = output frequency in MHz;
 - C_L = output load capacitance in pF;
 - V_{CC} = supply voltage in V;
 - N = number of inputs switching;
 - $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms

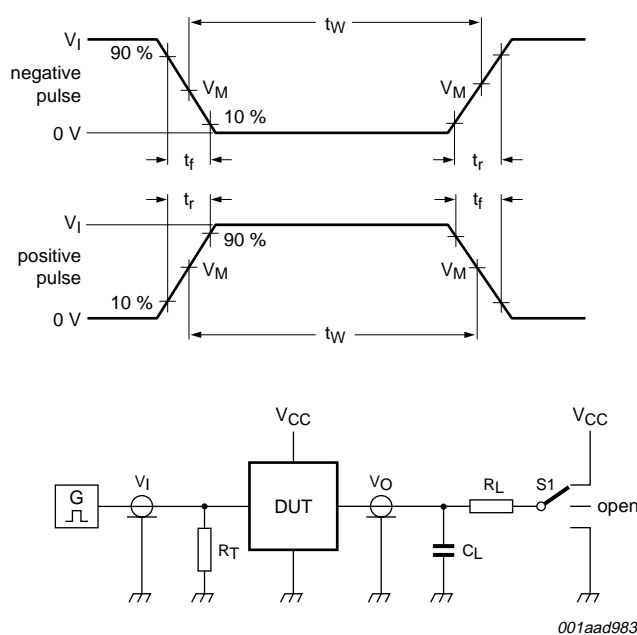


Measurement points are given in [Table 9](#).

Fig 5. Propagation delay data input (nA) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC3GU04	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

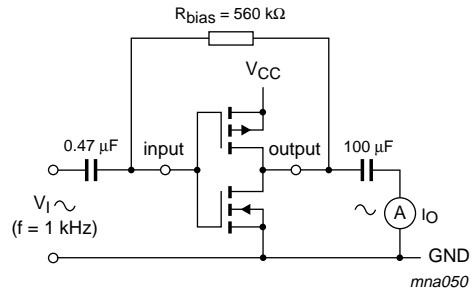
S1 = Test selection switch.

Fig 6. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC3GU04	GND to V_{CC}	≤ 6 ns	50 pF	1 k Ω	open

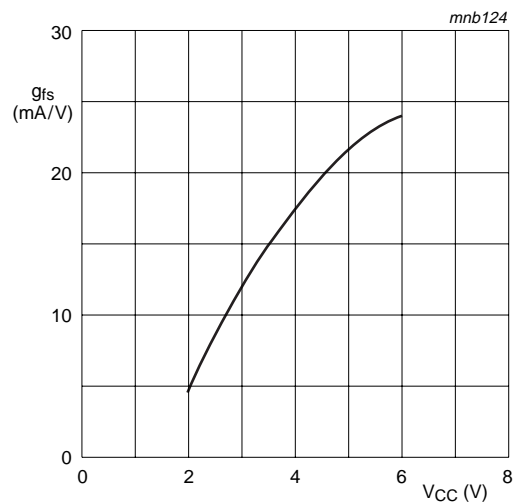
12.1 Additional characteristics



$$g_{fs} = \frac{\Delta I_o}{\Delta V_i}$$

V_O is constant.

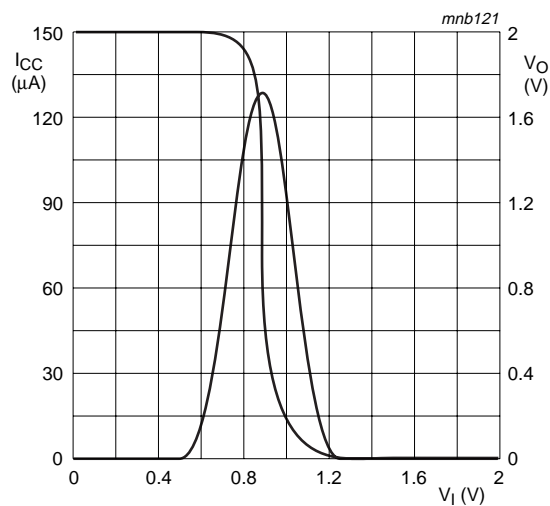
Fig 7. Test set-up for measuring forward transconductance



$T_{amb} = 25\text{ }^{\circ}\text{C}$.

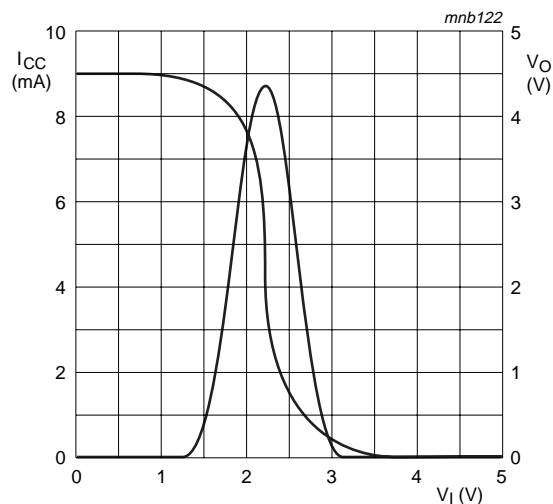
Fig 8. Typical forward transconductance as a function of supply voltage

13. Typical transfer characteristics



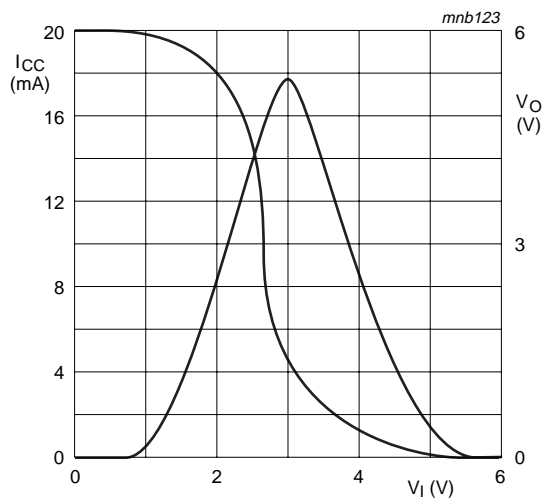
$V_{CC} = 2.0\text{ V}; I_O = 0\text{ A}$.

Fig 9. Typical transfer characteristics $V_{CC} = 2.0\text{ V}$



$V_{CC} = 4.5\text{ V}; I_O = 0\text{ A}$.

Fig 10. Typical transfer characteristics $V_{CC} = 4.5\text{ V}$



$V_{CC} = 6.0\text{ V}; I_O = 0\text{ A}$.

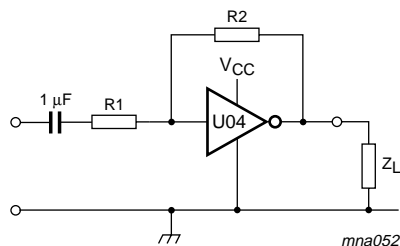
Fig 11. Typical transfer characteristics $V_{CC} = 6.0\text{ V}$

14. Application information

Some applications for the 74HC3GU04 are:

- Linear amplifier (see [Figure 12](#))
- Crystal oscillator (see [Figure 14](#)).

Remark: All values given are typical values unless otherwise specified.



$Z_L > 10 \text{ k}\Omega$.

$R1 \geq 3 \text{ k}\Omega$.

$R2 \leq 1 \text{ M}\Omega$.

Open loop amplification: $A_{OL} = 20$ (typical).

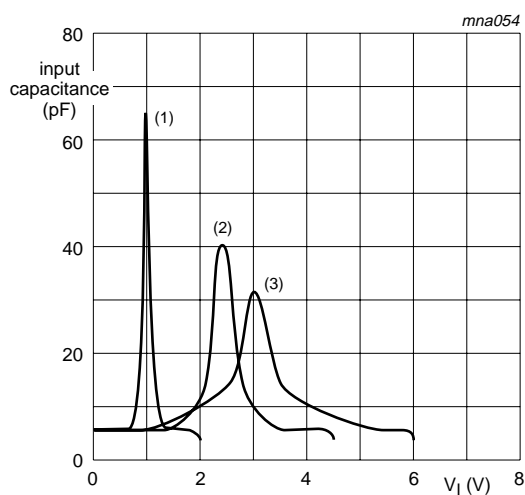
$$\text{Voltage amplification: } A_V = -\frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})}$$

$V_{o(p-p)} = V_{CC} - 1.5 \text{ V}$ centered at $0.5 \times V_{CC}$.

Unity gain bandwidth product is 5 MHz (typical).

Input capacitance see [Figure 13](#).

Fig 12. Linear amplifier application

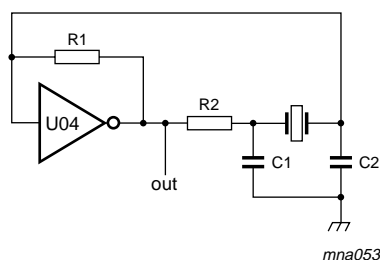


(1) $V_{CC} = 2.0 \text{ V}$.

(2) $V_{CC} = 4.5 \text{ V}$.

(3) $V_{CC} = 6.0 \text{ V}$.

Fig 13. Typical input capacitance as a function of the input voltage



Test data is given in [Table 11](#) and [Table 12](#).

C1 = 47 pF (typical).

C2 = 22 pF (typical).

R1 = 1 M Ω to 10 M Ω (typical).

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} ($I_{CC} = 2$ mA at $V_{CC} = 3.0$ V and $f = 1$ MHz)

Fig 14. Crystal oscillator application

Table 11. External components for resonator ($f < 1$ MHz)

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	2.2 M Ω	220 k Ω	56 pF	20 pF
16 kHz to 24.9 kHz	2.2 M Ω	220 k Ω	56 pF	10 pF
25 kHz to 54.9 kHz	2.2 M Ω	100 k Ω	56 pF	10 pF
55 kHz to 129.9 kHz	2.2 M Ω	100 k Ω	47 pF	5 pF
130 kHz to 199.9 kHz	2.2 M Ω	47 k Ω	47 pF	5 pF
200 kHz to 349.9 kHz	2.2 M Ω	47 k Ω	47 pF	5 pF
350 kHz to 600 kHz	2.2 M Ω	47 k Ω	47 pF	5 pF

Table 12. Optimum value for R2

Frequency	R2	Optimum
3 kHz	2.0 k Ω	minimum required I_{CC}
	8.0 k Ω	minimum influence due to change in V_{CC}
6 kHz	1.0 k Ω	minimum required I_{CC}
	4.7 k Ω	minimum influence by V_{CC}
10 kHz	0.5 k Ω	minimum required I_{CC}
	2.0 k Ω	minimum influence by V_{CC}
14 kHz	0.5 k Ω	minimum required I_{CC}
	2.0 k Ω	minimum influence by V_{CC}
> 14 kHz	replace R2 by C3 = 35 pF (typical)	

15. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

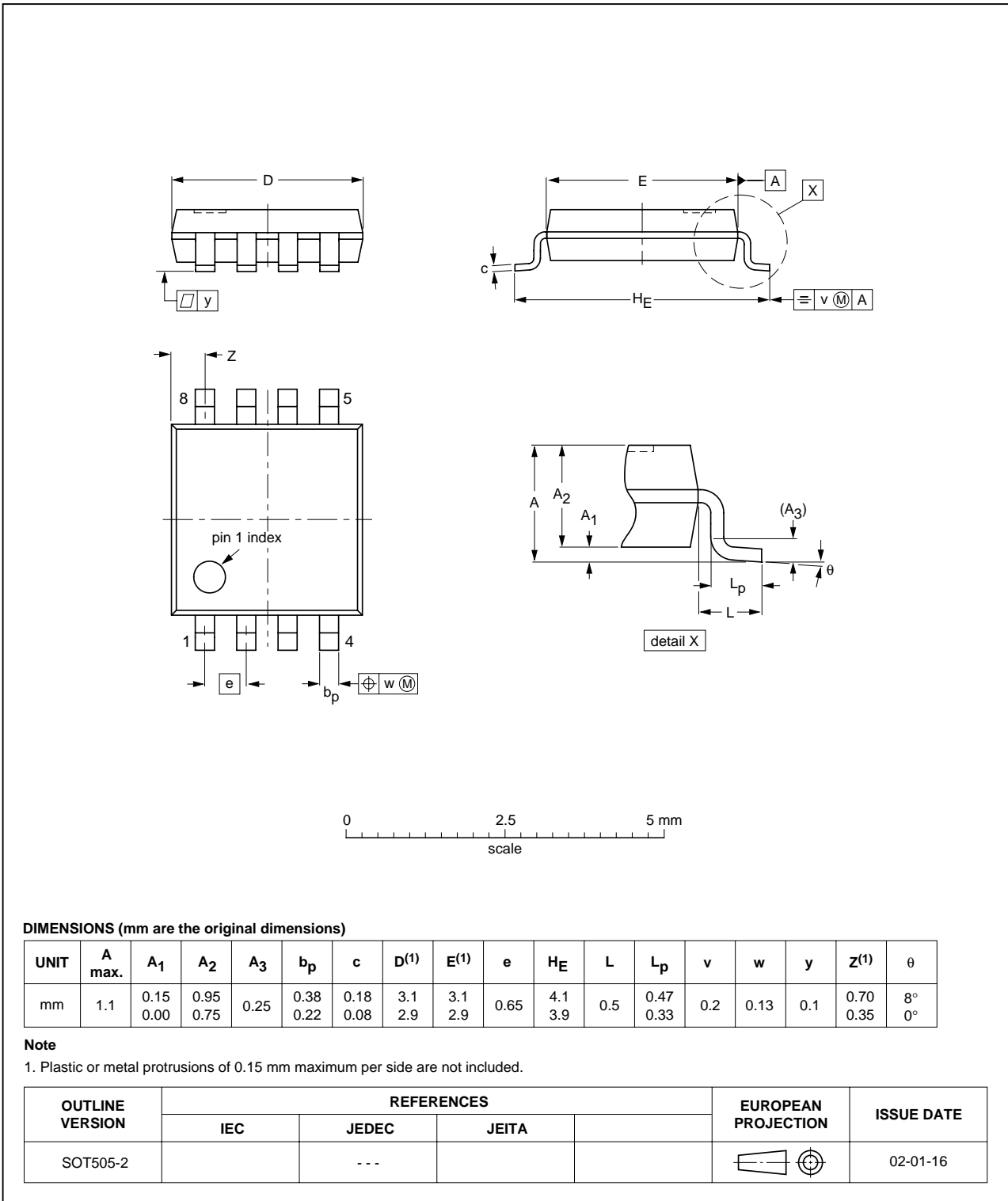


Fig 15. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

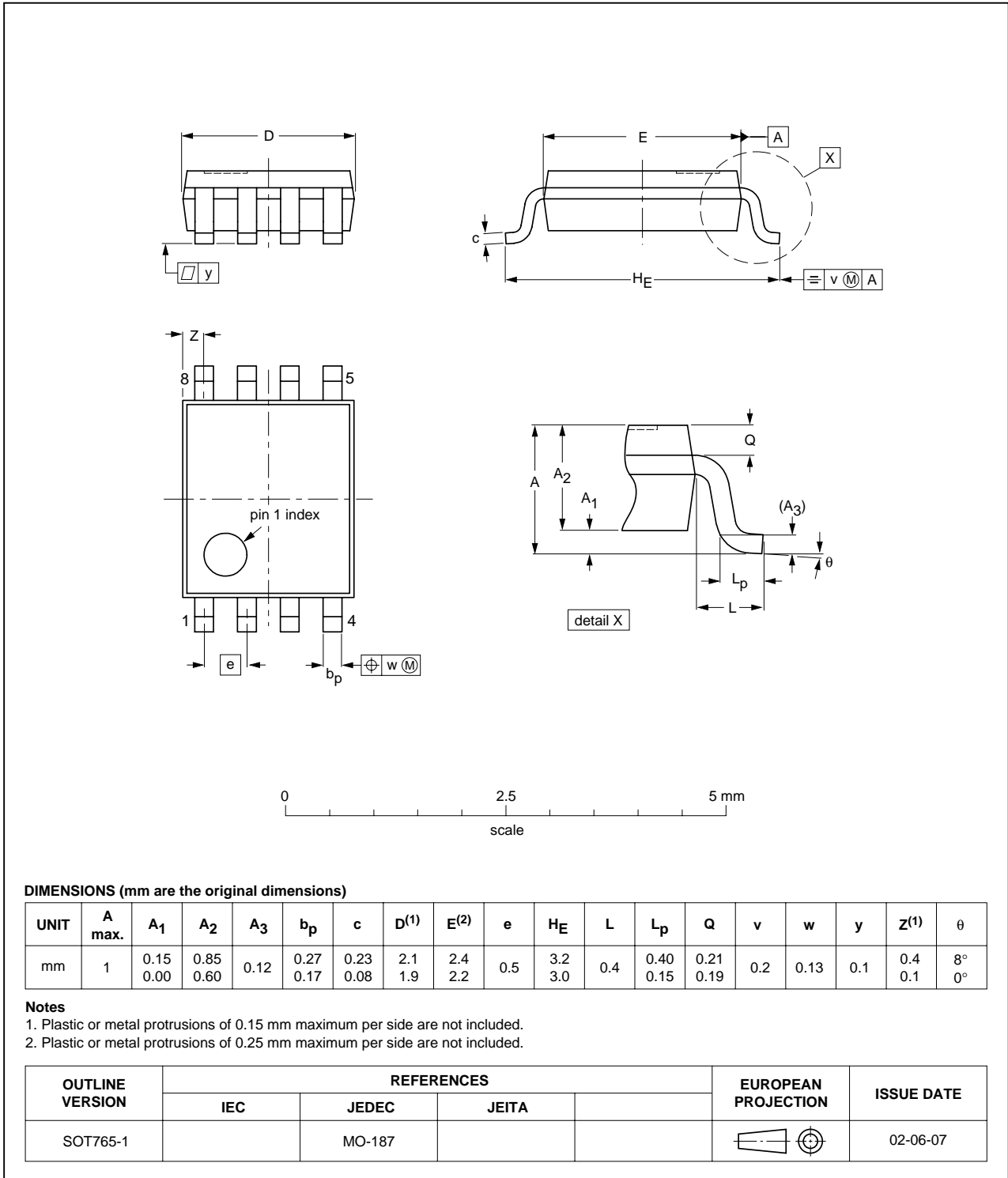


Fig 16. Package outline SOT765-1 (VSSOP8)

XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm

SOT996-2

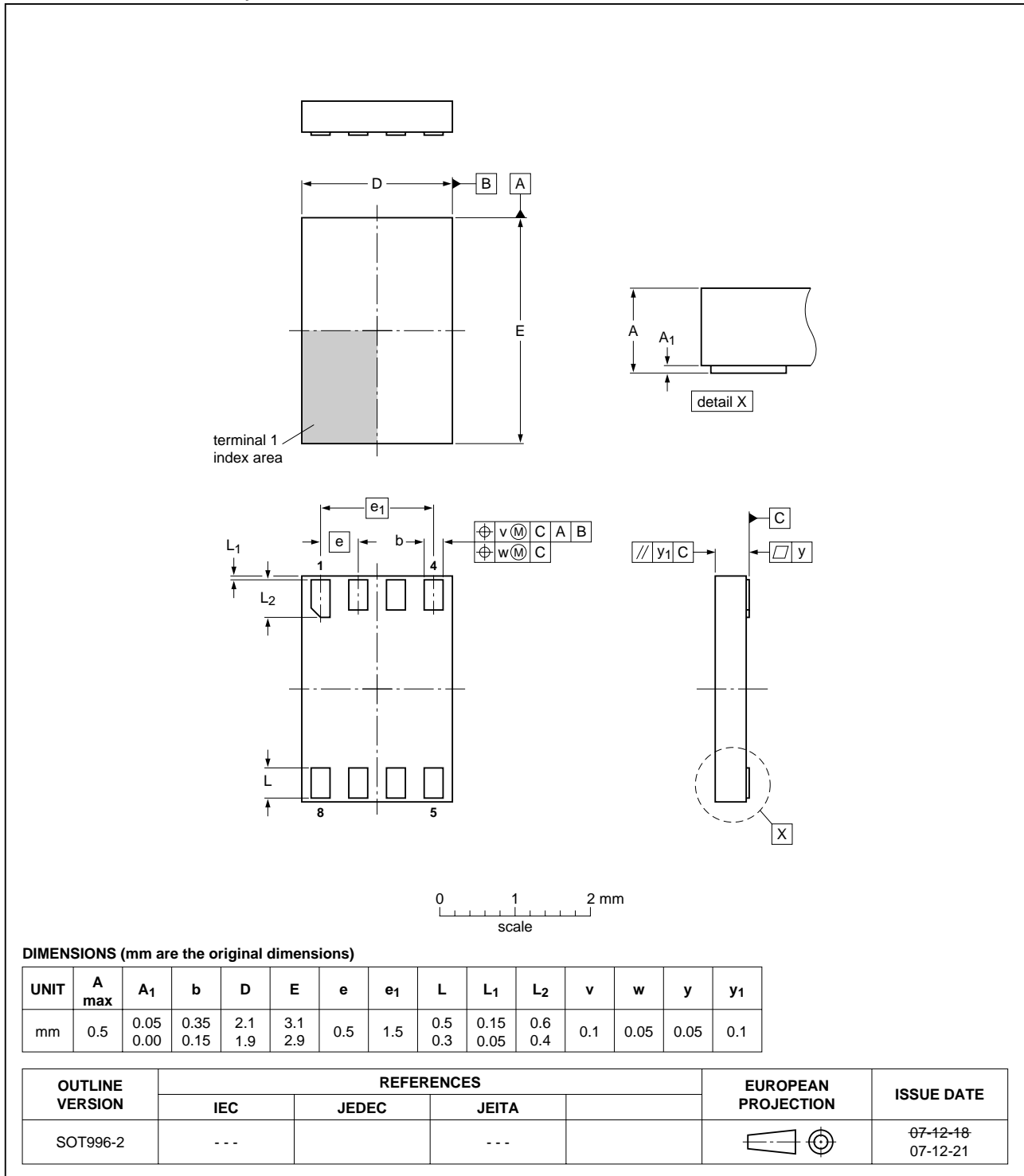


Fig 17. Package outline SOT996-2 (XSON8U)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC3GU04_3	20090511	Product data sheet	-	74HC3GU04_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Added type number 74HC3GU04GD (XSON8U package) 			
74HC3GU04_2	20031126	Product specification	-	74HC3GU04_1
74HC3GU04_1	20030818	Product specification	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 11 May 2009

Document identifier: 74HC3GU04_3