array MICROSYSTEMS **Data Sheet** **a66212**

Rev 1.2 - 03/93

Programmable array Controller (PaC)

T-52-33-55

The Programmable array Controller (PaC) is designed to operate with the Digital array Signal Processor (DaSP) and the other members of array Microsystems' a66 family of products to provide a very high performance DSP processing system. The DaSP/PaC chip set is specifically designed to fulfill the numerical processing, memory address generation, program sequencing and storage requirements of very high performance, real time DSP systems, especially those involving the computation of the Fast Fourier Transform (FFT). The PaC is used to generate memory addresses in such a DSP system and readily supports the overlapping of complex input/output data transfers with data processing. The PaC also contains an instruction memory for holding the user's DSP program, and can either be hosted from a control processor or run in a stand-alone configuration. While this data sheet will provide internal architecture and timing information, the designer is strongly encouraged to read the **PaC User's Guide** for further information.

The a66212 supercedes the a66211 Programmable array Controller.

FEATURES:

- Full address generation capability for radix-2, radix-4, and mixed radix-2/radix-4 FFTs of up to 64K complex or 128K real points.
- Simultaneously generates up to five 16 bit addresses to both I/O buffer and data processing memories to permit full overlapping and synchronization of I/O transfers with data processing.
- Overlap/discard address generation for supporting real-time frequency domain FIR filtering.
- 32 word instruction store for holding DSP program.
- Commercial temperature range parts are available in 30 MHz and 40 MHz speed grades.
- Military and industrial temperature range parts are available in 30 MHz speed grades.
- 144 pin PGA package.
- 2W typical power dissipation.

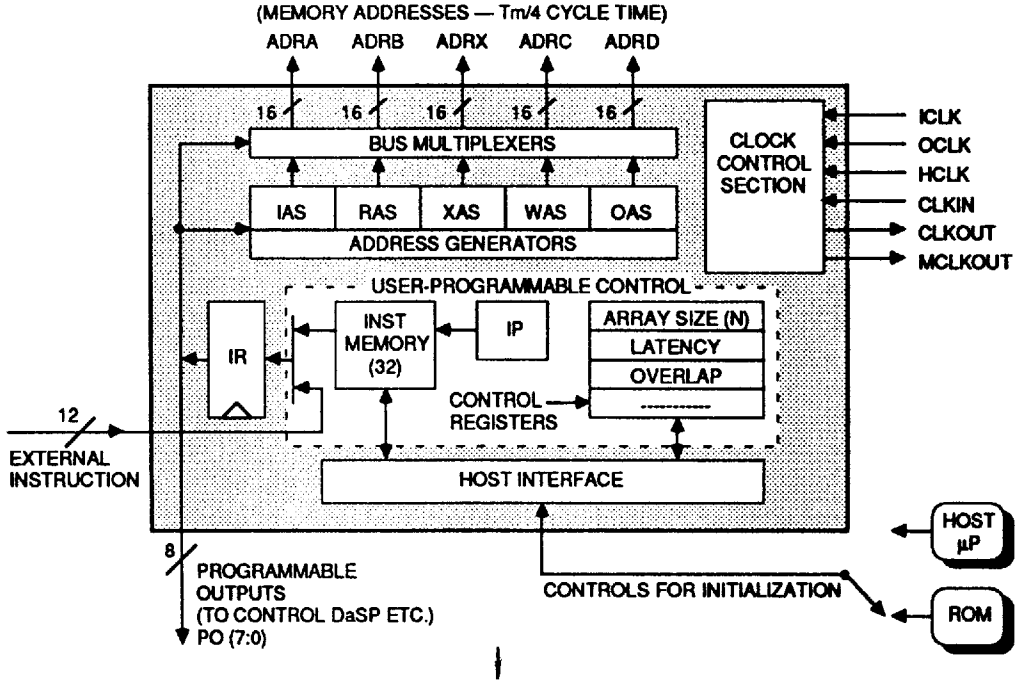
APPLICATIONS:

- Radar
- Sonar
- EW/ECM
- Digital Radio
- Test Instruments
- Medical Instruments
- Spectrum Analyzers
- Transmultiplexing
- Image Processing
- Image Compression
- Image Reconstruction
- Spread Spectrum Communications

RELATED PRODUCTS:

- Digital array Signal Processor (DaSP): a66111
- Reconfigurable array Store (RaS): a66311
- Memory Modules: a664XX

FUNCTIONAL BLOCK DIAGRAM:



FUNCTIONAL DESCRIPTION:

General Information

The Programmable array Controller (PaC) is designed to be used with array Microsystems' Digital array Signal Processor (DaSP) and the Reconfigurable array Store (RaS), array's memory modules, or off-the-shelf static RAMs to implement very high performance array processing systems for DSP applications. In such systems, the PaC typically satisfies all memory address generation and program storage requirements while the DaSP performs all data processing. The DaSP/PaC chip set can be used in a variety of system architectures which allow system throughput requirements to be traded-off against hardware constraints. A detailed functional description of both the PaC and these DaSP/PaC-based system architectures appears in the **PaC User's Guide**.

Memory Address Sequences and Control

As shown in the block diagram on page 1, the core of the PaC consists of five address generators which are shown as IAS, OAS, RAS, WAS and XAS. IAS and OAS generate address sequences for data input and output, respectively, while RAS and WAS generate read and write addresses to data processing memories respectively. The XAS sequencer normally addresses an auxiliary or coefficient data memory. These address generators typically create all the addressing sequences required to implement various FFT-based DSP systems. Each address generator outputs a new address on every rising edge of the appropriate clock input. IAS and OAS are clocked by ICLK and OCLK, respectively, while RAS, WAS, and XAS are clocked by CLKIN. ICLK, OCLK, and CLKIN can be completely asynchronous with respect to one another. As shown in the block diagram, the 16 bit outputs of these five address generators are routed through multiplexing logic to five external address buses labeled ADRA, ADRB, ADRC, ADRD and ADRX; memory write enable strobes are also routed to four control pins labeled AWE', BWE', CWE', and DWE'. These address buses and write enables can be used to control up to five distinct memories simultaneously.

Typically, each PaC address bus addresses a memory containing complex (i.e. real and imaginary) data. The data port of each memory, in turn, is connected to one of the three I/O ports of the DaSP, to an input data collection buffer, or to an output data buffer. When the PaC is used with the DaSP running in the dual I/O mode, all of these memories can be single-ported, and only a minimum of glue logic is needed to complete a system.

Normally, a DaSP/PaC chip set is used in conjunction with a ping-pong memory architecture in which arrays of data are passed through the DaSP between pairs of memories, with one memory supplying data to the DaSP while the other receives output data from the DaSP. In such a ping-pong memory system, it is necessary to be able to change the destinations of the PaC address generator outputs from one data pass to the next. This function is accomplished by the bus multiplexers shown in the block diagram, and these multiplexers are, in turn, controlled by the BSC ("bus switch code") field in the PaC instruction, which will be discussed later. Note that the output of the XAS generator is always routed to the ADRX address bus.

The address sequences created by the five PaC address generators are selected by the 5 bit NODE field in the PaC instruction. The various address sequences supported by the PaC are as follows:

Mnemonic	Sequence Description
FFT0 to FFT15	Data and coefficient address sequences associated with an in-place, decimation-in-frequency (DIF) FFT algorithm. The sequences span from column 0 to column 15 of a radix-2, radix-4, or mixed radix-2/radix-4 FFT flowgraph, covering up to a 64K point complex data array. The radix base for the algorithm is defined by the PaC instruction and the RCONFIG control register. Digit reversed addresses can be optionally produced in the final FFT column.
SEQ	Sequential: A normal sequential binary sequence for the purpose of window or filter, multiplication, magnitude squared, vector addition, etc.
SSEQ	Symmetric Sequential: A normal sequential binary sequence which is symmetrical about the center point to handle symmetric windows, etc.
FFT2N	Supports DaSP's FFT2N function; generates addressing sequences to handle the data recombination associated with the implementation of a 2N real-point FFT using an N complex-point FFT.
FFTNN	Supports DaSP's FFTNN function; generates addressing sequences to handle the data recombination associated with the implementation of two separate real N-point FFTs via a single N complex-point FFT.
FTRS	Filter Sequence: The overlap/save sequence to allow overlapping of input data frames during frequency domain FIR filtering of a continuous input sequence.

Control Registers

The PaC also contains several user-loadable control registers which add to the versatility of the PaC (see block diagram). These registers supply various parameters to the PaC describing the user's system configuration and are briefly described below:

Mnemonic	Register Description
RCONFIG(15:0)	Contains system configuration information such as cascaded system, single memory system, radix type, etc.
PLAT(3:0)	Processor latency; specifies the latency of the DaSP in terms of machine cycles (user should always set to 4).
PSLEN(7:0)	Pause length; used to insert delays between data passes.
PRGSZ(5:0)	Program size; number of instructions in user's PaC program.
MLAT(11:0)	Memory latency; specifies the latencies present in the address and data paths of each of the processing and auxiliary memory blocks. A latency in a memory path will be introduced if address and/or data of a memory are being latched for high performance applications. The PaC compensates for these latencies when generating the addresses and write strobes for corresponding memories.
M(4:0)	Base-2 or base-4 logarithm of N (i.e. array length) as required.
N(15:0)	Specifies the size of the data array to be processed. It can range from 4 points to 64K complex points.
M4(3:0)	Holds value of (M-1)/2 for use during mixed-radix FFTs.
K(15:0)	Specifies the size of the overlap in successive input data frames. The overlapping is normally used for frequency domain filtering. It can range from 0 to 50% of the array size (in inverse powers of two).
LFND(5:0)	Left neighbor node field; contains the value of the NODE instruction field of the current PAC's left neighbor in full column-pipelined cascaded systems.
RTND(5:0)	Right neighbor node field; contains the value of the NODE instruction field of the current PAC's right neighbor in full column-pipelined cascaded systems.
TCNT(15:0)	Test count; a diagnostic register not intended for general usage which should normally be ignored.
STAD(15:0)	Starting address; specifies the page offset to be applied to addresses output on the ADRA, ADRB, ADRC, and ADRD buses.

Instruction Memory

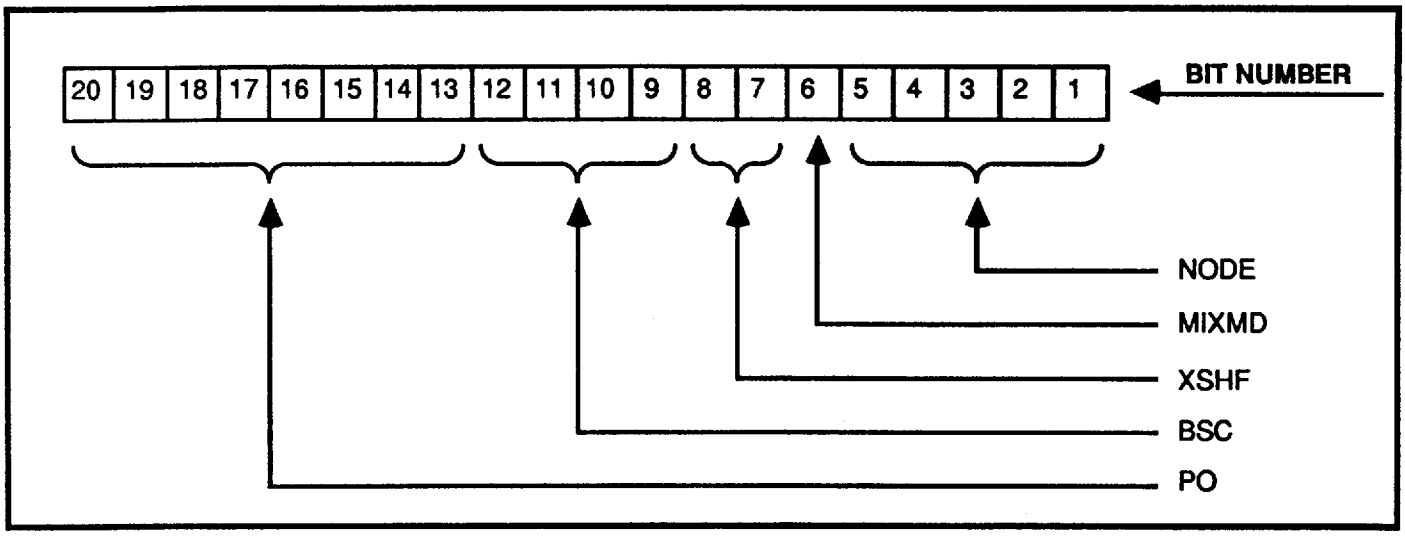
The PaC contains a 32 word by 20-bit instruction RAM which holds the user's DSP program. The PaC instruction layout appears in Figure 1. The concept of a PaC instruction is somewhat different from that of a typical microprocessor. In microprocessors, an instruction typically manipulates just a few data values. A PaC instruction controls a full pass of an N-point data array through the DaSP, where N is defined by the similarly named PaC control register. During the pass, the DaSP function programmed into the PO(7:0) field of the PaC instruction will be applied to successive sets of data values from the N-point data array. DaSP functions and data sets are defined in the **DaSP Data Sheet** and **DaSP User's Guide**. Since one PaC instruction controls a complete pass of the data array through the DaSP, a 1024 point FFT using a radix-4 algorithm, for example, takes only five instructions since the corresponding FFT flowgraph consists of five FFT columns. If additional passes such as windowing or magnitude-squared are desired, one instruction will be needed for each such pass. The on-chip 32 word program memory suffices for most applications; however, external program memory may also be used if necessary (see the **PaC User's Guide** for further details).

The various fields of the PaC instruction as displayed in Figure 1 are briefly described below:

PO(7:0)	Programmable outputs. The user-defined 8 bit value in this field is directly fed to the PO pins of PaC; normally, 6 of these bits are used to hold the 6 bit DaSP function code.

FIGURE 1 - PaC INSTRUCTION FORMAT

T-52-33-55



BSC(3:0) Bus switch code. This field controls the bus multiplexers of the PaC to assign the appropriate address generators to the ADRA, ADRB, ADRC and ADRD address buses. The BSC field is also output directly to the BSC pins where it can be accessed for the purpose of controlling the data buffers in the user's system. The legal BSC encodings are shown in Table 1.

XSHF(1:0) This field defines the number of bit positions to left-shift the XAS address generator output prior to outputting it on the ADRX bus. This feature permits coefficient table decimation which is useful for sharing coefficient memories between different sized FFTs.

MIXMD This bit indicates if a mixed-radix FFT (radix-2/radix-4) is being performed; it should be set in the PaC instructions comprising the radix-4 passes. By using the mixed-radix mode, it is possible to transform a data array in which the number of points is an odd power of 2 at almost the speed of an even power of 2 (i.e. radix-4) array.

NODE(4:0) This field selects the addressing sequences produced by the five address generators of the PaC during the current data pass. These sequences were briefly described earlier. The legal encodings of this field are listed in Table 2.

Host Interface and PaC Initialization

All the control registers and the instruction memory of the PaC are memory mapped for ease of initialization; this memory map appears in Figure 2. The PaC can be initialized by a host processor or it can autoboot itself from an external ROM. The initialization option is determined by the state of the AUTOBOOT pin. Control register and instruction memory data are transferred to the PaC via the ADRA and ADRB buses; for this purpose, ADRA serves as an input address bus, while ADRB serves as a data bus. After initialization, the SYNC pins on both the DaSP and the PaC should also be activated to synchronize PaC address generation with DaSP data processing. Finally, processing is started by activating the GO pin, after which the PaC manages the complete system. The PaC executes the DSP algorithm by either continuously looping through the PaC program or executing it one instruction at a time in single-step fashion, as determined by the ASTRT bit in the RCONFIG control register.

Clocks

The PaC is operated by using a system clock (CLKIN) at a frequency of 4/Tm, where Tm is the machine cycle time of the DaSP (100 nsec minimum). However, additional clock inputs ICLK, OCLK and HCLK are also provided. ICLK and OCLK manage input data collection and output data dumping, respectively, at the desired rate. HCLK is used to clock data and addresses into the PaC during PaC initialization. CLKIN, ICLK, OCLK, and HCLK can all be asynchronous with respect to one another.

TABLE 1 - PaC INSTRUCTION BSC FIELD ENCODINGS

T-52-33-55

BSC	RECURSIVE OPERATION:				CASCADED OPERATION:			
	ADRA	ADRB	ADRC	ADRD	ADRA	ADRB	ADRC	ADRD
0000	IAS	***	WAS	OAS	IAS	RAS	WAS	OAS
0001	IAS	WAS	RAS	OAS	RAS	IAS	WAS(1)	OAS
0010	OAS	IAS	RAS	WAS	T.S.	WAS(2)	RAS(3)	T.S.
0011	RAS	IAS	OAS	WAS	T.S.	RAS(4)	OAS	WAS
0100	WAS	IAS	OAS	RAS				
0101	***	OAS	WAS	IAS				
0110	WAS	OAS	RAS	IAS				
0111	OAS	IAS	WAS	***				
1000	OAS	RAS	IAS	WAS				
1001	OAS	WAS	IAS	RAS				
1010	OAS	WAS	RAS	IAS				
1011	(Reserved)							
1100	WAS	OAS	IAS	RAS				
1101	(Reserved)							
1110	(Reserved)							
1111	(Reserved)							

*** RAS if MUXRW = 0
RAS/WAS if MUXRW = 1

Notes for cascaded operation:

1. The write address generator is used to generate the read address sequence for the PaC's right neighbor.

2. The write address generator is used to generate the write address sequence for the PaC's left neighbor.

3. The read address generator is used to generate the read address sequence for the PaC's right neighbor.

4. The read address generator is used to generate the write address sequence for the PaC's left neighbor.

T.S. - Tri-State

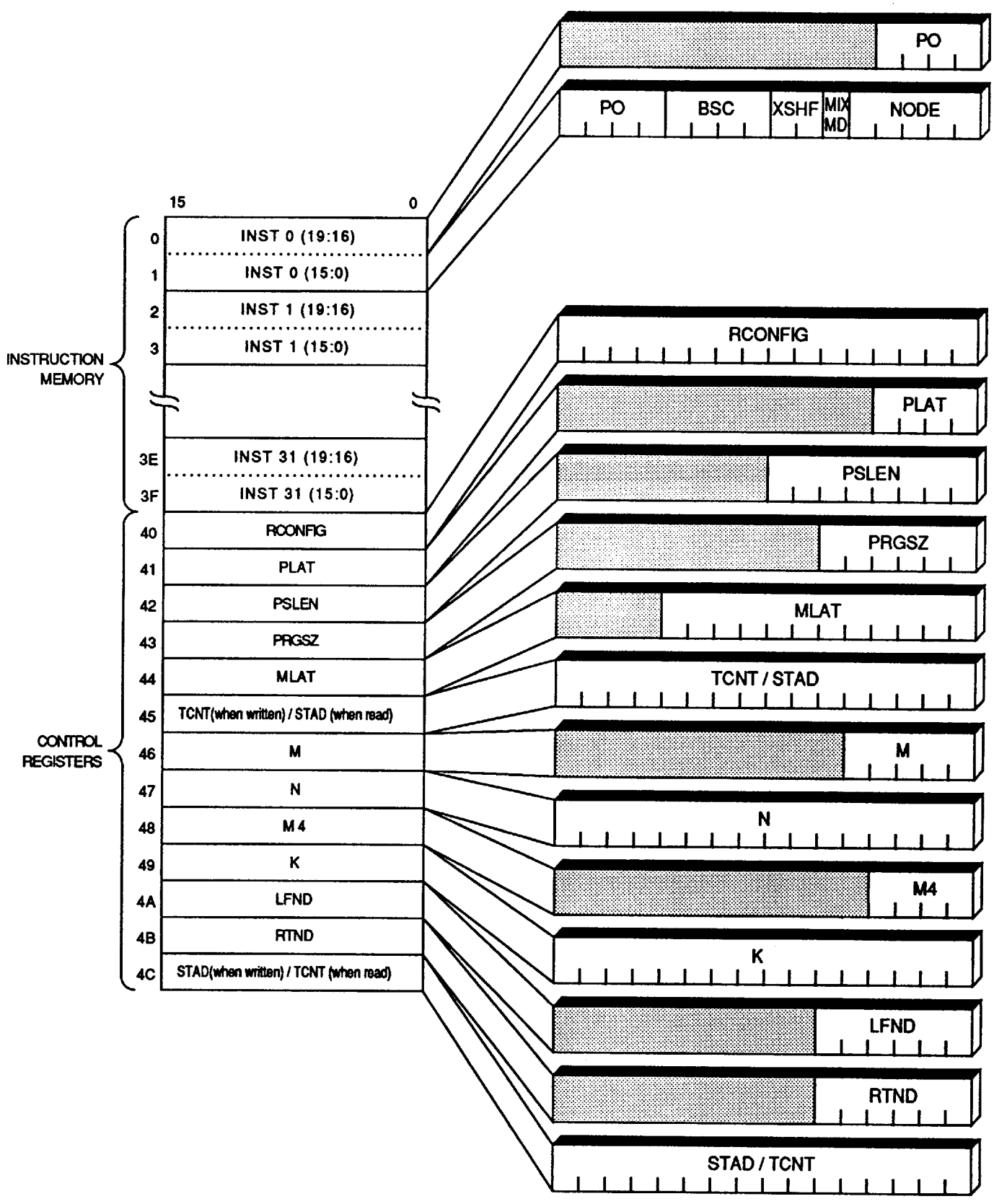
TABLE 2 - PaC INSTRUCTION NODE FIELD ENCODINGS

Hex Code	Mnemonic	Description
00	FFT0	FFT Column 0
01	FFT1	FFT Column 1
02	FFT2	FFT Column 2
03	FFT3	FFT Column 3
04	FFT4	FFT Column 4
05	FFT5	FFT Column 5
06	FFT6	FFT Column 6
07	FFT7	FFT Column 7
08	FFT8	FFT Column 8
09	FFT9	FFT Column 9
0A	FFT10	FFT Column 10
0B	FFT11	FFT Column 11
0C	FFT12	FFT Column 12
0D	FFT13	FFT Column 13
0E	FFT14	FFT Column 14
0F	FFT15	FFT Column 15
10	SEQ	Sequential
11	SSEQ	Symmetric Sequential
12	FFT2N	Double-Length Real FFT
13	FFTNN	Dual Real FFT
14	FTRS	Filter Sequence
15-1E	Reserved	
1F	EOPM	End of Process Marker

a66212

FIGURE 2 - MEMORY MAP OF PaC CONTROL AND INSTRUCTION REGISTERS

T-52-33-55



PIN DESCRIPTIONS:

T-52-33-55

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
		ADDRESS BUSES	
ADRA (15:0)	I/O	(Output) Address Bus for Memory A/(Input) Host Address Bus	16
ADRB (15:0)	I/O	(Output) Address Bus for Memory B/(Input) Host Data Bus	16
ADRC (15:0)	O	Address Bus for Memory C	16
ADRD (15:0)	O	Address Bus for Memory D	16
ADRX (15:0)	O	Address Bus for Auxillary Memory X	16
OE'	I	Output Enable: Tristates Address Buses, PO(7:0), IP(4:0) If High	1
		MEMORY CONTROLS	
AWE'	O	Memory A Write Strobe	1
BWE'	O	Memory B Write Strobe	1
CWE'	O	Memory C Write Strobe	1
DWE'	O	Memory D Write Strobe	1
OVAWE'	O	Filter Overlap Memory A Write Strobe	1
OVBWE'	O	Filter Overlap Memory B Write Stobe	1
OVACS'	O	Filter Overlap Memory A Chip Select	1
OVBCS'	O	Filter Overlap Memory B Chip Select	1
		PASS EXECUTION CONTROLS	
BOP	O	Beginning of Pass Marker	1
EOP	O	End of Pass Marker	1
EOPR	O	End of Process Marker	1
IBUSY	O	Input Data Collection in Progress	1
OBUSY	O	Output Data Dump in Progress	1
IFULL	O	Input Memory Full	1
OEMPTY	O	Output Memory Empty	1
		HOST INTERFACE/INITIALIZATION CONTROLS	
AUTOBOOT	I	Autoboot from a Memory	1
BOOTDONE	O	PaC Autoboot Complete	1
CS'	I/O	(Input) PaC Chip Select from Host/(Output) Autoboot Memory Select	1
WR'	I	Write Strobe from Host	1
RST'	I	Reset Input	1
INITPR	O	Initializes External Processor	1
GO	I	Start Instruction Execution	1
		GENERAL COMMUNICATION SIGNALS	
PO (7:0)	I/O	(Ouput) Programmable Outputs from Internal Instruction/ (Input) External Instruction Fields XSHF (1:0), MIXMD, NODE (4:0)	8
IP (4:0)	I/O	(Output) Internal Instruction Memory Pointer/ (Input) External PaC Instruction Field BSC (3:0)	5
BSC (3:0)	O	Bus Switch Code: Controls Internal Bus Multiplexers	4
MUXRW	O	Multiplexed Read Write (Single Memory System)	1
		QUAD-MODE CONTROLS	
QAS0	O	Quad-Mode Address Strobe 0	1
QAS1	O	Quad-Mode Address Strobe 1	1
QAS2	O	Quad-Mode Address Strobe 2	1
QAS3	O	Quad-Mode Address Strobe 3	1
		CLOCK SIGNALS	
CLKIN	I	System Clock Input (Frequency 4/Tm)	1
ICLK	I	Input Data Collection Clock	1
OCLK	I	Output Data Dump Clock	1
HCLK	I	Host Interface Clock	1
SYNC	I	System Clock Synchronization Signal	1
CLKOUT	O	Delayed System Clock Output (Frequence 4/Tm)	1
MCLKOUT	O	Machine-Cycle Clock Output (Frequency 1/Tm)	1
		SERIAL SCAN FOR NON-FUNCTIONAL-TEST (NFT)	
NFT	I	NFT Testing in Progress	1
NFTS	I	NFT Scan in Progress	1
SIN	I	NFT Serial Scan Input	1
SOUT	O	NFT Serial Scan Output	1
		SUPPLY	
VCC	I	VOLTAGE SUPPLY	4
GND	I	GROUND	4
		TOTAL PACKAGE PINS USED	144

a66212

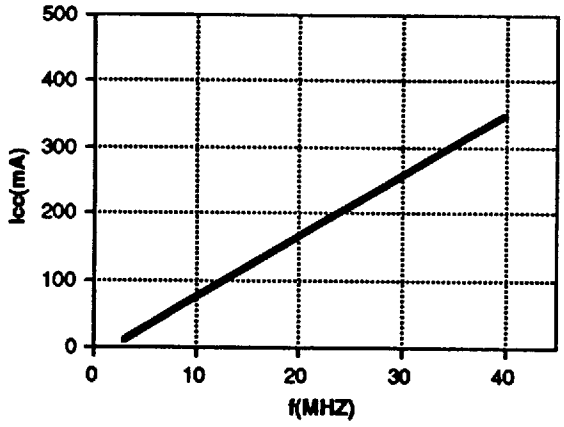
ABSOLUTE MAXIMUM RATINGS:

Positive Supply Voltage .....-0.5V to 7.0V
DC Input Voltage .....-0.5V to 7.0V
DC Output Voltage (Applied in Hi-Z State) ..-0.5V to 7.0V
Low Level Output Current .....20 mA
Operating Case Temperature .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C

Note:
Operation at any Absolute Maximum Rating is not implied. Ratings are provided for guidance purposes only and are not tested. Exposure to absolute maximum rating conditions over extended periods may affect device reliability.

TYPICAL OPERATING CURRENT vs FREQUENCY: (@ Vcc = 5V, T_a = 25°C)

T-52-33-55



OPERATING CONDITIONS:

Parameter	Temperature Range: Commercial a66212BCG Min	Nom	Max	Commercial a66212ACG Min	Nom	Max	Industrial a66212BIG Min	Nom	Max	Military a66212BMG a66212BEG Min	Nom	Max	Units
V_{cc} Supply Voltage	4.75	5	5.25	4.75	5	5.25	4.5	5	5.5	4.5	5	5.5	V
T_c Case Temperature	0		70	0		70	-40		85	-55		125	°C

D.C. ELECTRICAL CHARACTERISTICS (Within Operating Conditions):

Parameter	Test Conditions	Temperature Range: Commercial a66212BCG Min	Max	Commercial a66212ACG Min	Max	Industrial a66212BIG Min	Max	Military a66212BMG a66212BEG Min	Max	Units
I_{cc} Supply Current	Vcc Max, fci Max		400		450		500		500	mA
V_{ih} Input High Voltage		2.0		2.0		2.2		2.2		V
V_{il} Input Low Voltage			0.8		0.8		0.6		0.6	V
V_{oh} Output High Voltage	Vcc Min, Ioh=-4.0mA	2.4		2.4		2.6		2.6		V
V_{ol} Output Low Voltage	Vcc Min, Iol= 4.0mA		0.4		0.4		0.4		0.4	V
I_{ih} Input High Current	Vin > 2.2V		100		100		100		100	µA
I_{il} Input Low Current	Vin < 0.8V	-100		-100		-100		-100		µA
V_{ic} Input Clamping Voltage	-1 mA +1 mA	-1.5 0.3	-0.3 1.5	-1.5 0.3	-0.3 1.5	-1.5 0.3	-0.3 1.5	-1.5 0.3	-0.3 1.5	V V
I_{oz} Hi-Z Output Current	Vcc Max, .4V<Vout<2.6V	-100	100	-100	100	-100	100	-100	100	µA
C_i Input Capacitance †	Vcc=5V,Tc=25° C		10		10		10		10	pF
C_o Output Capacitance †	Vcc=5V,Tc=25° C		10		10		10		10	pF

† Parameter is guaranteed (but not tested) by design.

Array MICROSYSTEMS

a66212

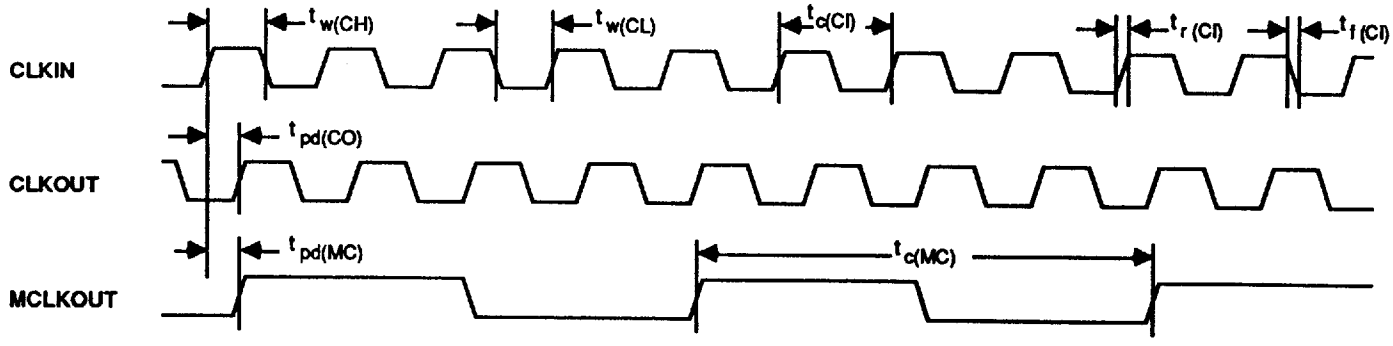
INTERNAL CLOCK CONTROL SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
f_{ci}	CLKIN Frequency	3	30	3	40	3	30	3	30	MHz
$t_{c(CI)}$	CLKIN Period	33	333	25	333	33	333	33	333	nS
$t_{w(CL)}$	CLKIN Low Level Pulse	12		12		12		12		nS
$t_{w(CH)}$	CLKIN High Level Pulse	10		10		10		10		nS
$t_{r(CI)}$	CLKIN Rise Time †		10		10		10		10	nS
$t_{f(CI)}$	CLKIN Fall Time †		10		10		10		10	nS
$t_{pd(CO)}$	CLKIN to CLKOUT Delay	1	16	1	12	1	14	1	14	nS
f_{mc}	MCLKOUT Frequency †	0.75	7.5	0.75	10	0.75	7.5	0.75	7.5	MHz
$t_{c(MC)}$	MCLKOUT Period †	133	1333	100	1333	133	1333	133	1333	nS
$t_{pd(MC)}$	CLKIN to MCLKOUT Delay	1	16	1	9	1	16	1	11	nS

† Parameter is guaranteed (but not tested) by design.

INTERNAL CLOCK CONTROL SIGNALS - A.C. WAVEFORMS



a66212

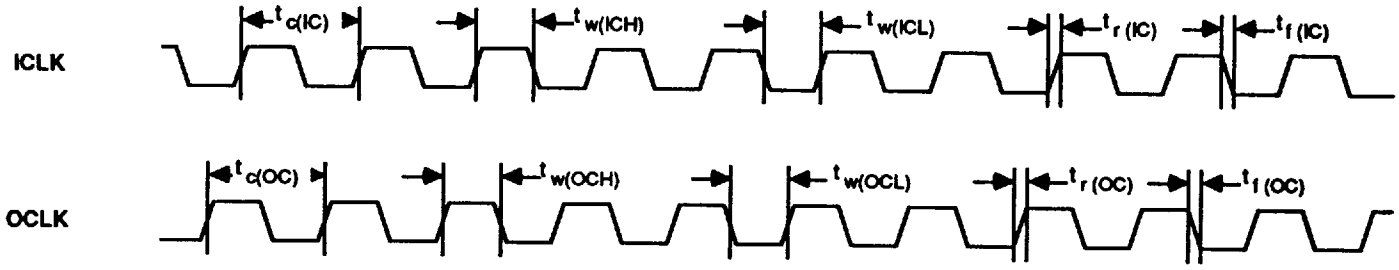
I/O CLOCK CONTROL SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
f_{ic}	ICLK Frequency		30		40		30		30	MHz
$t_{c(IC)}$	ICLK Period	33		25		33		33		nS
$t_{w(ICL)}$	ICLK Low Level Pulse	12		11		12		12		nS
$t_{w(ICH)}$	ICLK High Level Pulse	12		11		12		12		nS
$t_{r(IC)}$	ICLK Rise Time †		10		10		10		10	nS
$t_{f(IC)}$	ICLK Fall Time †		10		10		10		10	nS
f_{oc}	OCLK Frequency		30		40		30		30	MHz
$t_{c(OC)}$	OCLK Period	33		25		33		33		nS
$t_{w(OCL)}$	OCLK Low Level Pulse	12		11		12		12		nS
$t_{w(OCH)}$	OCLK High Level Pulse	12		11		12		12		nS
$t_{r(OC)}$	OCLK Rise Time †		10		10		10		10	nS
$t_{f(OC)}$	OCLK Fall Time †		10		10		10		10	nS

† Parameter is guaranteed (but not tested) by design.

I/O CLOCK CONTROL SIGNALS - A.C. WAVEFORMS

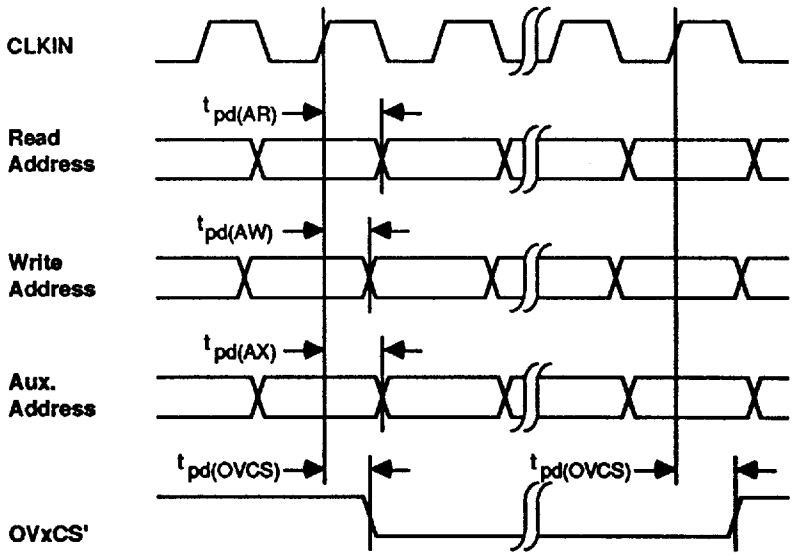


READ / WRITE CONTROL SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{pd(AR)}$	CLKIN to Read Address Delay	3	20	3	16	2.5	19	2.5	19	nS
$t_{pd(AW)}$	CLKIN to Write Address Delay	3	20	3	16	2.5	19	2.5	19	nS
$t_{pd(AX)}$	CLKIN to Auxiliary Address Delay	5	21	5	17	3	20	3	20	nS
$t_{pd(OVCS)}$	CLKIN to any OVxCS'	3	17	3	12	1.5	15	1.5	15	nS

READ / WRITE CONTROL SIGNALS - A.C. WAVEFORMS



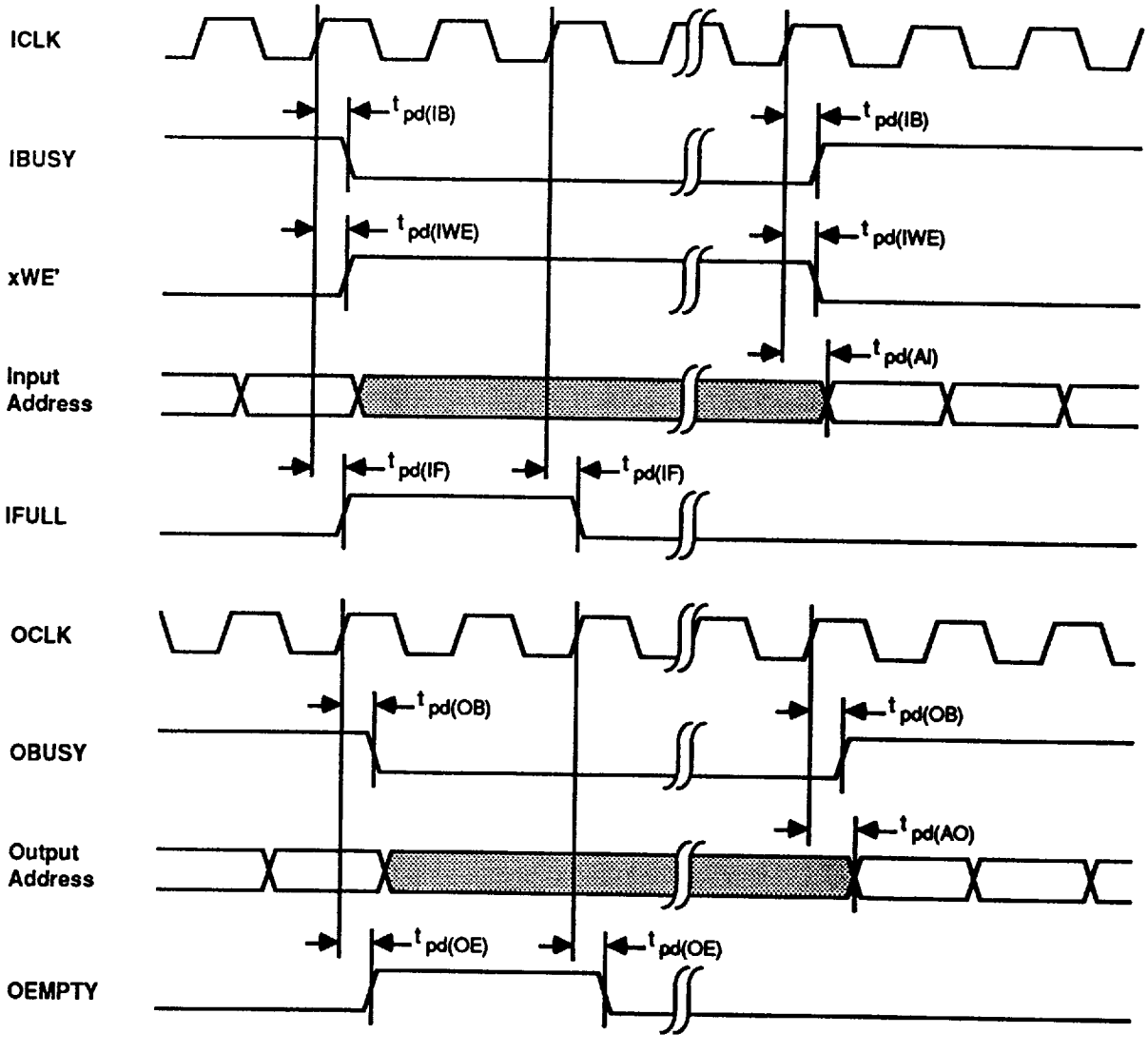
a66212

T-52-33-55

INPUT / OUTPUT CONTROL SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{pd(AI)}$	ICLK to Input Address Delay	3	20	3	16	2.5	19	2.5	19	nS
$t_{pd(AO)}$	OCLK to Output Address Delay	3	20	3	16	2.5	19	2.5	19	nS
$t_{pd(IB)}$	ICLK to IBUSY Delay	3	19	3	15	1	18	1	18	nS
$t_{pd(IF)}$	ICLK to IFULL Delay	3	19	3	15	1	18	1	18	nS
$t_{pd(OB)}$	OCLK to OBUSY Delay	3	19	3	15	1	18	1	18	nS
$t_{pd(OE)}$	OCLK to OEMPTY Delay	3	19	3	15	1	18	1	18	nS
$t_{pd(IWE)}$	ICLK to any xWE' Delay	3	16	3	12	1.5	15	1.5	15	nS
$t_{pd(ICS)}$	ICLK to any OVxCS' Delay	3	16	3	12	1.5	15	1.5	15	nS
$t_{pd(OVWE)}$	ICLK to any OVxWE' Delay	3	16	3	12	1.5	15	1.5	15	nS

INPUT / OUTPUT CONTROL SIGNALS - A.C. WAVEFORMS



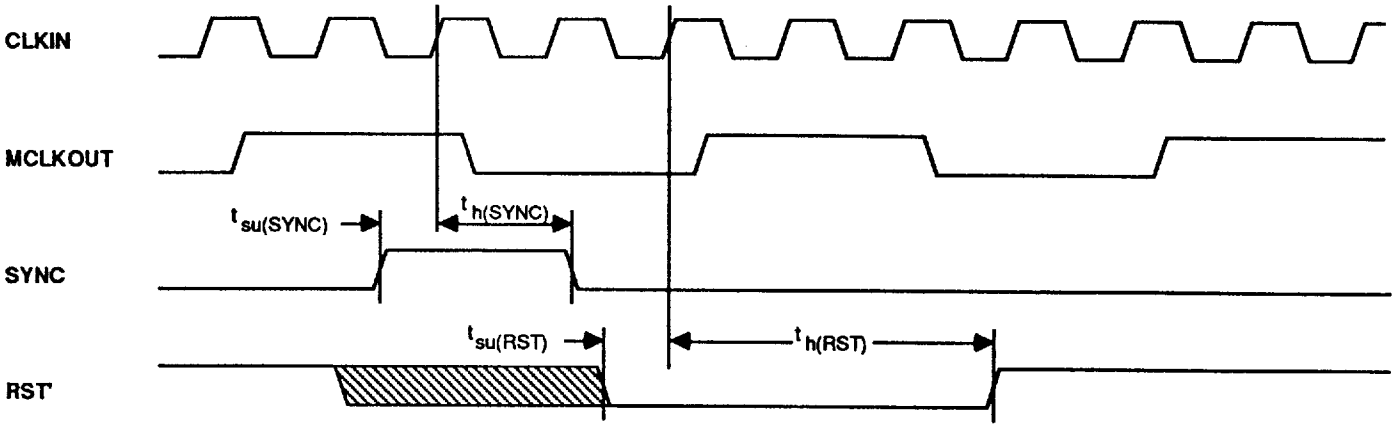
Array MICROSYSTEMS

INITIALIZATION SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{su(SYNC)}$	SYNC Setup to CLKIN	20		11		12		12		nS
$t_{h(SYNC)}$	SYNC Hold after CLKIN	0		0		0		0		nS
$t_{su(RST)}$	RST' Setup to CLKIN	23		20		24		24		nS
$t_{h(RST)}$	RST' Hold after CLKIN	3		3		3		3		nS

INITIALIZATION SIGNALS - A.C. WAVEFORMS



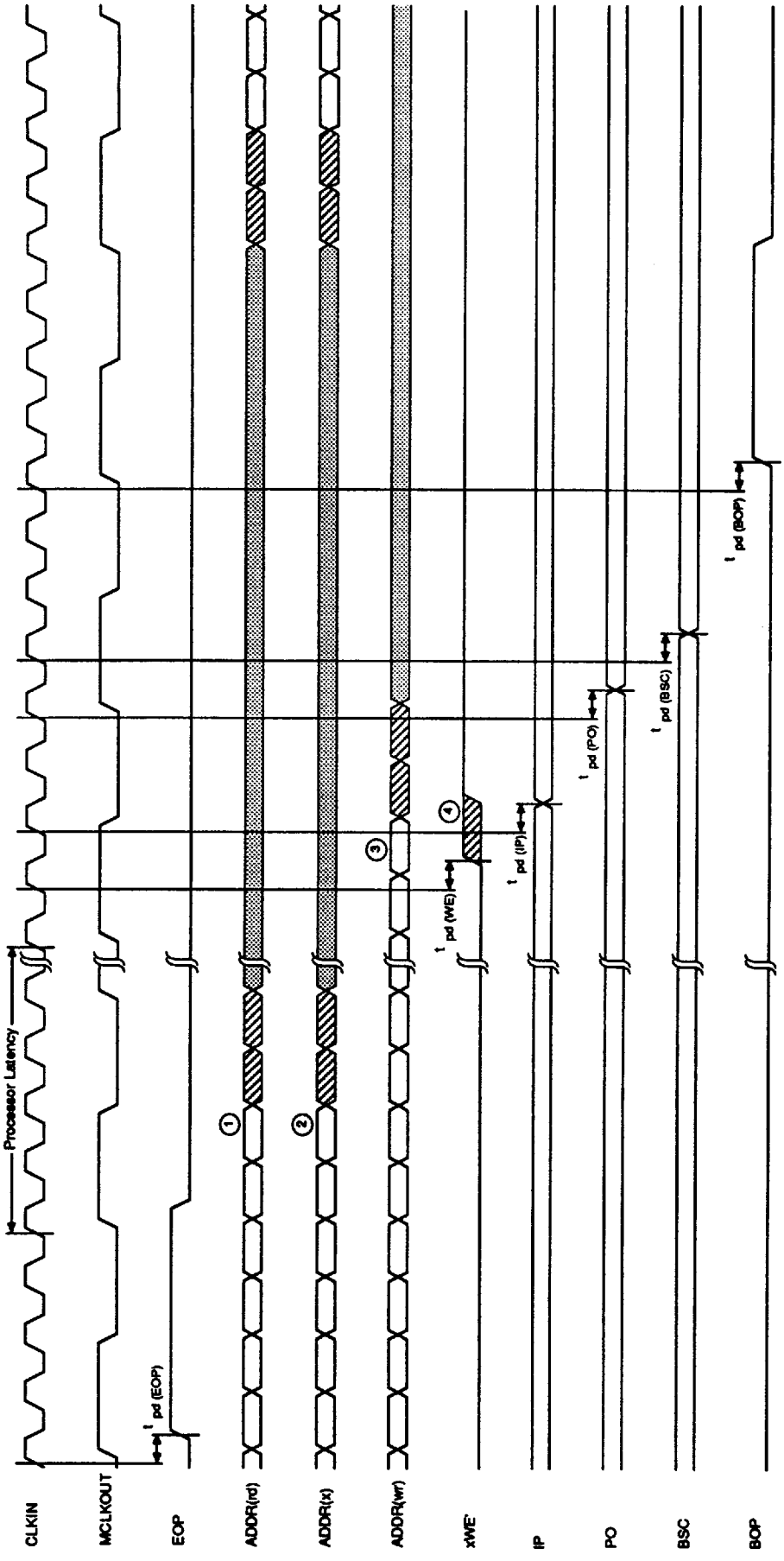
PASS MARKING SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{pd(EOP)}$	CLKIN to EOP Delay	6	22	6	18	3	22	3	22	nS
$t_{pd(IP)}$	CLKIN to IP Delay	5	22	5	18	3	19	3	19	nS
$t_{pd(PO)}$	CLKIN to PO Delay	5	22	5	18	3	21	3	21	nS
$t_{pd(BSC)}$	CLKIN to BSC Delay	5	22	5	18	2	18	2	18	nS
$t_{pd(BOP)}$	CLKIN to BOP Delay	6	22	6	18	3	22	3	22	nS
$t_{pd(WE)}$	CLKIN to any xWE' Delay	3	16	3	12	1.5	14	1.5	14	nS
$t_{su(GO)}$	GO Setup to CLKIN	16		10		12		12		nS
$t_{h(GO)}$	GO Hold after CLKIN	0		0		0		0		nS

a66212

T-52-33-55

PASS MARKING SIGNALS - A.C. WAVEFORMS



Notes:

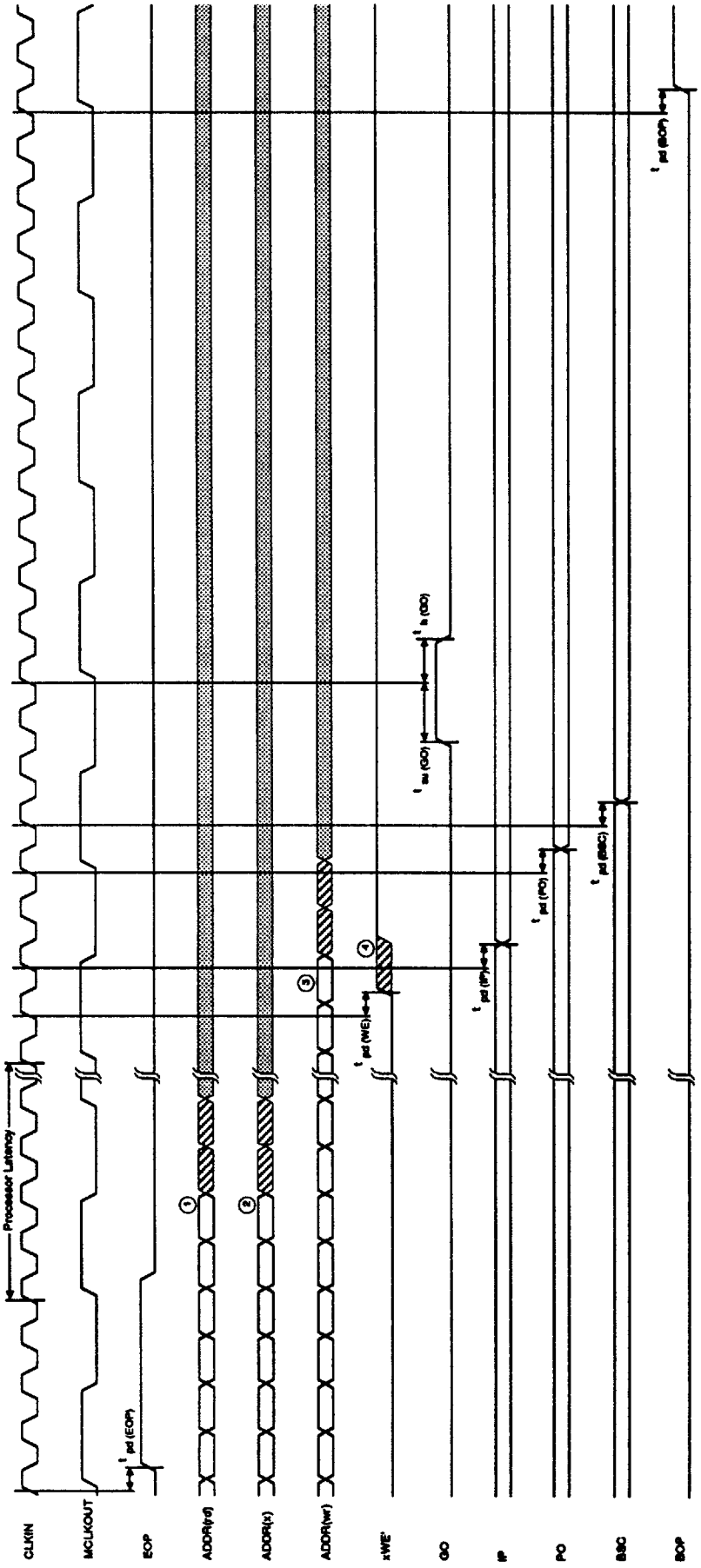
1) The alignment of the last read address is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

2) The alignment of the last auxiliary address is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

3) The alignment of the last write address is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

4) The alignment of the rising edge of the write enable is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

PASS MARKING SIGNALS - A.C. WAVEFORMS CONTINUED



Notes:

1) The alignment of the last read address is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

2) The alignment of the last auxiliary address is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

3) The alignment of the last write address is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

4) The alignment of the rising edge of the write enable is dependent on the value stored in the PaC's MLAT register (see the **PaC User's Guide**).

HOST INTERFACE SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
f_{hc}	HCLK Frequency		10		10		10		10	MHz
$t_{c(HC)}$	HCLK Period	100		100		100		100		nS
$t_{w(HCL)}$	HCLK Low Level Pulse	30		30		30		30		nS
$t_{w(HCH)}$	HCLK High Level Pulse	30		30		30		30		nS
$t_{r(HC)}$	HCLK Rise Time †		10		10		10		10	nS
$t_{f(HC)}$	HCLK Fall Time †		10		10		10		10	nS
$t_{su(HA)}$	ADRA to HCLK Setup	18		9		10		10		nS
$t_{h(HA)}$	ADRA after HCLK Hold	0		0		0		0		nS
$t_{su(HD)}$	ADRB to HCLK Setup	16		12		14		14		nS
$t_{h(HD)}$	ADRB after HCLK Hold	2		1		2		2		nS
$t_{su(CS)}$	CS' to HCLK Setup	30		30		32		32		nS
$t_{h(CS)}$	CS' after HCLK Hold	0		0		0		0		nS
$t_{su(WR)}$	WR' to HCLK Setup	6		3		5		5		nS
$t_{h(WR)}$	WR' to HCLK Hold	0		0		0		0		nS
t_{aa}	ADRA to ADRB Delay	8	45	8	40	4	45	4	45	nS

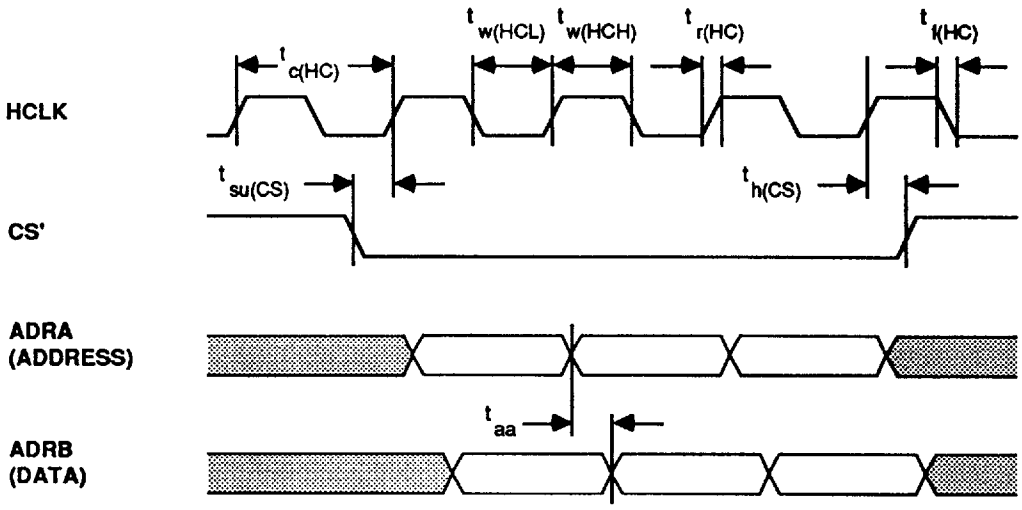
† Parameter is guaranteed (but not tested) by design.

HOST INTERFACE SIGNALS - A.C. WAVEFORMS

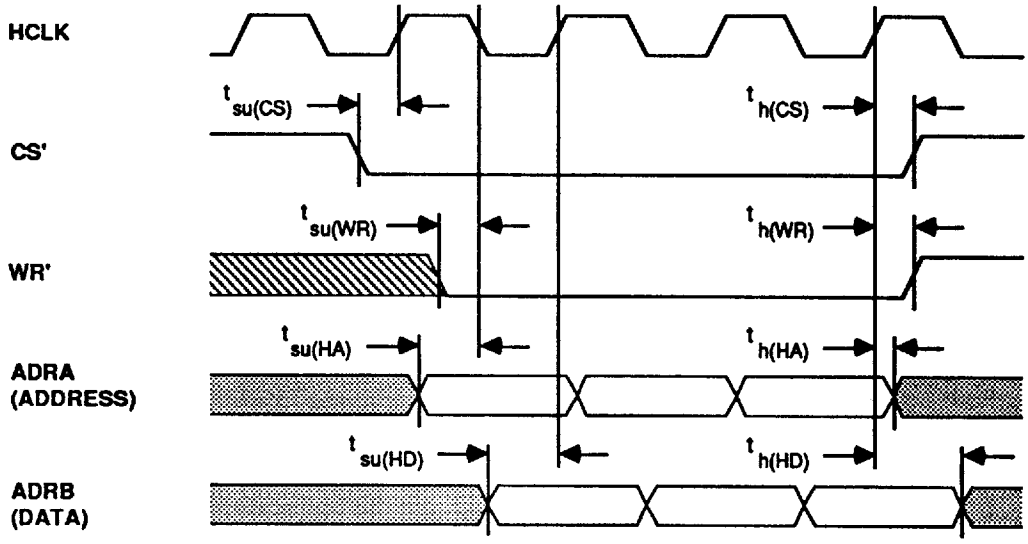
T-52-33-55

(HOST READ CYCLE)

(WR' = HIGH for entire read cycle)



(HOST WRITE CYCLE)



a66212

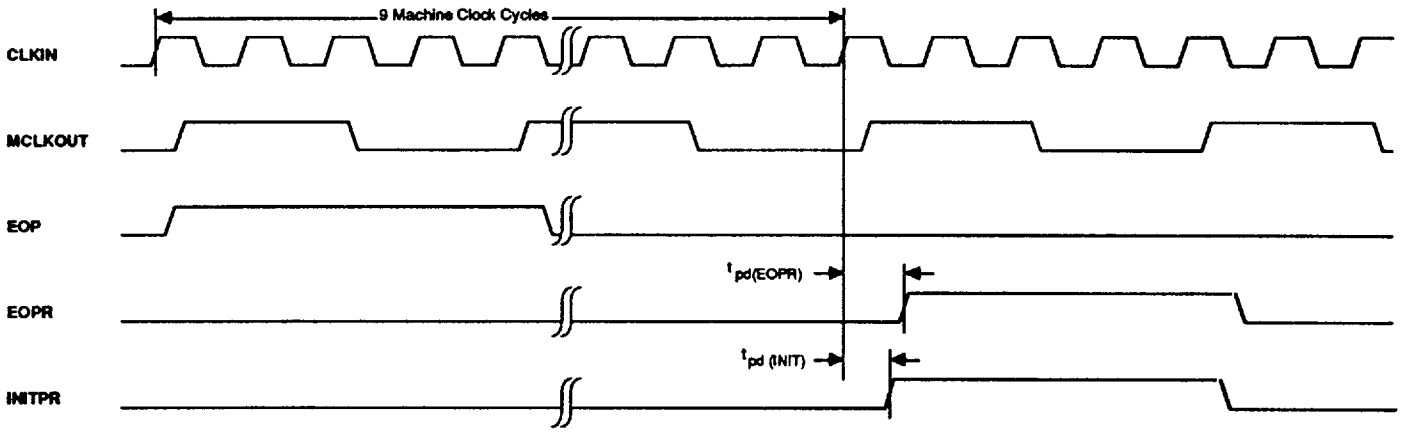
PROCESS MARKING SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

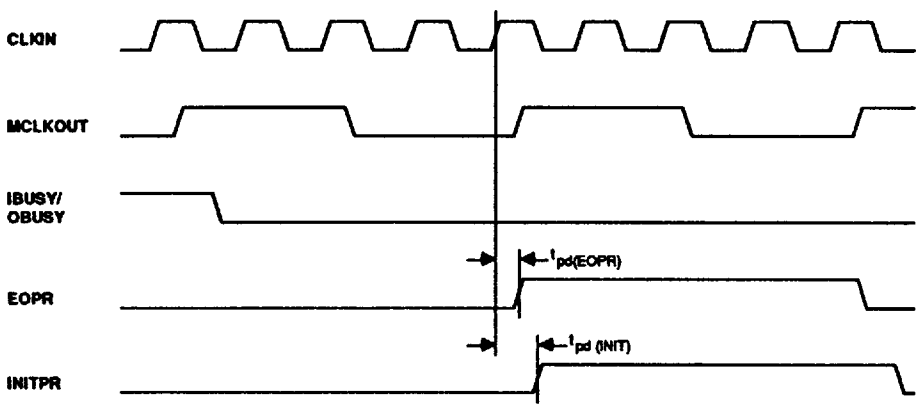
Parameter	Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{pd(INIT)}$ CLKIN to INITPR Delay	6	22	6	18	3	22	3	22	nS
$t_{pd(EOPR)}$ CLKIN to EOPR Delay	6	22	6	18	3	22	3	22	nS

PROCESS MARKING SIGNALS - A.C. WAVEFORMS

(IF I/O IS COMPLETE BEFORE PROCESSING)



(IF PROCESSING IS COMPLETE BEFORE I/O)



array Microsystems, Inc 1420 Quail Lake Loop Colorado Springs, CO 80906 Telephone: +1 (719) 540-7900 FAX +1 (719) 540-7950 Rev 1.2 - 03/93

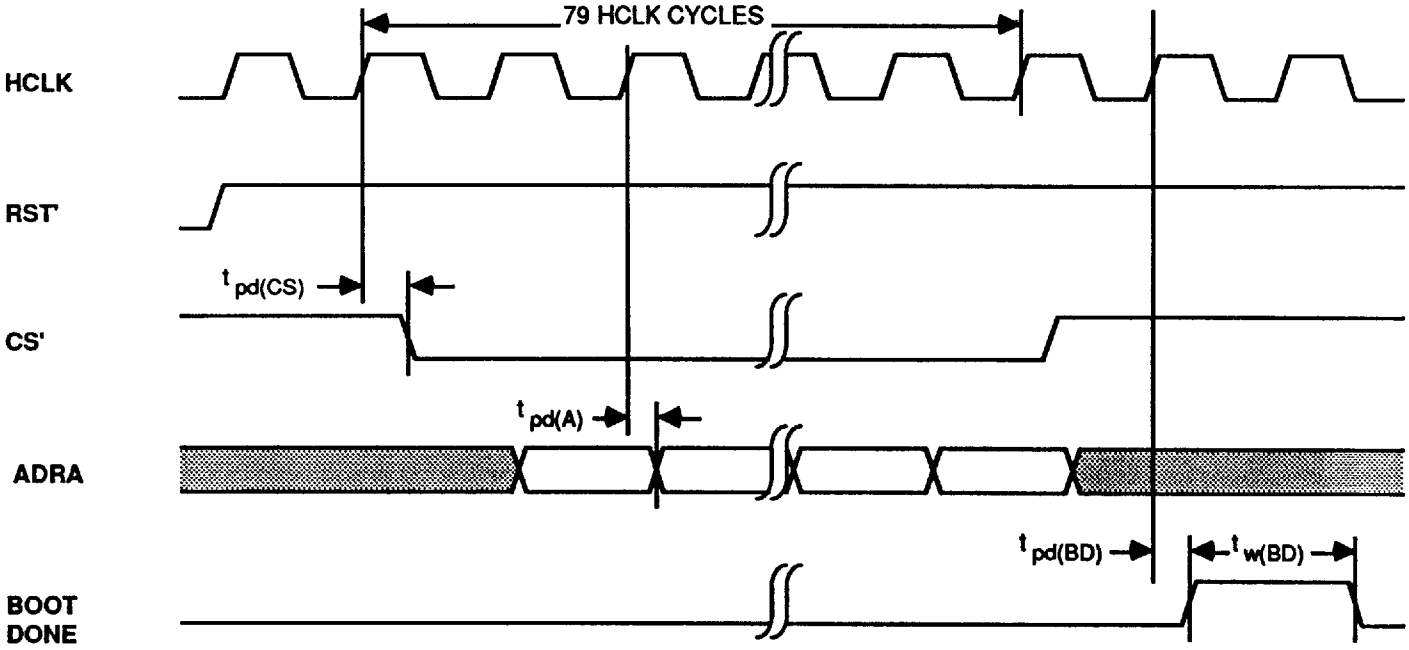
AUTOBOOT SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{pd(CS)}$	HCLK to CS' Delay	3	18	3	13	1	16	1	16	nS
$t_{pd(BD)}$	HCLK to BOOTDONE Delay	3	18	3	13	1	16	1	16	nS
$t_{w(BD)}$	BOOTDONE Pulse Width †	2tc(HC)		2tc(HC)		2tc(HC)		2tc(HC)		nS
$t_{pd(A)}$	HCLK to ADRA Delay	5	22	5	16	3	19	3	19	nS

† Parameter is guaranteed (but not tested) by design.

AUTOBOOT SIGNALS - A.C. WAVEFORMS



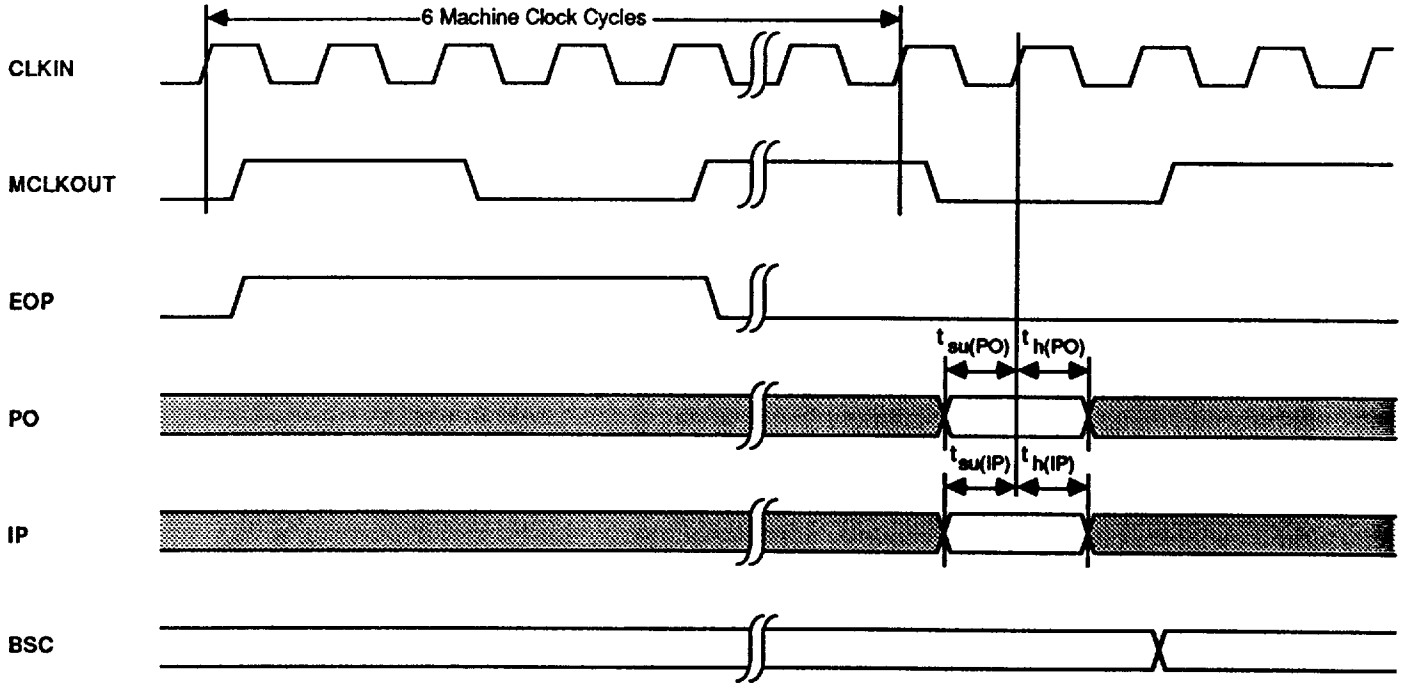
EXTERNAL INSTRUCTION SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{su(PO)}$	PO to CLKIN Setup	8		6		7		7		nS
$t_{h(PO)}$	PO to CLKIN Hold	5		4		4		4		nS
$t_{su(IP)}$	IP to CLKIN Setup	7		5		6		6		nS
$t_{h(IP)}$	IP to CLKIN Hold	5		4		4		4		nS

EXTERNAL INSTRUCTION SIGNALS - A.C. WAVEFORMS

(AFTER NON-EOPM INSTRUCTIONS)

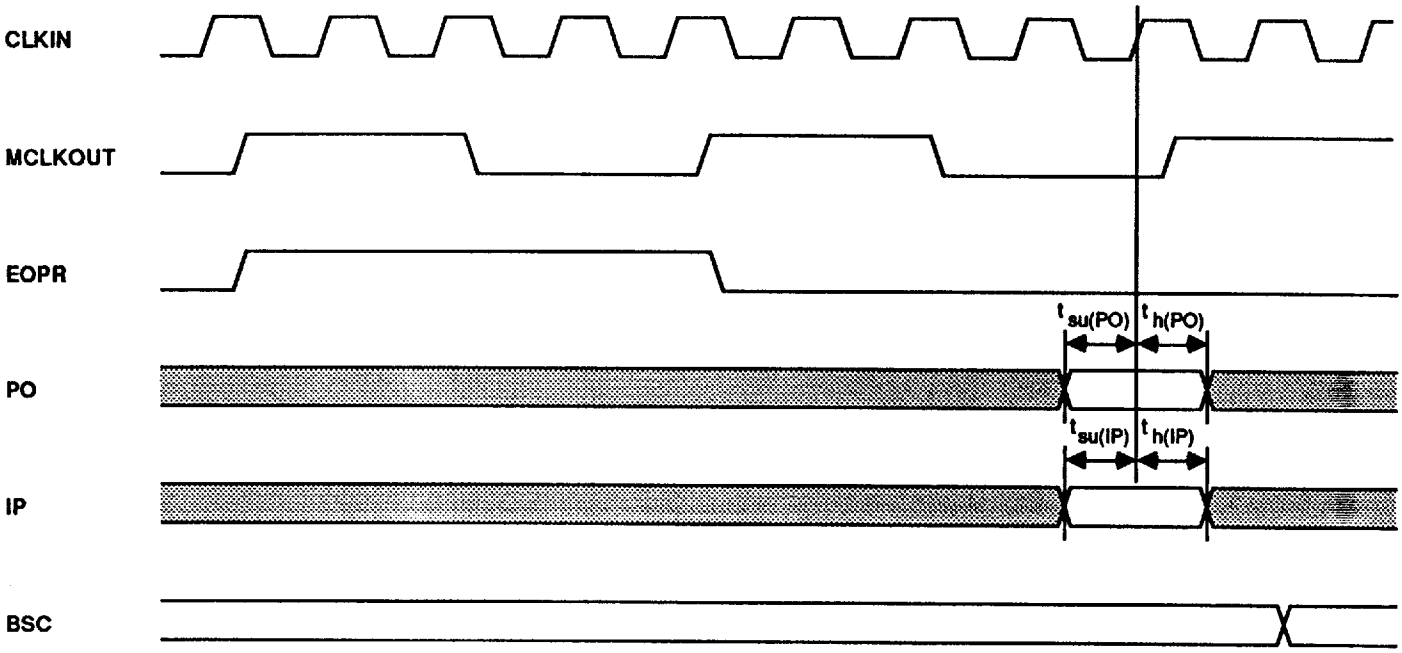


array Microsystems, Inc 1420 Quail Lake Loop Colorado Springs, CO 80906 Telephone: +1 (719) 540-7900 FAX +1 (719) 540-7950 Rev 1.2 - 03/92

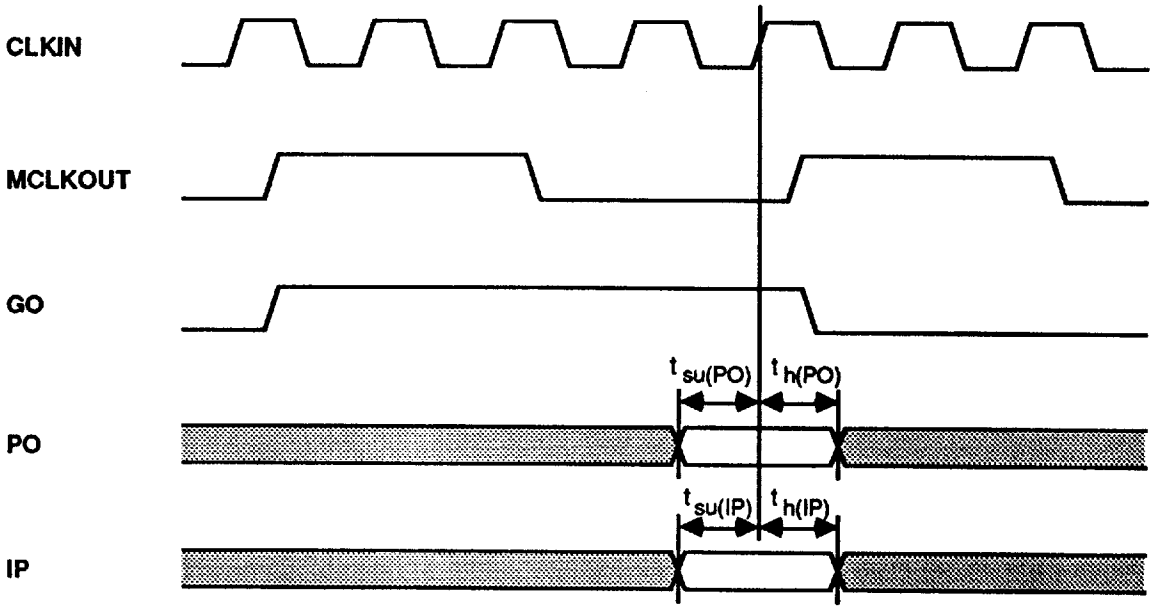
EXTERNAL INSTRUCTION SIGNALS - A.C. WAVEFORMS (cont'd)

T-52-33-55

(AFTER EOPM INSTRUCTION)



(IN RELATION TO GO)



a66212

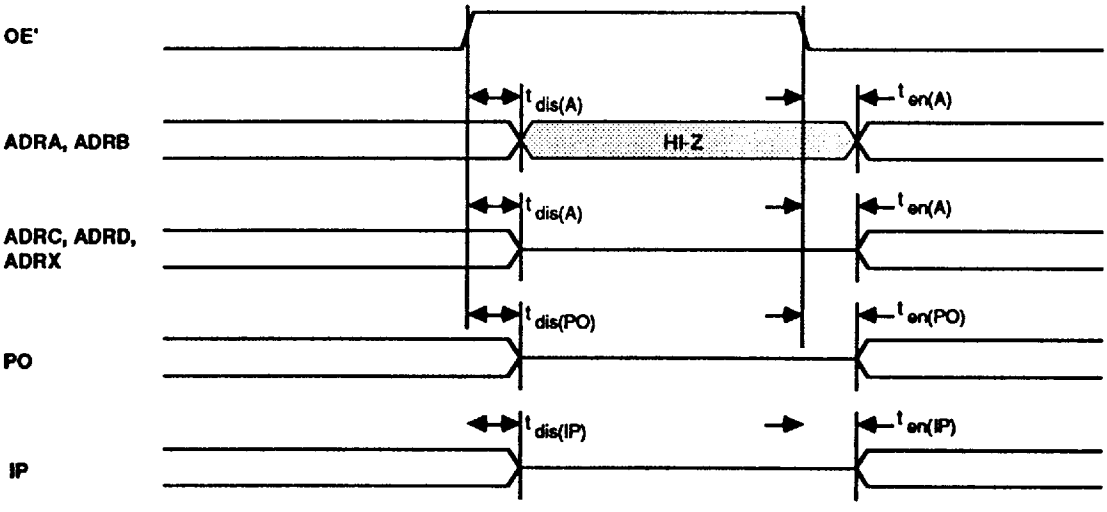
HIGH IMPEDANCE TIMING - A.C. ELECTRICAL CHARACTERISTICS

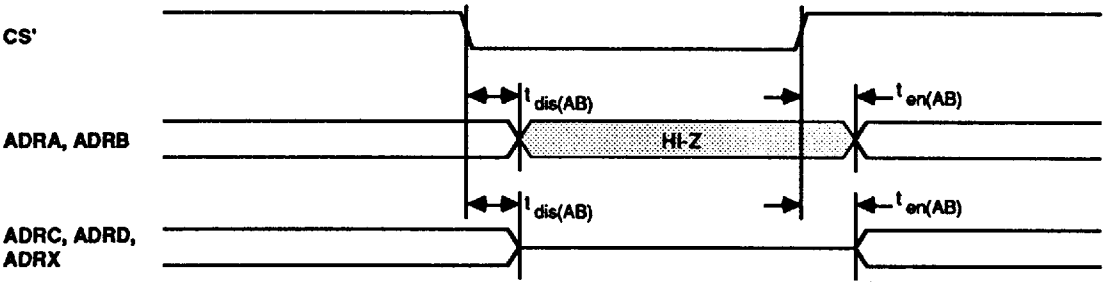
T-52-33-55

Parameter		Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{dis(A)}$	OE' to Address Disable †		30		30		40		40	nS
$t_{dis(PO)}$	OE' to PO Disable †		30		30		40		40	nS
$t_{dis(IP)}$	OE' to IP Disable †		30		30		40		40	nS
$t_{en(A)}$	OE' to Address Enable †		30		30		40		40	nS
$t_{en(PO)}$	OE' to PO Enable †		30		30		40		40	nS
$t_{en(IP)}$	OE' to IP Enable †		30		30		40		40	nS
$t_{dis(AB)}$	CS' to ADRA/ADRB Disable †		35		35		45		45	nS
$t_{en(AB)}$	CS' to ADRA/ADRB Enable †		35		35		45		45	nS

† Parameter is guaranteed (but not tested) by design.

HIGH IMPEDANCE TIMING - A.C. WAVEFORMS



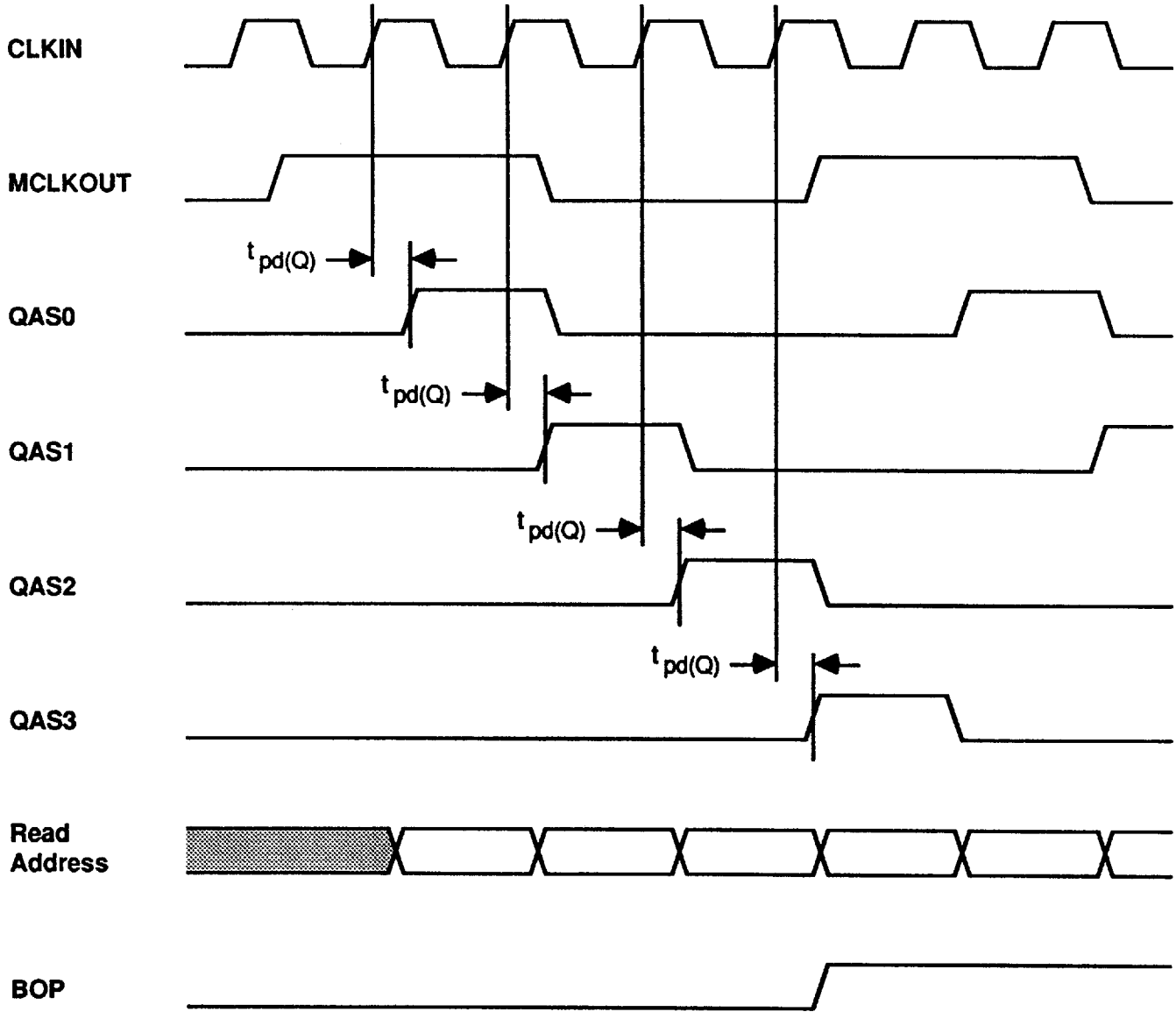


QUAD BUS SIGNALS - A.C. ELECTRICAL CHARACTERISTICS

T-52-33-55

Parameter	Temperature Range: Commercial a66212BCG Min	Commercial a66212BCG Max	Commercial a66212ACG Min	Commercial a66212ACG Max	Industrial a66212BIG Min	Industrial a66212BIG Max	Military a66212BMG a66212BEG Min	Military a66212BMG a66212BEG Max	Units
$t_{pd(Q)}$ CLKIN to QASx	1	19	2	16	1	19	1	19	nS

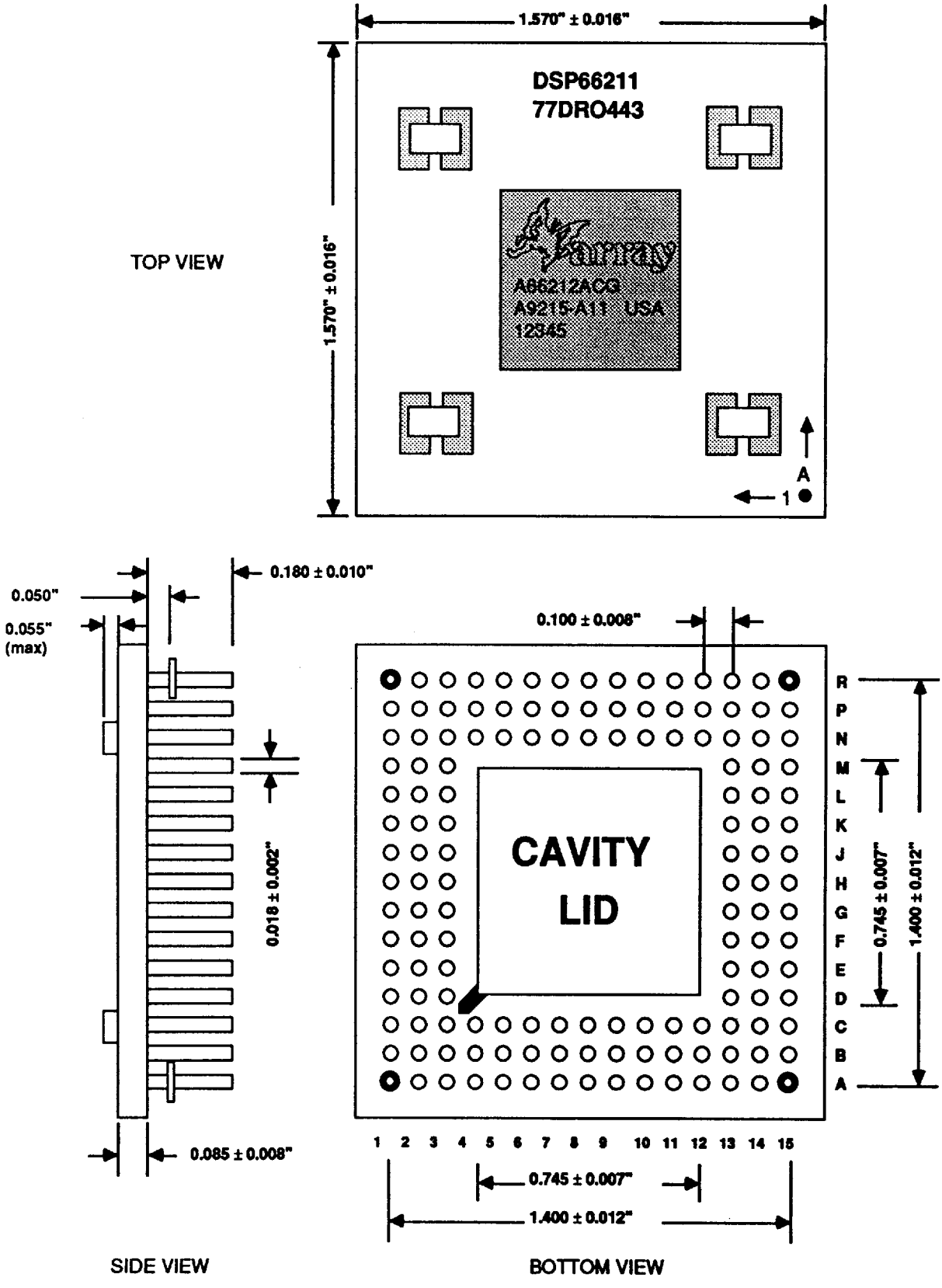
QUAD BUS SIGNALS - A.C. WAVEFORMS



a66212

a66212 PACKAGE DRAWING:

T-52-33-55

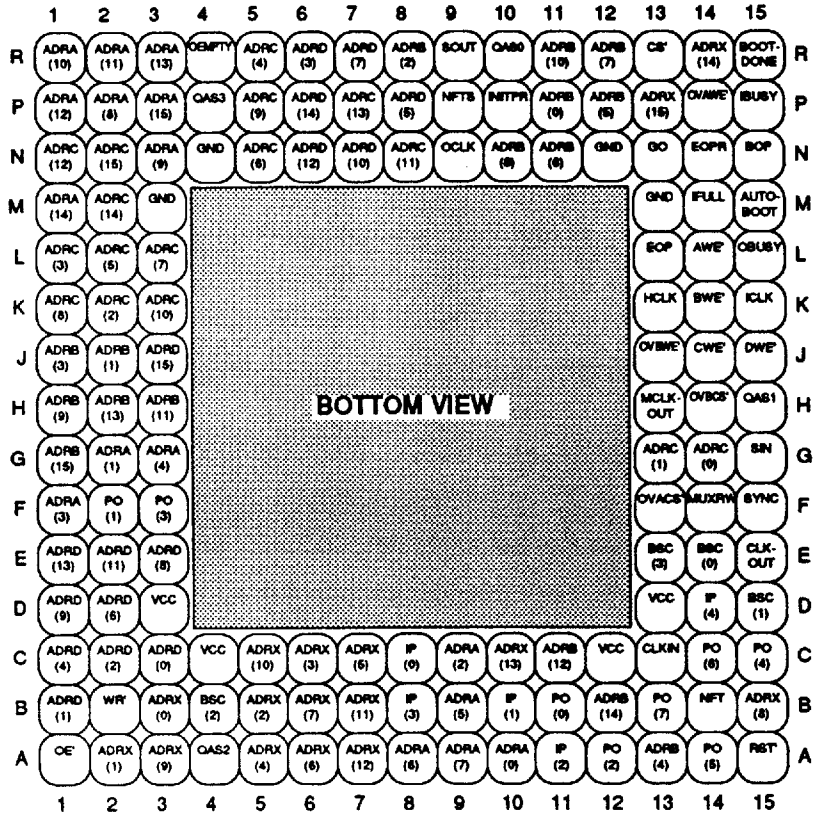


Array MICROSYSTEMS

a66212

a66212 PIN OUT:

T-52-33-55



a66212 PIN LIST:

SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
ADRA(0)	A10	PO(0)	B11	ADRC(4)	R5	ADRD(0)	C3	MUXRW	F14	IP(0)	C8
ADRA(1)	G2	PO(1)	F2	ADRC(5)	L2	ADRD(1)	B1	NFT	B14	IP(1)	B10
ADRA(2)	C9	PO(2)	A12	ADRC(6)	N5	ADRD(2)	C2	NFTS	P9	IP(2)	A11
ADRA(3)	F1	PO(3)	F3	ADRC(7)	L3	ADRD(3)	R6	OBUSY	L15	IP(3)	B8
ADRA(4)	G3	PO(4)	C15	ADRC(8)	K1	ADRD(4)	C1	OCLK	N9	IP(4)	D14
ADRA(5)	B9	PO(5)	A14	ADRC(9)	P5	ADRD(5)	P8	OE'	A1	QAS0	R10
ADRA(6)	A8	PO(6)	C14	ADRC(10)	K3	ADRD(6)	D2	OEMPTY	R4	QAS1	H15
ADRA(7)	A9	PO(7)	B13	ADRC(11)	N8	ADRD(7)	R7	OVACS'	F13	QAS2	A4
ADRA(8)	P2	BOP	N15	ADRC(12)	N1	ADRD(8)	E3	OVAWE'	P14	QAS3	P4
ADRA(9)	N3	EOP	L13	ADRC(13)	P7	ADRD(9)	D1	OVBCS'	H14	AUTOBOOT	M15
ADRA(10)	R1	CLKIN	C13	ADRC(14)	M2	ADRD(10)	N7	OVBWE'	J13	BOOTDONE	R15
ADRA(11)	R2	CLKOUT	E15	ADRC(15)	N2	ADRD(11)	E2	RST'	A15	GO	N13
ADRA(12)	P1	ADRB(8)	N10	MCLKOUT	H13	ADRD(12)	N6	ADRX(8)	B15	SIN	G15
ADRA(13)	R3	ADRB(9)	H1	AWE'	L14	ADRD(13)	E1	ADRX(9)	A3	SOUT	R9
ADRA(14)	M1	ADRB(10)	R11	BWE'	K14	ADRD(14)	P6	ADRX(10)	C5	WR'	B2
ADRA(15)	P3	ADRB(11)	H3	CWE'	J14	ADRD(15)	J3	ADRX(11)	B7	SYNC	F15
ADRB(0)	P11	ADRB(12)	C11	DWE'	J15	ADRX(0)	B3	ADRX(12)	A7	VCC	C4
ADRB(1)	J2	ADRB(13)	H2	CS'	R13	ADRX(1)	A2	ADRX(13)	C10	VCC	D3
ADRB(2)	R8	ADRB(14)	B12	EOPR	N14	ADRX(2)	B5	ADRX(14)	R14	VCC	C12
ADRB(3)	J1	ADRB(15)	G1	HCLK	K13	ADRX(3)	C6	ADRX(15)	P13	VCC	D13
ADRB(4)	A13	ADRC(0)	G14	IBUSY	P15	ADRX(4)	A5	BSC(0)	E14	GND	M13
ADRB(5)	P12	ADRC(1)	G13	ICLK	K15	ADRX(5)	C7	BSC(1)	D15	GND	N12
ADRB(6)	N11	ADRC(2)	K2	IFULL	M14	ADRX(6)	A6	BSC(2)	B4	GND	M3
ADRB(7)	R12	ADRC(3)	L1	INITPR	P10	ADRX(7)	B6	BSC(3)	E13	GND	N4

a66212

a66212 ORDERING INFORMATION:

T-52-33-55

PART NUMBER	SPEED	PROCESSING	TEMPERATURE RANGE	VOLTAGE RANGE	PINS	PACKAGE TYPE
a66212ACG	40MHz	Commercial	0° C to +70° C	4.75V to 5.25V	144	PGA
a66212BCG	30MHz	Commercial	0° C to +70° C	4.75V to 5.25V	144	PGA
a66212BIG	30MHz	Commercial	-40° C to +85° C	4.50V to 5.50V	144	PGA
a66212BEG	30MHz	Commercial	-55° C to +125° C	4.50V to 5.50V	144	PGA
			Advance Information			
a66212BMG	30MHz	MIL STD 883C	-55° C to +125° C	4.50V to 5.50V	144	PGA

WARNING - LIFE SUPPORT APPLICATIONS POLICY
array Microsystems' products should not be used within Life Support Systems without the specific written consent of array Microsystems, Inc. A Life Support System is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in significant personal injury or death..

NOTICE - APPLICATIONS SUPPORT POLICY
array Microsystems Inc. assumes no liability for applications assistance or customer product design.

NOTICE - PRODUCT AVAILABILITY
array Microsystems Inc. reserves the right to make changes to product specifications or to discontinue products without notice.

*Permission is hereby expressly granted to copy this publication for informational purposes only. Copying this material for any other use is strictly prohibited.

array Microsystems, Inc 1420 Quail Lake Loop Colorado Springs, CO 80906 Telephone: +1 (719) 540-7900 FAX +1 (719) 540-7950 Rev 1.2 - 03/93