T-46-07-27

>> 32-bit bus interface latches, non-inverting or inverting.

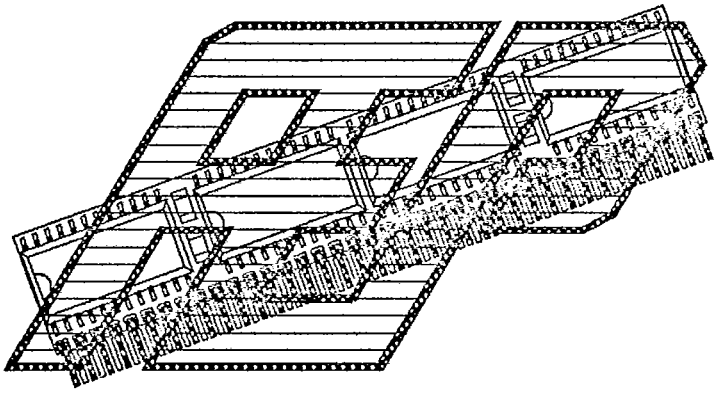
>> High density .070 center spaced ZIP leads for maximum I/O in minimum area.

>> Space saving vertical mounting orientation.

>> Convenient "in one side, out the other" broadside pin-out.

>> TTL compatible

>> Uses single +5V power supply



32 LINE LATCH MODULE

DESCRIPTION:

The AEPLZ32 is a high speed,high density 32-line latch module ideal for use with 16 or 32-bit wide address/data paths or buses. It combines the advantages of the 845 (non-inverting) or 846 (inverting) type parallel latch ICs with very large data widths and a board-space saving configuration. The vertical mounting orientation and compact I/O pin footprint make it superb for projects with tight space constraints.

Physically the module consists of an FR4 PC material substrate mounted with four 845 or 846 type latch ICs, four 0.10 microfarad decoupling capacitors, and 75 I/O pins in a staggered ZIP package format. It can be ordered with any 845 or 846 type parallel latches made by any manufacturer producing them in a 24 pin SOP package. The module features two Preset pins and two Output Enable pins controlling two sets of sixteen outputs. Overall Output Enable, Master Reset, and Latch Enable pins are also used.

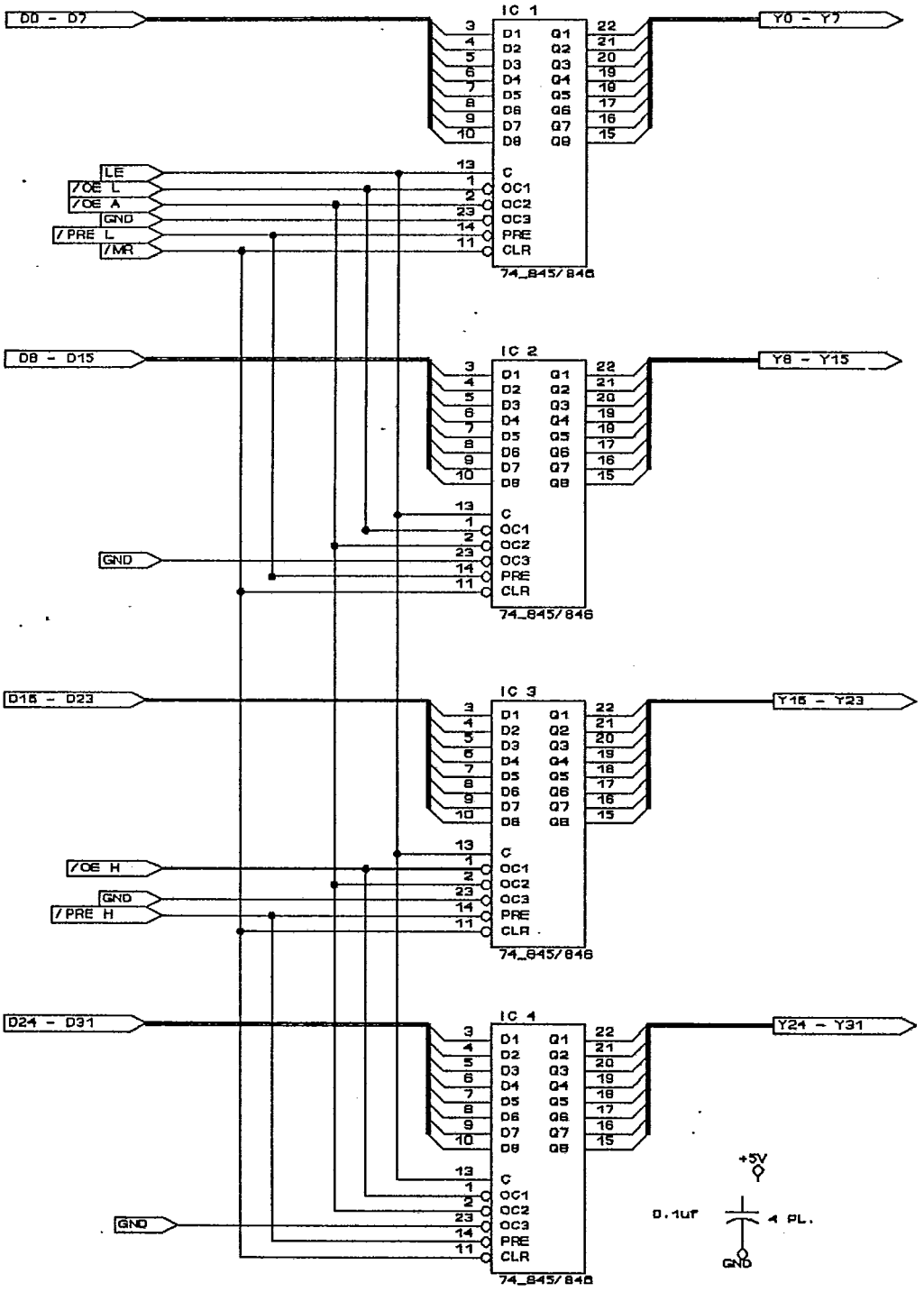
Performance specifications and electrical characteristics are determined by the IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors' data sheets, like those attached, or from their data books.

Mechanical dimensions are 0.505 inch high by 2.66 inches long by 0.22 inch wide. The I/O pins are in two rows which are 0.1 inch apart and offset longitudinally 0.035 inch. In each row the pins are on 0.070 inch center spacing. See included specification drawing.

The AEPLZ32 is one of a family of digital circuit support function modules which includes a 32 line buffer, a 32 line transceiver, and a 32 line register module. These are natural companions for AEP memory modules.

32 LINE LATCH MODULE
AEPLZ32
FUNCTIONAL DIAGRAM

T-46-07-27



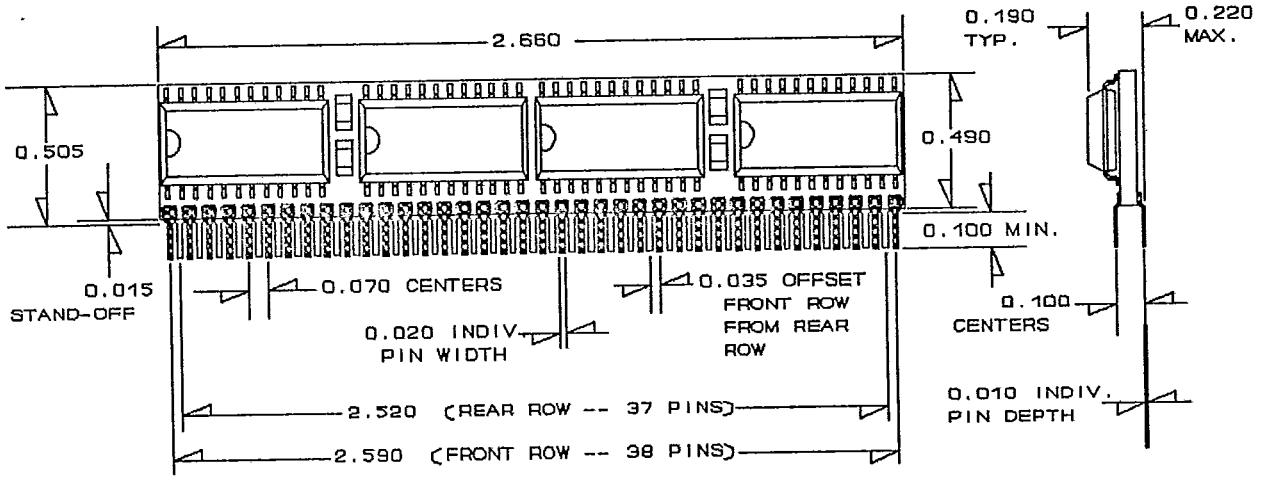
T-90-20

AEP 32 LINE MODULE SERIES PACKAGING INFORMATION

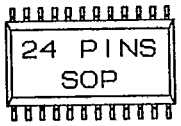
SPECIFICATION DRAWING

APPLY TO: BZ, LZ, RZ, TZ, SRZ, TRZ, CZ

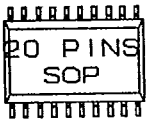
DIMENSIONS IN INCHES, TOLERANCE: +/- 0.010 UNLESS SPECIFIED.



75 PINS TOTAL

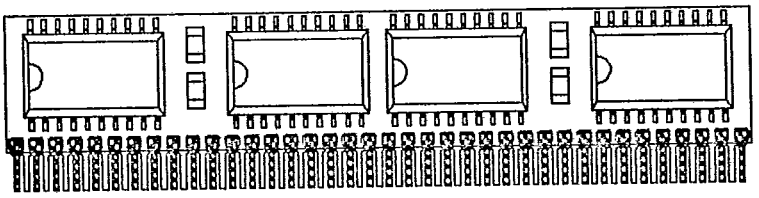


IC FOR LZ
RZ
SRZ
TRZ



IC FOR BZ
CZ
TZ

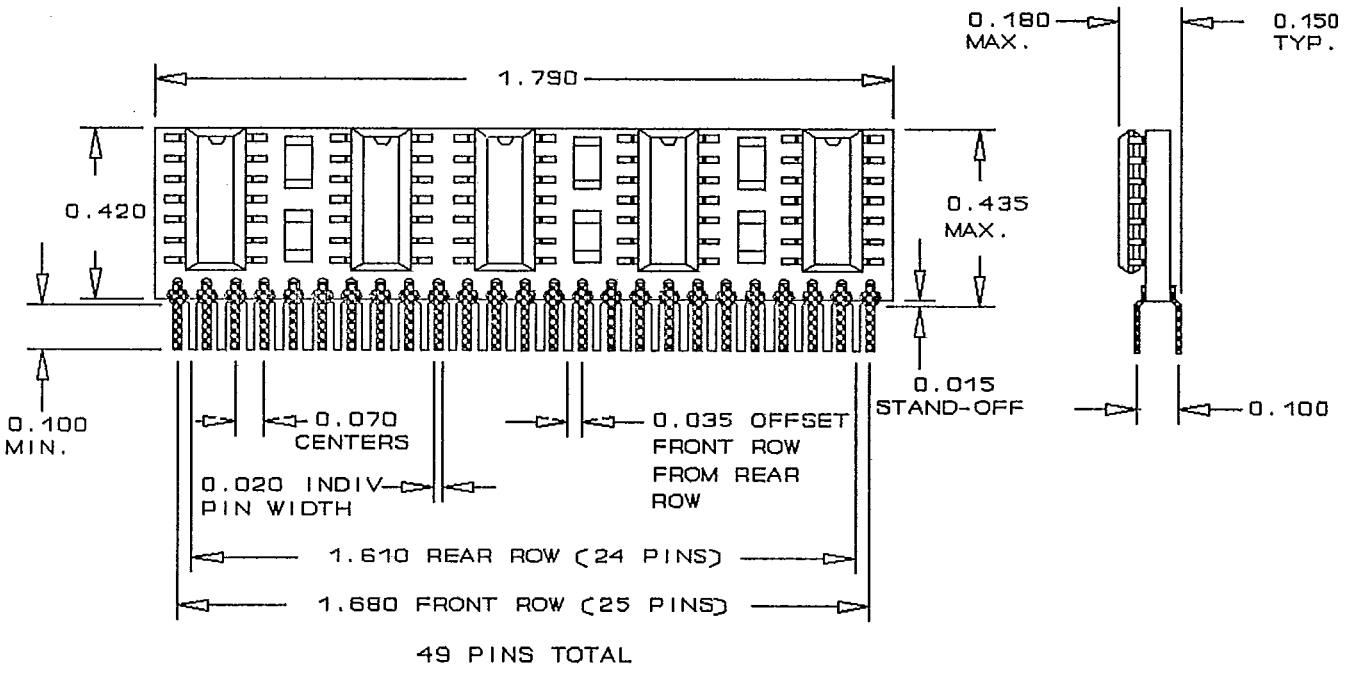
** MODULE DIMENSIONS REMAIN UNCHANGE.



AEP 32 LINE SUPPORT MODULE SERIES
PARITY GENERATOR/CHECKER
PACKAGING INFORMATION

APPLY TO: PZ-286, PZ-280

DIMENSIONS IN INCHES, TOLERANCE: +/- 0.010 UNLESS SPECIFIED.



The AEPPZ32-280 uses only one pull up resistor and 3 capacitors.
The AEPPZ32-286 uses three pull up resistors and 3 capacitors.