

## Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C512R
- Low Power 3-Volt CMOS Operation
  - 100  $\mu$ A max. Standby
  - 26 mW max. Active at 1 MHz for  $V_{CC} = 3.3$  VDC
  - 110 mW max. Active at 5 MHz for  $V_{CC} = 5.5$  VDC
- Read Access Time - 200 ns
- Wide Selection of JEDEC Standard Packages including OTP
  - 28-Lead, 600-mil Cerdip and OTP Plastic DIP, SOIC or TSOP
  - 32-Pad LCC, 32-Lead JLCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100  $\mu$ s/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

## Description

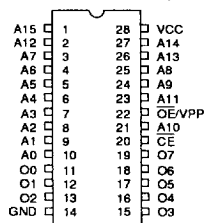
The AT27LV512R chip is a low power, low voltage 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18 mW at 1 MHz and  $V_{CC}$  at 3.3 VDC, the AT27LV512R will draw less than one fifth the power of a standard 5-volt EPROM. Standby mode supply current is typically less than 10  $\mu$ A.

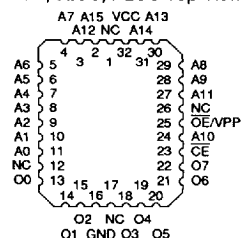
## Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable
NC	No Connect

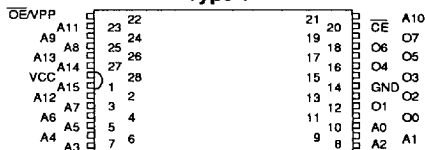
CDIP, PDIP, SOIC Top View



LCC, JLCC, PLCC Top View



TSOP Top View  
Type 1



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.



**512K (64K x 8)  
Low Voltage  
UV  
Erasable  
CMOS  
EPROM**

## Description (Continued)

The AT27LV512R comes in a choice of industry standard JEDEC-approved through hole and surface mount packages including windowed and one time programmable (OTP) packages, such as the OTP thin small outline package (TSOP). All devices feature two line control ( $\overline{CE}$ ,  $\overline{OE}$ ) to give designers the flexibility to prevent bus contention.

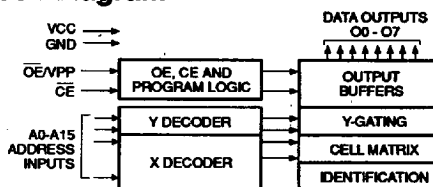
The AT27LV512R operating with  $V_{CC}$  at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at  $V_{CC} = 5.0$  VDC.

Atmel's 27LV512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100  $\mu$ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV512R programs identically as an AT27C512R.

## Erase Characteristics

The entire memory array of the AT27LV512R is erased (all outputs read as  $V_{OH}$ ) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000  $\mu$ W/cm<sup>2</sup> intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W-sec/cm<sup>2</sup>. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias .....	-40°C to +85°C
Storage Temperature .....	-65°C to +125°C
Voltage on Any Pin with Respect to Ground .....	-2.0 V to +7.0 V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0 V to +14.0 V <sup>(1)</sup>
V <sub>PP</sub> Supply Voltage with Respect to Ground .....	-2.0 V to +14.0 V <sup>(1)</sup>
Integrated UV Erase Dose .....	7258 W-sec/cm <sup>2</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Notes:

1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75$  V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

## Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V <sub>CC</sub>	Outputs
Read	V <sub>IL</sub>	V <sub>IL</sub>	Ai	V <sub>CC</sub>	DOUT
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	X <sup>(1)</sup>	V <sub>CC</sub>	High Z
Standby	V <sub>IH</sub>	X	X	V <sub>CC</sub>	High Z
Rapid Program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>PP</sub>	Ai	V <sub>CC</sub> <sup>(2)</sup>	DIN
PGM Verify <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	Ai	V <sub>CC</sub> <sup>(2)</sup>	DOUT
PGM Inhibit <sup>(2)</sup>	V <sub>IH</sub>	V <sub>PP</sub>	X	V <sub>CC</sub> <sup>(2)</sup>	High Z
Product Identification <sup>(2),(4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A9 = V <sub>H</sub> <sup>(3)</sup> A0 = V <sub>IL</sub> or V <sub>IL</sub> A1-A15 = V <sub>IL</sub>	V <sub>CC</sub> <sup>(2)</sup>	Identification Code

- Notes:
1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  2. Refer to Programming characteristics. Programming modes require  $V_{CC} > 4.5$  V.
  3. V<sub>H</sub> = 12.0  $\pm$  0.5 V.

4. Two identifier bytes may be selected. All Ai inputs are held low (V<sub>IL</sub>), except A9 which is set to V<sub>H</sub> and A0 which is toggled low (V<sub>IL</sub>) to select the Manufacturer's Identification byte and high (V<sub>IH</sub>) to select the Device Code byte.

## D.C. and A.C. Operating Conditions for Read Operation

AT27LV512R			
		-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V

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## D.C. and Operating Characteristics for Read Operation

(V<sub>CC</sub> = 3.0 V to 5.5 V unless otherwise specified)

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = -0.1 V to V <sub>CC</sub> +1 V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = -0.1 V to V <sub>CC</sub> +0.1 V		10	μA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), CE = V <sub>CC</sub> -0.3 to V <sub>CC</sub> +1.0 V		100	μA
		I <sub>SB2</sub> (TTL), CE = 2.0 to V <sub>CC</sub> +1.0 V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	I <sub>CC1</sub> f = 5 MHz, I <sub>OUT</sub> = 0 mA, CE = V <sub>IL</sub> , V <sub>CC</sub> = 5.5 V	Com.	20	mA
			Ind.	25	mA
		I <sub>CC2</sub> f = 1 MHz, I <sub>OUT</sub> = 0 mA CE = V <sub>IL</sub> , V <sub>CC</sub> = 3.3 V	Com.	8	mA
			Ind.	10	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> +0.75	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> -0.3	V
		I <sub>OH</sub> = -400 μA		2.4	V

Notes: 1. V<sub>CC</sub> must be applied simultaneously or before OE/V<sub>PP</sub>, and removed simultaneously or after OE/V<sub>PP</sub>.

## A.C. Characteristics for Read Operation (V<sub>CC</sub> = 3.0 V to 5.5 V)

				AT27LV512R				
				-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Units
t <sub>ACC</sub> <sup>(3)</sup>	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	Com.		200		250	ns
			Ind.		200		250	ns
t <sub>CE</sub> <sup>(2)</sup>	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$			200		250	ns
t <sub>OE</sub> <sup>(2,3)</sup>	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$			70		100	ns
t <sub>DF</sub> <sup>(4,5)</sup>	$\overline{OE}/V_{PP}$ High to Output Float	$\overline{CE} = V_{IL}$			50		50	ns
t <sub>OH</sub>	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ , whichever occurred first	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		0		0		ns

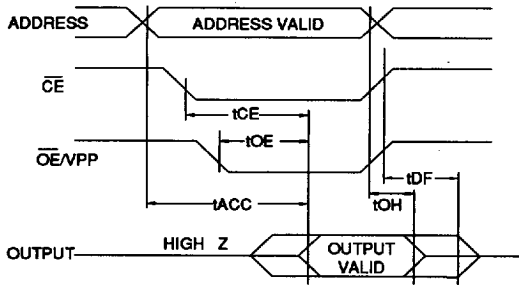
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.



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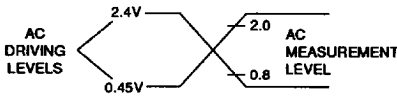
## A.C. Waveforms for Read Operation <sup>(1)</sup>



### Notes:

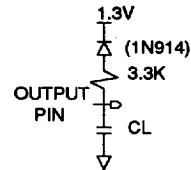
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V. See Input Test Waveforms and Measurement Levels.
2.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{CE}-t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
3.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{ACC}-t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

## Input Test Waveforms and Measurement Levels



$t_R, t_F < 20$  ns (10% to 90%)

## Output Test Load



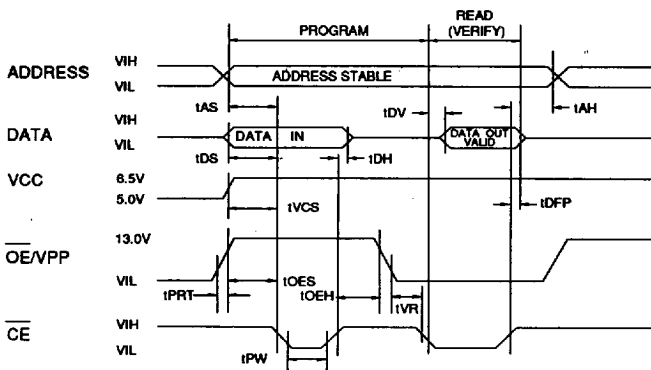
Note:  $C_L = 100$  pF including jig capacitance.

## Pin Capacitance ( $f = 1$ MHz, $T = 25^\circ\text{C}$ ) <sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	4	8	pF	$V_{IN} = 0$ V
$C_{OUT}$	8	12	pF	$V_{OUT} = 0$ V

Notes: 1. Typical values for 5-V supply voltage. This parameter is only sampled and is not 100% tested.

## Programming Waveforms <sup>(1)</sup>



### Notes:

1. The Input Timing Reference is 0.8 V for  $V_{IL}$  and 2.0 V for  $V_{IH}$ .
2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.

## D.C. Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{ V}$ ,  $\overline{OE}/V_{PP} = 13.0 \pm 0.25\text{ V}$

Sym- bol	Parameter	Test Conditions	Limits		Units
			Min	Max	
ILI	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	$\mu\text{A}$
VIL	Input Low Level	(All Inputs)	-0.6	0.8	V
VIH	Input High Level		2.0	$V_{CC}+1$	V
VOL	Output Low Volt.	$I_{OL} = 2.1\text{ mA}$		.45	V
VOH	Output High Volt.	$I_{OH} = -400\text{ }\mu\text{A}$	2.4		V
ICC2	VCC Supply Current (Program and Verify)			25	mA
Ipp2	$\overline{OE}/V_{PP}$ Current	$\overline{CE} = V_{IL}$		25	mA
VID	A9 Product Identification Voltage		11.5	12.5	V

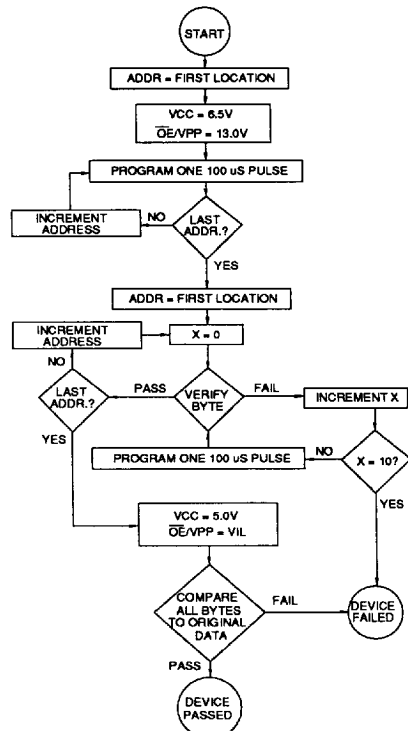
## Atmel's 27LV512R Integrated Product Identification Code<sup>(1)</sup>

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Note: 1. The AT27LV512R has the same Product Identification Code as the AT27C512R. Both are programming compatible.

## Rapid Programming Algorithm

A 100  $\mu\text{s}$   $\overline{CE}$  pulse width is used to program. The address is set to the first location.  $V_{CC}$  is raised to 6.5 V and  $\overline{OE}/V_{PP}$  is raised to 13.0 V. Each address is first programmed with one 100  $\mu\text{s}$   $\overline{CE}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100  $\mu\text{s}$  pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $\overline{OE}/V_{PP}$  is then lowered to  $V_{IL}$  and  $V_{CC}$  to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.



## A.C. Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{ V}$ ,  $\overline{OE}/V_{PP} = 13.0 \pm 0.25\text{ V}$

Sym- bol	Parameter	Test Conditions* (see Note 1)	Limits		Units
			Min	Max	
tAS	Address Setup Time		2		$\mu\text{s}$
toES	$\overline{OE}/V_{PP}$ Setup Time		2		$\mu\text{s}$
toEH	$\overline{OE}/V_{PP}$ Hold Time		2		$\mu\text{s}$
tDS	Data Setup Time		2		$\mu\text{s}$
tAH	Address Hold Time		0		$\mu\text{s}$
tDH	Data Hold Time		2		$\mu\text{s}$
tDFP	$\overline{CE}$ High to Out- put Float Delay	(Note 2)	0	130	ns
tvCS	VCC Setup Time		2		$\mu\text{s}$
tpW	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	$\mu\text{s}$
tDV	Data Valid from $\overline{CE}$	(Note 2)		1	$\mu\text{s}$
tVR	$\overline{OE}/V_{PP}$ Recovery Time		2		$\mu\text{s}$
tpRT	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

### \*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns  
 Input Pulse Levels ..... 0.45 V to 2.4 V  
 Input Timing Reference Level ..... 0.8 V to 2.0 V  
 Output Timing Reference Level ..... 0.8 V to 2.0 V

### Notes:

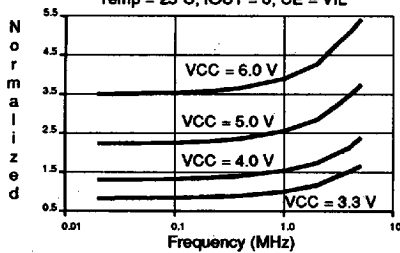
1.  $V_{CC}$  must be applied simultaneously or before  $\overline{OE}/V_{PP}$  and removed simultaneously or after  $\overline{OE}/V_{PP}$ .
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100  $\mu\text{sec} \pm 5\%$ .



## LV EPROM Product Characteristics

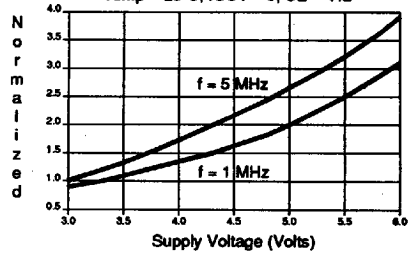
**NORMALIZED SUPPLY CURRENT vs. FREQUENCY**

Temp = 25°C, I<sub>OUT</sub> = 0,  $\overline{CE}$  = VIL

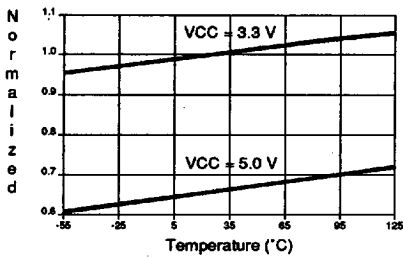


**NORMALIZED SUPPLY CURRENT vs. VOLTAGE**

Temp = 25°C, I<sub>OUT</sub> = 0,  $\overline{CE}$  = VIL

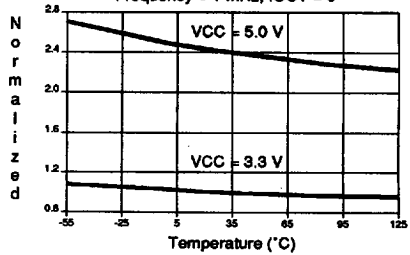


**NORMALIZED ACCESS TIME vs. TEMPERATURE**



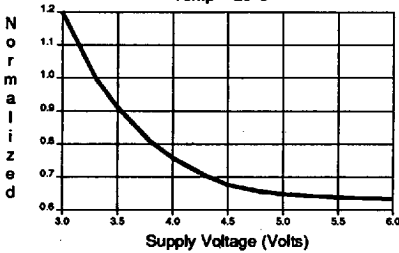
**NORMALIZED SUPPLY CURRENT vs. TEMP.**

Frequency = 1 MHz, I<sub>OUT</sub> = 0



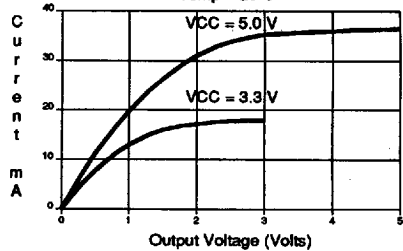
**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**

Temp = 25°C



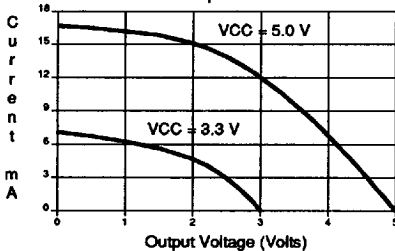
**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**

Temp = 25°C



**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**

Temp = 25°C



**Ordering Information**

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA) V <sub>CC</sub> = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV512R-20DC AT27LV512R-20JC AT27LV512R-20KC AT27LV512R-20LC AT27LV512R-20PC AT27LV512R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	10	0.1	AT27LV512R-20DI AT27LV512R-20KI AT27LV512R-20LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
250	8	0.1	AT27LV512R-25DC AT27LV512R-25JC AT27LV512R-25KC AT27LV512R-25LC AT27LV512R-25PC AT27LV512R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	10	0.1	AT27LV512R-25DI AT27LV512R-25KI AT27LV512R-25LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)

**4**

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA) V <sub>CC</sub> = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV512R-20TC	28T	Commercial (0° to 70°C)
250	8	0.1	AT27LV512R-25TC	28T	Commercial (0° to 70°C)

Package Type	
<b>28DW6</b>	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
<b>32J</b>	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
<b>32KW</b>	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
<b>32LW</b>	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
<b>28P6</b>	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
<b>28R</b>	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
<b>28T</b>	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)


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