CMS68P256, CMS68P512, CMS68P1MB ONE TIME PROGRAMMABLE READ-ONLY MEMORY MEMORY CARDS

SMNS201E–JUNE 1992–REVISED DECEMBER 1992

T-81-27-90

- Industry Standard PCMCIA Cards
- Standard Card Size (85.6 mm × 54.0 mm × 3.3 mm)
- Single 5-V Power Supply (± 5% Tolerance)
- Utilize TSOP (Thin Small Outline Package) OTP PROM (One Time Programmable Read-Only Memory)
- 68-Pin PCMCIA (Rev. 2.0) / JEIDA (Rev. 4.1) Compatible
- 8-Bit or 16-Bit User-Configurable Organizations
- Low Power Dissipation
- Operating Free-Air Temperature Range 0°C to 55°C
- Standard 68 Pin Two-Piece Connector
- All Inputs and Outputs are Fully TTL Compatible
- 3-State Output

68-PIN MEMORY CARD† (CONNECTOR VIEW)

GND	1	35	GND
D3	2	36	$\overline{CD1}$
D4	3	37	D11
D5	4	38	D12
D6	5	39	D13
D7	6	40	D14
$\overline{CE1}$	7	41	D15
A10	8	42	$\overline{CE2}$
$\overline{OE}$	9	43	NC
A11	10	44	NC
A9	11	45	NC
A8	12	46	A17
A13	13	47	A18
A14	14	48	A19
$\overline{PGM}$	15	49	NC
NC	16	50	NC
V_{CC}	17	51	V_{CC}
V_{PP1}	18	52	V_{PP2}
A16	19	53	NC
A15	20	54	NC
A12	21	55	NC
A7	22	56	NC
A6	23	57	NC
A5	24	58	NC
A4	25	59	NC
A3	26	60	NC
A2	27	61	$\overline{REG}$
A1	28	62	NC
A0	29	63	NC
D0	30	64	D8
D1	31	65	D9
D2	32	66	D10
WP	33	67	$\overline{CD2}$
GND	34	68	GND

NC = No internal connection.

† Pinout shown is for maximum density card. See pin assignment table for specifics.

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description

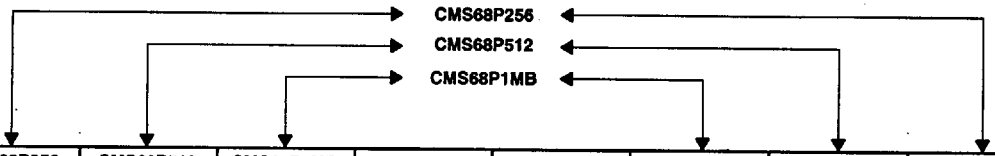
The CMS68Pxxx series are TI Standard Memory Cards designed to be used either as an internal memory system or as external add-on memory according to PCMCIA/JEIDA industry standard card specifications. These cards are offered with a memory size from 256K bytes to 1024K bytes of one time electrically programmable read only memory, and the card organization (×8 or ×16) is directly user-configurable. The cards comprise 2, 4, or 8 TMS27PC010As, each in a 32-lead plastic thin small outline package (TSOP). Refer to the TMS27PC010A data sheet for more information.

available organizations

PART NUMBER	ORGANIZATION	ACCESS TIME	TOTAL DENSITY	CONNECTOR
CMS68P256-200, CMS68P256N-200‡	256K × 8 / 128K × 16	200 ns	256K-Bytes	Two-piece, 68 pin
CMS68P512-200, CMS68P512N-200‡	512K × 8 / 256K × 16	200 ns	512K-Bytes	Two-piece, 68 pin
CMS68P1MB-200, CMS68P1MBN-200‡	1 MEG × 8 / 512K × 16	200 ns	1024K-Bytes	Two-piece, 68 pin

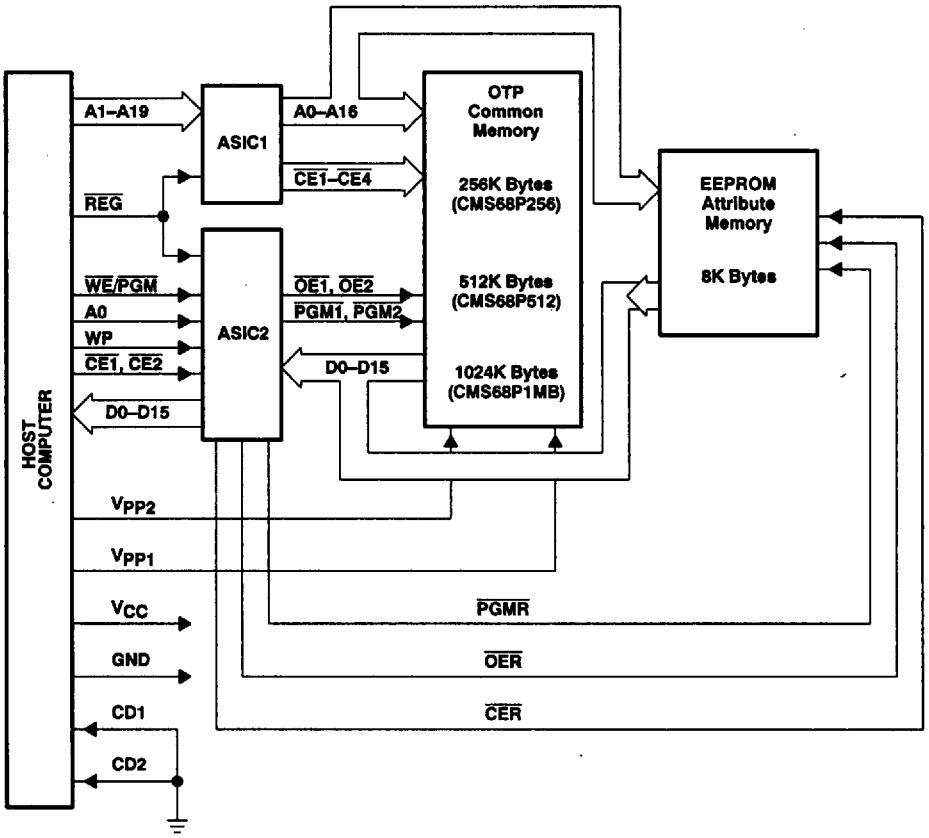
‡ CMS68PxxxN devices do not include attribute memory.

pin assignments



CMS68P256	CMS68P512	CMS68P1MB	PIN NUMBER	PIN NUMBER	CMS68P1MB	CMS68P512	CMS68P256
GND	GND	GND	1	35	GND	GND	GND
D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	3	37	D11	D11	D11
D5	D5	D5	4	38	D12	D12	D12
D6	D6	D6	5	39	D13	D13	D13
D7	D7	D7	6	40	D14	D14	D14
$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15	D15
A10	A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC
A11	A11	A11	10	44	NC	NC	NC
A9	A9	A9	11	45	NC	NC	NC
A8	A8	A8	12	46	A17	A17	A17
A13	A13	A13	13	47	A18	A18	NC
A14	A14	A14	14	48	A19	NC	NC
$\overline{PGM}$	$\overline{PGM}$	$\overline{PGM}$	15	49	NC	NC	NC
NC	NC	NC	16	50	NC	NC	NC
V_{CC}	V_{CC}	V_{CC}	17	51	V_{CC}	V_{CC}	V_{CC}
V_{PP1}	V_{PP1}	V_{PP1}	18	52	V_{PP2}	V_{PP2}	V_{PP2}
A16	A16	A16	19	53	NC	NC	NC
A15	A15	A15	20	54	NC	NC	NC
A12	A12	A12	21	55	NC	NC	NC
A7	A7	A7	22	56	NC	NC	NC
A6	A6	A6	23	57	NC	NC	NC
A5	A5	A5	24	58	NC	NC	NC
A4	A4	A4	25	59	NC	NC	NC
A3	A3	A3	26	60	NC	NC	NC
A2	A2	A2	27	61	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
A1	A1	A1	28	62	NC	NC	NC
A0	A0	A0	29	63	NC	NC	NC
D0	D0	D0	30	64	D8	D8	D8
D1	D1	D1	31	65	D9	D9	D9
D2	D2	D2	32	66	D10	D10	D10
WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	34	68	GND	GND	GND

functional block diagram



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pin description

SYMBOL	FUNCTION
A0–A19	Address inputs. Lines driven by the host which enable direct addressing of up to 1 megabyte of memory. Signal A0 is not used in word access mode. Signal A19 is the most significant bit.
D0–D15	Bidirectional data bus. The most significant bit is D15. Bit number and significance decrease downward to D0.
$\overline{CE1}$, $\overline{CE2}$	Active-low card. Enables signals driven by the host; $\overline{CE1}$ is used to enable even bytes, $\overline{CE2}$ to enable odd bytes. A multiplexing scheme based on A0, $\overline{CE1}$, and $\overline{CE2}$ allows 8-bit hosts to access all data on D0–D7 if desired.
$\overline{OE}$	Active-low signal. Driven by the host; used to gate memory-read data from the memory card.
$\overline{PGM}$	Programming enable signal.
V_{PP1}	Programming voltage 1.
V_{PP2}	Programming voltage 2.
$\overline{CD1}$, $\overline{CD2}$	Card detect. Signals for proper memory card insertion detection. The signals are connected to ground internally on the memory card.
WP	Write protect. Status signal of write protect. Switch on the memory card.
$\overline{REG}$	When active access to the memory card is limited to Attribute Memory used to record capacity and other configuration and attribute information.
V_{CC}	Power supply.
GND	Ground.
NC	No connection.

function table

FUNCTION MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{PGM}$	V_{PP2}	V_{PP1}	D8–D15	D0–D7
Standby	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Read (x8)	H H	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY OD-BY
Read (x16)	H	L	L	X	L	H	V_{CC}	V_{CC}	OD-BY	EV-BY
OD-BY Read	H	L	H	X	L	H	V_{CC}	V_{CC}	OD-BY	HI-Z
Write (x8)	H H	H H	L L	L H	H H	L L	V_{CC} V_{PP}	V_{PP} V_{CC}	XXX XXX	EV-BY OD-BY
Write (x16)	H	L	L	X	H	L	V_{PP}	V_{PP}	OD-BY	EV-BY
OD-BY Write	H	L	H	X	H	L	V_{PP}	V_{CC}	OD-BY	XXX

EV-BY = Even Byte
OD-BY = Odd Byte
HI-Z = High Impedance
X = V_{IL} or V_{IH}
XXX = Don't Care

attribute memory read function

FUNCTION MODE	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	A0	$\overline{OE}$	$\overline{WE}$	V_{PP2}	V_{PP1}	D8–D15	D0–D7
Standby Mode	X	H	H	X	X	X	V_{CC}	V_{CC}	HI-Z	HI-Z
Byte access (8 bits)	L L	H H	L L	L H	L L	H H	V_{CC} V_{CC}	V_{CC} V_{CC}	HI-Z HI-Z	EV-BY Not Valid
Byte access (16 bits)	L	L	L	X	L	H	V_{CC}	V_{CC}	Not Valid	EV-BY
Odd-byte-only access	L	L	H	X	L	H	V_{CC}	V_{CC}	Not Valid	HI-Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.5 to 14 V
Input voltage range, (see Note 1) ..... – 0.5 to 6.5 V
Output voltage range, (see Note 1) ..... – 0.5 to V_{CC}
Operating free-air temperature range ..... – 0°C to 55°C
Storage temperature range ..... – 40°C to 70°C
Connector insertion cycles 10 000

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

				MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.75	5	5.25	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL	2.0		V_{CC} + 0.5	V
			CMOS	V_{CC} – 0.2		V_{CC} + 0.5	V
V_{IL}	Low-level input voltage		TTL	– 0.5		0.8	V
			CMOS	– 0.5		GND + 0.2	V
T_A	Operating free-air temperature			0		55	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over full range of operating conditions

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage (except WP)		I_{OH} = 12 mA, V_I = 0.9 V_{CC}	3.7		V
			I_{OH} = 1.2 mA, V_I = 0.9 V_{CC}	4.4		
V_{OL}	Low-level output voltage (except CD1, CD2)		I_{OL} = 12 mA, V_I = 0.1 V_{CC}		0.5	V
			I_{OL} = 1.2 mA, V_I = 0.1 V_{CC}		0.1	
I_I	Input current (leakage)		V_I = 0 to 5.25 V		±1	µA
I_O	Output current (leakage)		V_O = 0 to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.25 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.25 V, $\overline{CEx}$ = V_{IH}		10	mA
		CMOS-input level	V_{CC} = 5.25 V, $\overline{CEx}$ = V_{CC} ± 0.2 V		2	
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.25 V, $\overline{CEx}$ = V_{IL}, t_{cycle} = Minimum cycle time†, outputs open		100	mA

† Minimum cycle time = maximum access time.

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capacitance over recommended ranges of supply voltage and free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	V_I = 0, f = 1 MHz			80	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz			80	pF

† Capacitance measurements are made on sample basis only.

switching characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	MIN	MAX	UNIT
$t_{a(A)}$	Access time from address	CL = 100 pF, 1 Series 74 TTL load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		200	ns
$t_{a(E)}$	Access time from chip enable			200	ns
$t_{en(G)}$	Output enable time from $\overline{OE}$			75	ns
t_{dis}	Output disable time from $\overline{OE}$ or $\overline{CEx}$, whichever occurs first‡		0	60	ns
$t_{v(A)}$	Output data valid time after change of address $\overline{CEx}$ or $\overline{OE}$ whichever occurs first		0		ns

‡ Value calculated from 0.5 V delta to measured output level.

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing wave form).
5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{OE}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{OE}$			150	ns

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

			MIN	TYP	MAX	UNIT
$t_{w(GPM)}$	Program pulse duration	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Address setup time		2		10	µs
$t_{su(E)}$	$\overline{CE}$ setup time		2			µs
$t_{su(G)}$	$\overline{OE}$ setup time		2			µs
$t_{su(D)}$	Data setup time		2			µs
$t_{su(VPP)}$	V_{PP} setup time		2			µs
$t_{su(VCC)}$	V_{CC} setup time		2			µs
$t_{h(A)}$	Address hold time		0			µs
$t_{h(D)}$	Data hold time		2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing wave form).

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PARAMETER MEASUREMENT INFORMATION

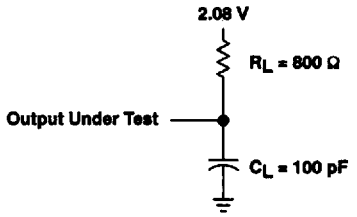
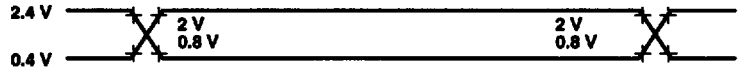


Figure 1. AC Test Output Load Circuit

AC testing Input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

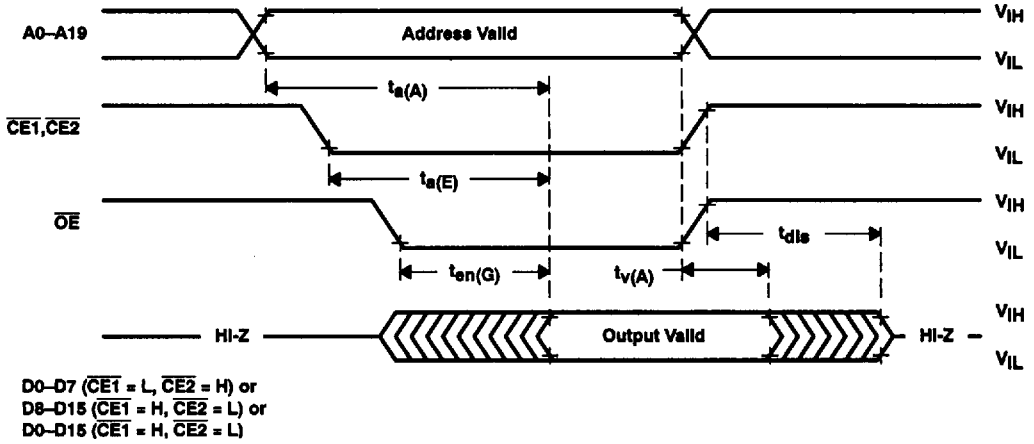


Figure 2. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

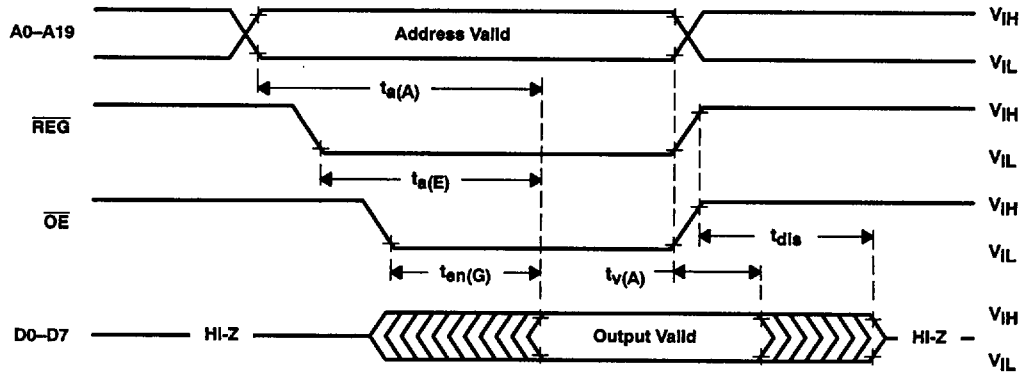
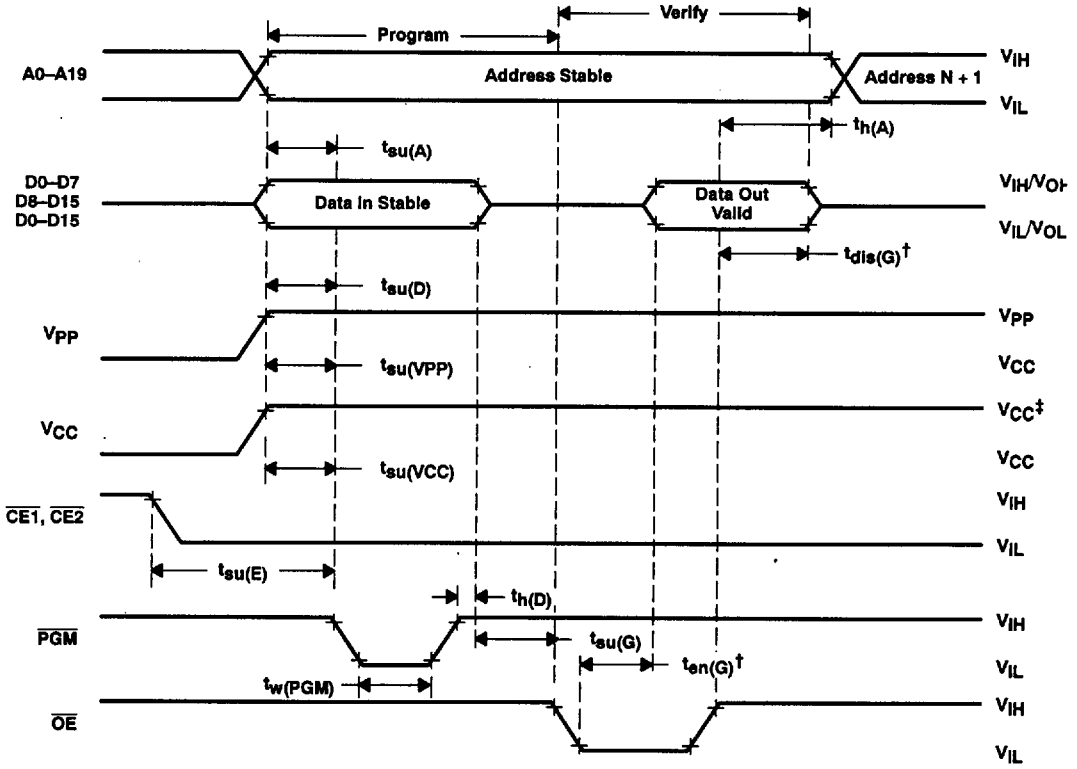


Figure 3. Attribute Memory Read Cycle Timing



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ V_{PP} = 13 V and V_{CC} = 6.5 V for SNAP! Pulse programming.

Figure 4. Program Cycle Timing (SNAP! Pulse Programming)

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PARAMETER MEASUREMENT INFORMATION

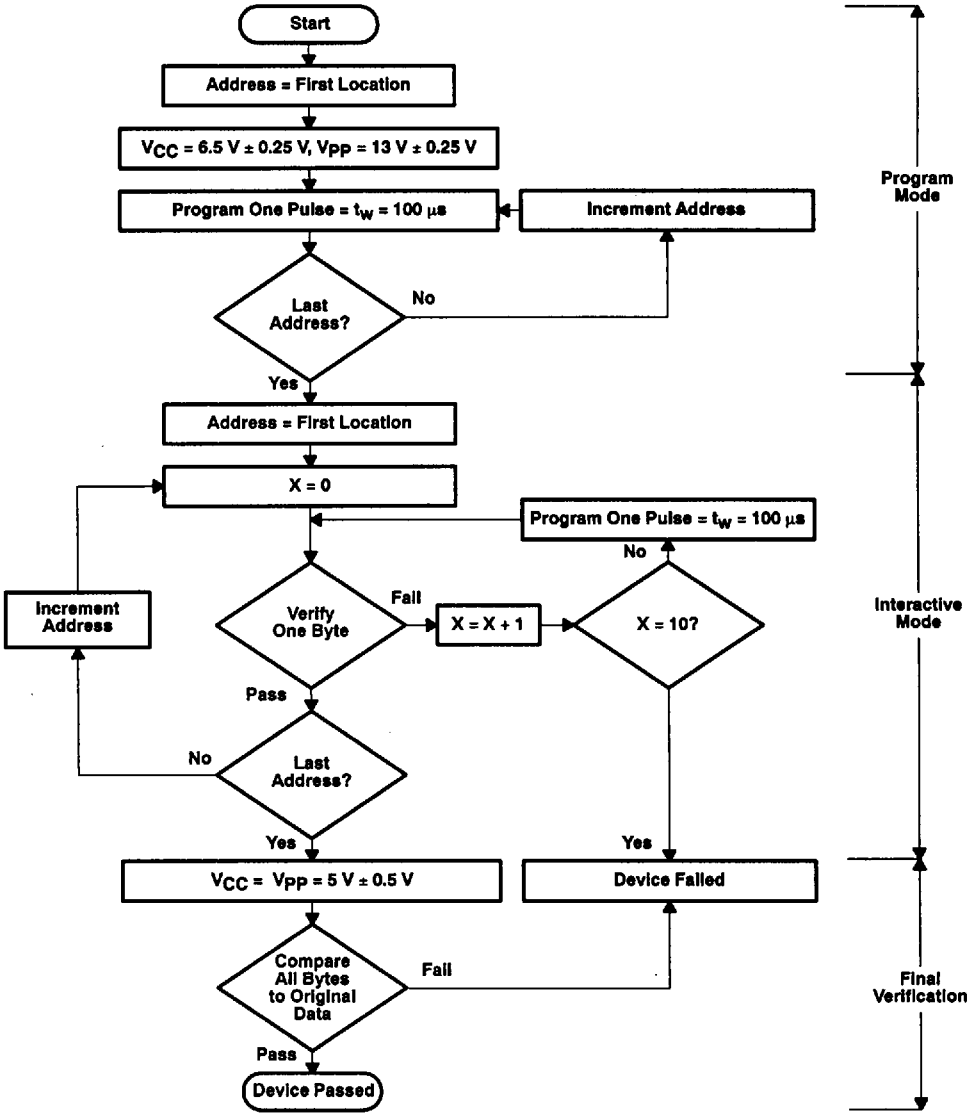

Figure 5. SNAP! Pulse Programming Flowchart

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