CYPRESS SEMICONDUCTOR

CY7C285

64K x 8 Reprogrammable Fast Column Access PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **Unique fast column access**
  - **— t_{AA} = 20 ns (commercial)**
  - **— t_{AA} = 25 ns (military)**
- **WAIT signal**
- **EPROM technology, 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Slim 300-mil package**
- **Capable of withstanding >2001V static discharge**

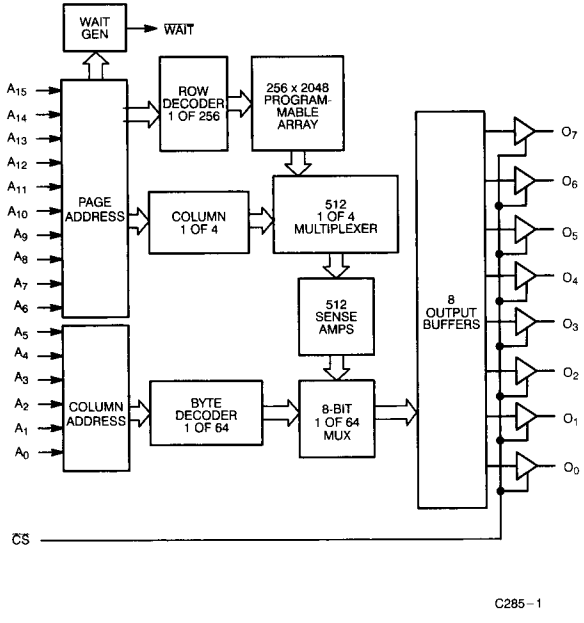
Functional Description

The CY7C285 is a high-performance 65,536 by 8-bit CMOS PROM. It is available in a 28-pin 300-mil package and features a unique fast column access feature that allow access times as fast as 20 ns for each byte in a 64-byte page. There are 1024 pages in the device. The access time when changing pages is 65 ns. In order to easily facilitate the use of the fast column access feature, a $\overline{WAIT}$ signal is generated to advise the processor of a page change.

The CY7C285 offers the advantage of low power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, allowing for each memory location to be 100% tested, with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the CY7C285 is accomplished by placing an active LOW signal on the $\overline{CS}$ pin. The contents of the memory location addressed by the address lines (A_0 – A_{15}) will become available on the output lines (O_0 – O_7).

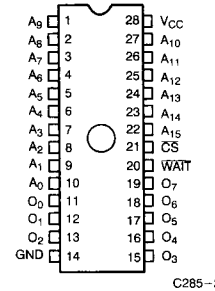
Logic Block Diagram



C285–1

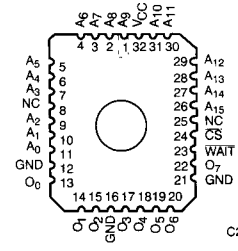
Pin Configurations

CerDIP
Top View



C285–2

LCC
Top View



C285–3

Selection Guide

Description		7C285–65	7C285–75	7C285–85
Maximum Access Time (ns)	Page Access Time	65	75	85
	Column Access Time	20	25	35
Maximum Operating Current (mA)	Commercial	180	180	180
	Military		200	200

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage (Pin 22) 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	− 40°C to +85°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3,4]

Parameter	Description	Test Conditions		7C285 Min.	7C285 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA[5]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
V_{CD}	Input Diode Clamp Voltage			Note 4		V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		− 40	+40	μA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		− 20	− 90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		180	mA
			Mil		200	mA

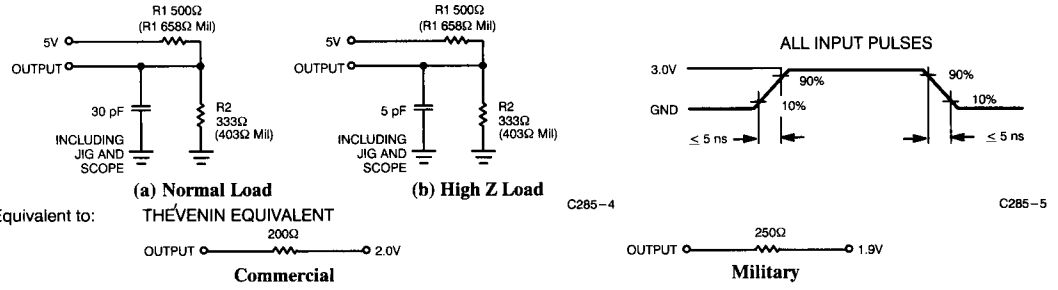
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Contact a Cypress representative for industrial temperature range specification.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs in this Data Book for general information on testing.
5. I_{OL} = 6.0 mA for military.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

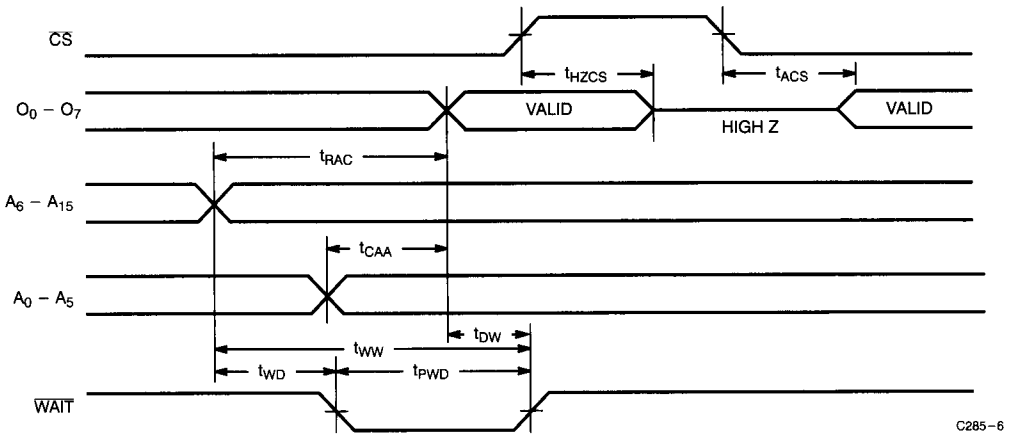
AC Test Loads and Waveform[4]



Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C285–65		7C285–75		7C285–85		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RAC}	Slow Address Access Time (A_6 – A_{15})		65		75		85	ns
t_{CAA}	Fast Address Access Time (A_0 – A_5)		20		25		35	ns
t_{HZCS}	Output High Z from $\overline{CS}$		15		20		25	ns
t_{ACS}	Output Valid from $\overline{CS}$		15		20		25	ns
t_{WD}	$\overline{WAIT}$ Delay from First Slow Address Change		20		25		35	ns
t_{DW}	$\overline{WAIT}$ Hold from Data Valid	0		0		0		ns
t_{WW}	$\overline{WAIT}$ Recovery from Last Address Change		90		110		120	ns
t_{PWD}	$\overline{WAIT}$ Pulse Width	10		12		15		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C285 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multipled by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The 7C285 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Mode Selection

	Pin Number				
	22	23	21	20	19–15, 13–11
Mode: Read or Output Disable	**A_{15}**	**A_{14}**	**$\overline{CS}$**	**$\overline{WAIT}$**	**$O_7 - O_0$**
Read (within a page: $A_6 - A_{15}$ stable)	A_{15}	A_{14}	V_{IL}	V_{OH}	$O_7 - O_0$
Read (page break: $A_6 - A_{15}$ transition)	A_{15}	A_{14}	V_{IL}	Pulse LOW	$O_7 - O_0$
Output Disable	A_{15}	A_{14}	V_{IH}	Output	High Z
Mode: Other	**V_{PP}**	**LATCH**	**$\overline{PGM}$**	**$\overline{VFY}$**	**$D_7 - D_0$**
Program	V_{PP}	V_{ILP}	V_{ILP}	V_{IHP}	$D_7 - D_0$
Program Inhibit	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}	High Z
Program Verify	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	$O_7 - O_0$
Blank Check	V_{PP}	V_{ILP}	V_{IHP}	V_{ILP}	Zeros

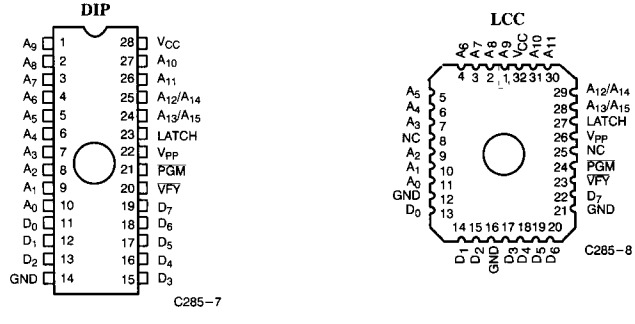


Figure 1. Programming Pinouts

Ordering Information[7]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
65	CY7C285-65PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C285-65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
75	CY7C285-75PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C285-75WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C285-75DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C285-75LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C285-75QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C285-75WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
85	CY7C285-85PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C285-85WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C285-85DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C285-85LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C285-85QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C285-85WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
7. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{CAA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11

Document #: 38-00097-G

CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

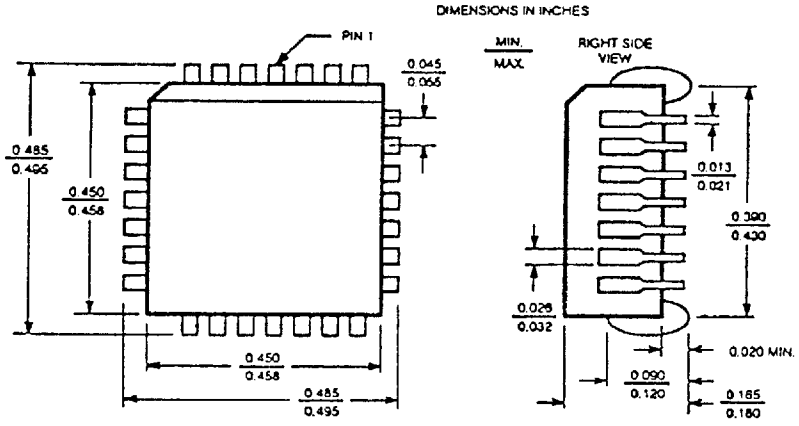
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

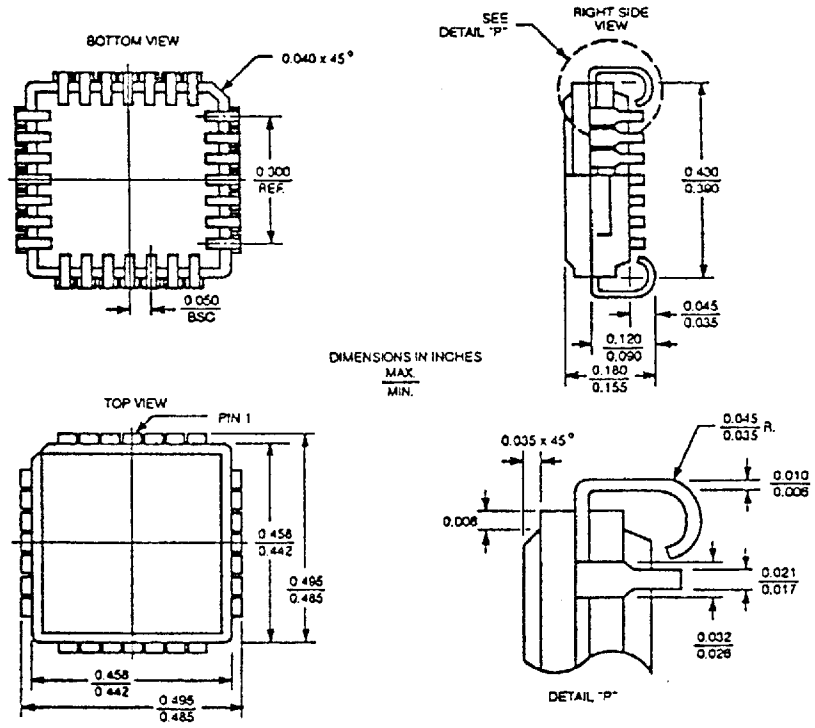


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

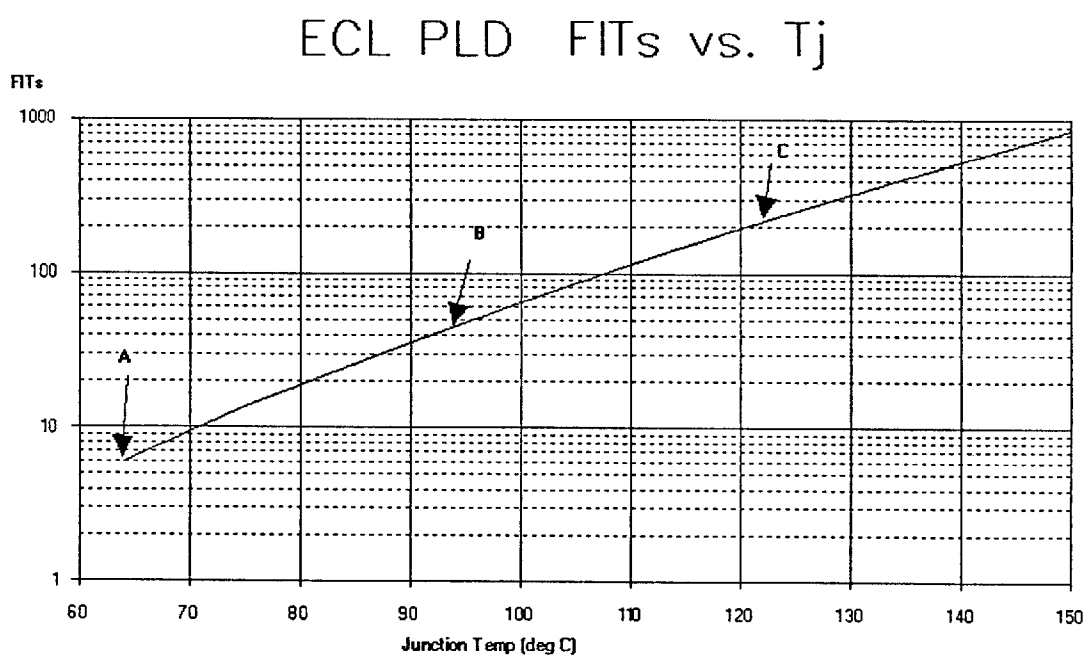


Figure 2. Failures in Time vs Junction Temperature

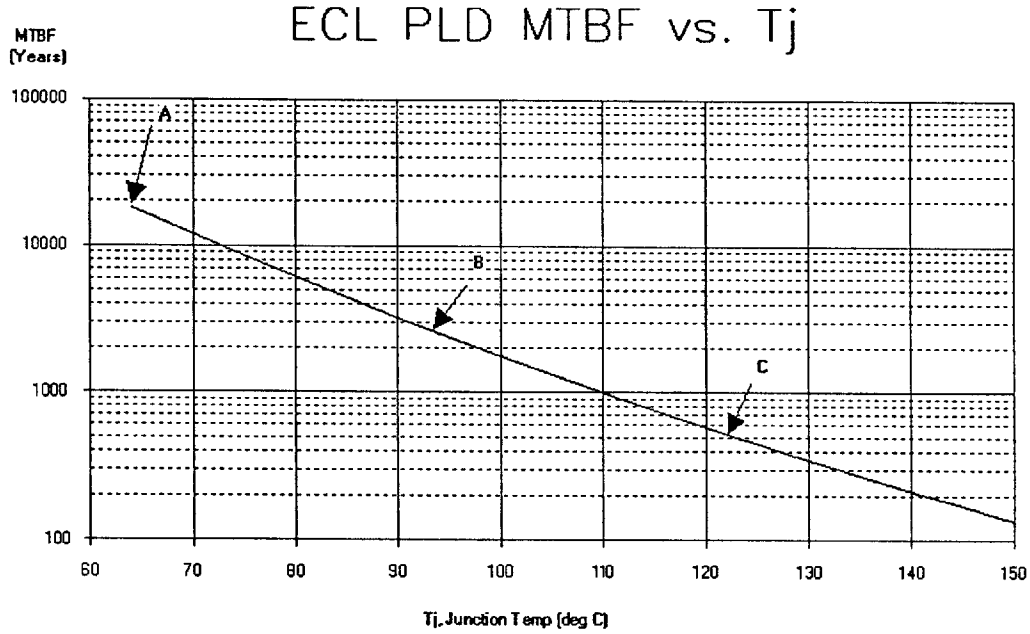


Figure 3. Mean Time Between Failures vs Junction Temp.

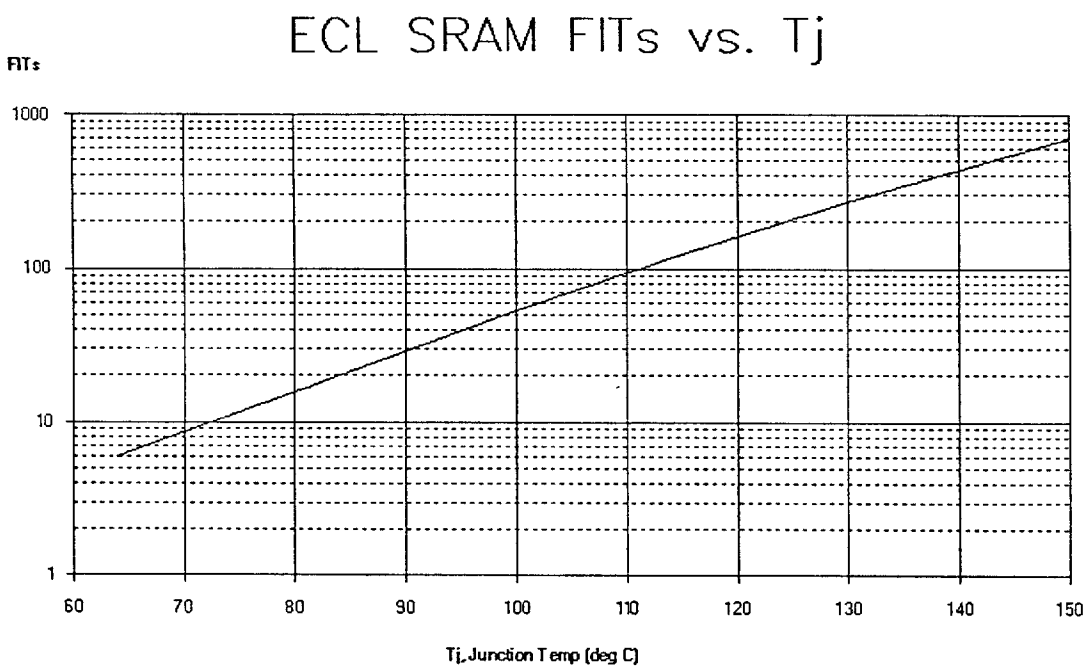


Figure 4. Failures in Time vs Junction Temperature

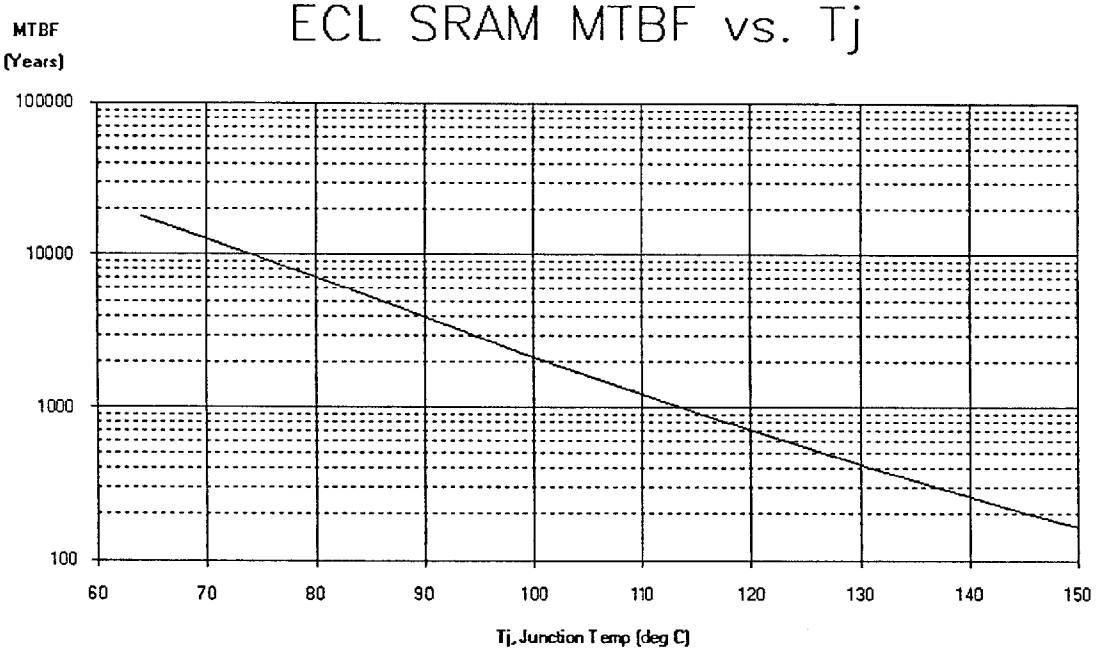


Figure 5. Mean Time Between Failure vs Junction Temp.