



CYPRESS

CYM9288/CYM9289

512K/1M x 72 Flowthrough NoBL SRAM Module

Features

- Operates at 66 MHz
- Uses 256K/512K x 18 high performance Flowthrough NoBL synchronous SRAMs
- 3.3V data inputs/outputs

Functional Description

The CYM9288/9289 are high-performance synchronous Flowthrough NoBL memory modules organized as 512K/1M by 72 bits. These modules are constructed from 256K/512K x 18 NoBL SRAM's in plastic surface mount packages on an

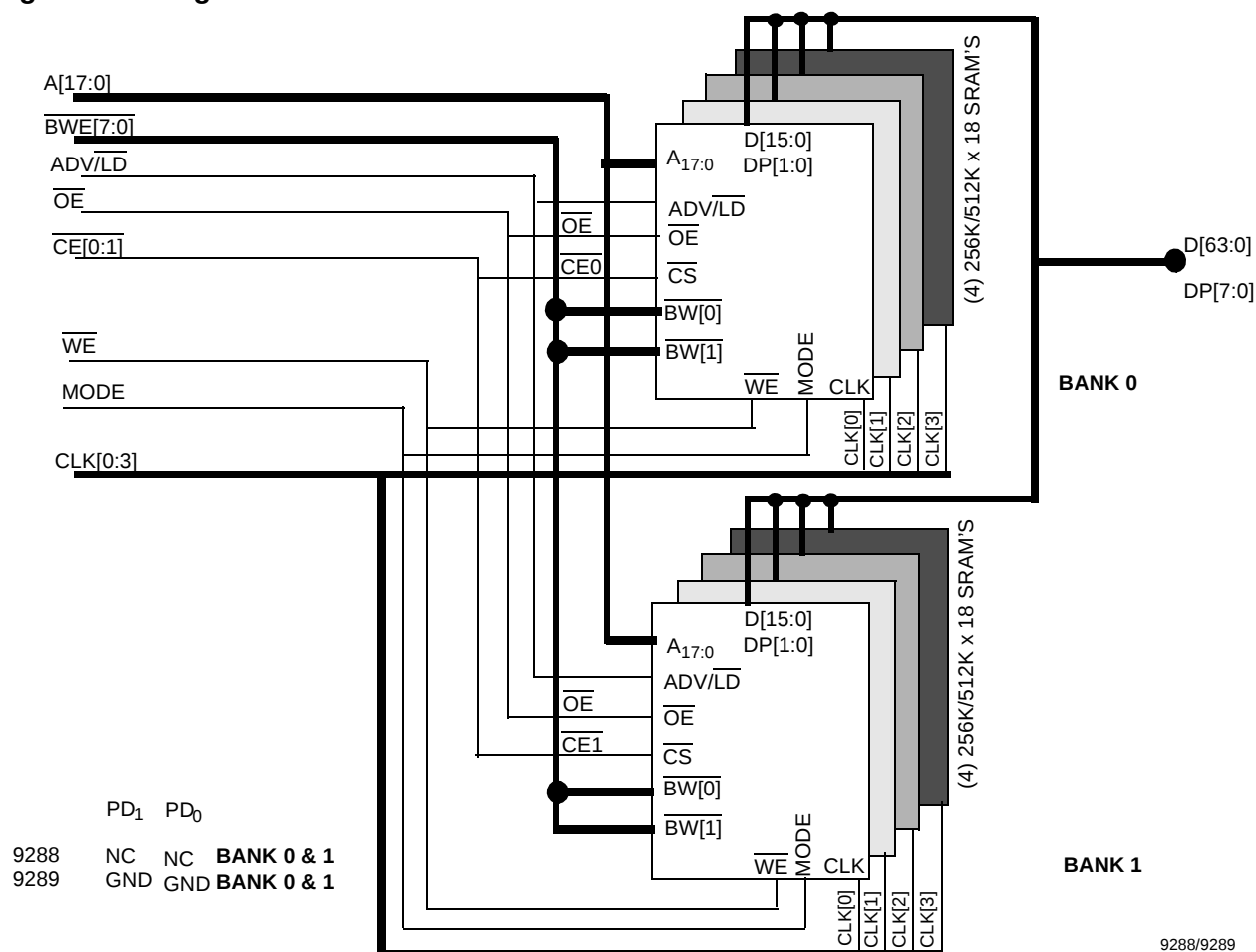
epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

Modules are configured as either one or two banks, where each bank has separate chip select controls. Separate clocks are provided for every pair of SRAMs.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 200 micro-inches (minimum) of 90/10 tin/lead over 50 micro-inches of nickel.

Logic Block Diagram - CYM9288/9289



9288/9289

Selection Guide

	NoBL Synchronous Module			
Part Number	CYM9288-60	CYM9288-66	CYM9289-60	CYM9289-66
Cache Size	512 K x 72	512 K x 72	1M x 72	1M x 72
SRAMs Used	8 of 256K x 18	8 of 256K x 18	8 of 512K x 18	8 of 512K x 18
System Clock (MHz)	60	66	60	66
Data t_{CDV}	12 ns	10.5 ns	12 ns	10.5 ns

Pin Configuration

Dual Read-Out ZIP Top View			
GND	1	85	GND
D63	2	86	DP7
D62	3	87	D61
Vcc3	4	88	GND
D60	5	89	D59
D58	6	90	D57
GND	7	91	GND
D56	8	92	DP6
D55	9	93	D54
GND	10	94	Vcc3
D53	11	95	D52
D51	12	96	D50
GND	13	97	GND
D49	14	98	D48
DP5	15	99	D47
Vcc3	16	100	GND
D46	17	101	D45
D44	18	102	D43
GND	19	103	GND
D42	20	104	D41
D40	21	105	DP4
GND	22	106	Vcc3
D39	23	107	D38
D37	24	108	D36
GND	25	109	GND
D35	26	110	D34
D33	27	111	D32
GND	28	112	GND
CLK3	29	113	CLK2
GND	30	114	GND
DP3	31	115	D31
D30	32	116	D29
Vcc3	33	117	GND
D28	34	118	D27
D26	35	119	D25
GND	36	120	GND
D24	37	121	DP2
D23	38	122	D22
GND	39	123	Vcc3
D21	40	124	D20
D19	41	125	D18
GND	42	126	GND
D17	43	127	D16
DP1	44	128	D15
Vcc3	45	129	GND
D14	46	130	D13
D12	47	131	D11
GND	48	132	GND
D10	49	133	D9
D8	50	134	DP0
GND	51	135	Vcc3
D7	52	136	D6
D5	53	137	D4
GND	54	138	GND
D3	55	139	D2
D1	56	140	D0
PD0	57	141	PD1
MODE	58	142	A19
A18	59	143	A17
A20	60	144	GND
A16	61	145	A15
A14	62	146	A13
GND	63	147	Vcc3
A12	64	148	A11
A10	65	149	A9
GND	66	150	GND
A8	67	151	A7
A6	68	152	A5
Vcc3	69	153	GND
A4	70	154	A3
A2	71	155	A1
A0	72	156	ADV/LD
GND	73	157	GND
CLK1	74	158	CLK0
GND	75	159	GND
BWE7	75	160	BWE6
BWE5	77	161	BWE4
GND	78	162	GND
BWE3	79	163	BWE2
BWE1	80	164	BWE0
GND	81	165	Vcc3
WE	82	166	OE
CE1	83	167	CE0
GND	84	168	GND

Pin Definitions

Signal	Description
V _{CC3}	3.3V supply
GND	Ground
A[20:0]	Addresses from processor
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{BWE}[7:0]$	Byte Write Enables
$\overline{CS}[1:0]$	Chip Select for the two banks
PD ₀ –PD ₁	Presence Detect output pins
D[63:0]	Data lines from processor
DP[7:0]	Data Parity lines from processor
CLK[0:3]	Clock lines to the module
ADV/ $\overline{LD}$	Advance Load Signal from processor
Mode	Mode pin for Burst Selection
NC	Signal not connected on module
RSVD	Reserved

Presence Detect Pins

	PD ₁	PD ₀
CYM9288 - 512K x 72	NC	NC
CYM9289 - 1M x 72	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to $+125^{\circ}\text{C}$

Ambient Temperature
with Power Applied 0°C to $+70^{\circ}\text{C}$

Supply Voltage to Ground Potential -0.5V to $+4.5\text{V}$

DC Voltage Applied to Outputs
in High Z State -0.5V to $+4.6\text{V}$

DC Input Voltage -0.5V to $+4.6\text{V}$

Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$3.3\text{V} \pm 5\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		-0.3	0.8	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -4 \text{ mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 8 \text{ mA}$		0.4	V
I_{CC} (9288)	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$		2400	mA
I_{CC} (9289)	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$		2400	mA

Capacitance^[1]

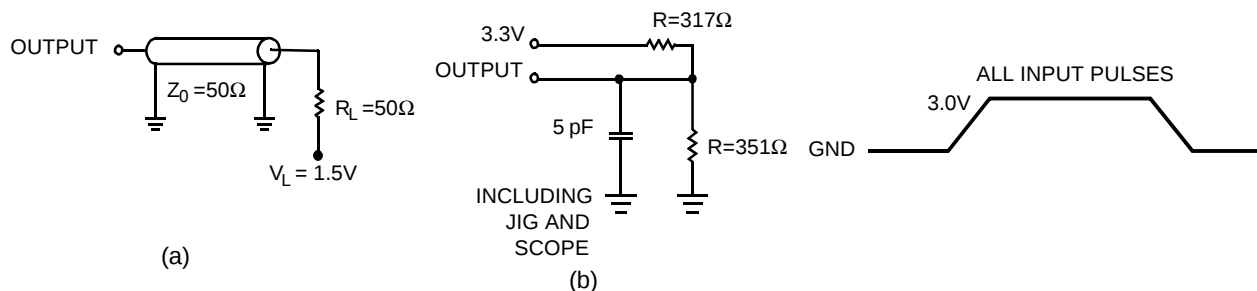
Parameter	Description	Test Conditions	Max.	Unit
C_A	Address Input Capacitance	$T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3\text{V}$	48	pF
C_I	Control Input Capacitance	$T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3\text{V}$	48	pF
C_O	Input/Output Capacitance	$T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3\text{V}$	16	pF
C_{CLK}	Clock Capacitance	$T_A = 25^{\circ}\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3\text{V}$	12	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

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AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range^[2]

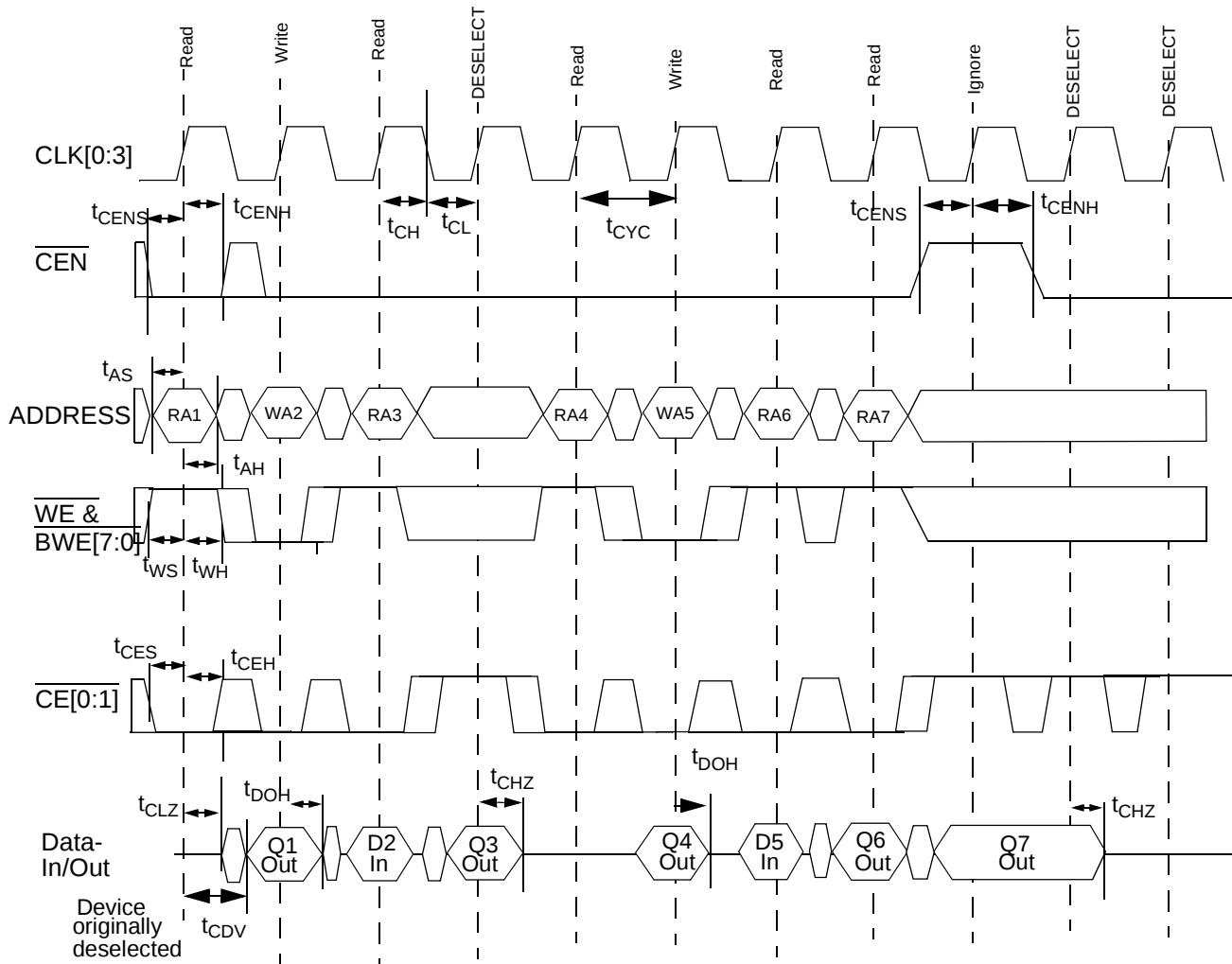
Parameter	Description	60		66		Unit
		Min.	Max.	Min.	Max.	
Clock						
t _{CYC}	Clock Cycle Time	16.6		15.0		ns
F _{MAX}	Maximum Operating Frequency		60		66	MHz
t _{CH}	Clock HIGH	6.0		5.0		ns
t _{CL}	Clock LOW	6.0		5.0		ns
Output Times						
t _{CDV}	Data Output Valid After CLK Rise		12		10.5	ns
t _{EOV}	$\overline{OE}$ LOW to Output Valid ^[3, 5]		6		6	ns
t _{DOH}	Data Output Hold After CLK Rise	1.5		1.5		ns
t _{CHZ}	Clock to High-Z ^[3, 4, 5]		5.0		5.0	ns
t _{CLZ}	Clock to Low-Z ^[3, 4, 5]	3.0		2.0		ns
t _{EOHZ}	$\overline{OE}$ HIGH to Output High-Z ^[3, 4, 5]		6.0		6.0	ns
t _{EOLZ}	$\overline{OE}$ LOW to Output Low-Z ^[3, 4, 5]	0		0		ns
Setup Times						
t _{AS}	Address Set-Up Before CLK Rise	2.5		2.0		ns
t _{DS}	Data Input Set-Up Before CLK Rise	2.5		2.0		ns
t _{WES}	$\overline{WE}$, $\overline{BWE}_{[7:0]}$ Set-Up Before CLK Rise	2.5		2.0		ns
t _{ALS}	$ADV/\overline{LD}$ Set-Up Before CLK Rise	2.5		2.0		ns
t _{CES}	Chip Selects Set-Up	2.5		2.0		ns
Hold Times						
t _{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t _{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t _{WEH}	$\overline{WE}$, $\overline{BWE}_{[7:0]}$ Hold After CLK Rise	0.5		0.5		ns
t _{ALH}	$ADV/\overline{LD}$ Hold after CLK Rise	0.5		0.5		ns
t _{CEH}	Chip Selects Hold After CLK Rise	0.5		0.5		ns

Notes:

- AC test conditions assume signal transition time of 2 ns or less, timing reference levels, input pulse levels and output loading shown in part (a) of AC Test Load for 3.3V devices and (c) for 2.5V devices.
- t_{CHZ} , t_{CLZ} , t_{EOV} , t_{EOLZ} , and t_{EOHZ} are specified with AC test conditions shown in part (a) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
- At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
- This parameter is sampled and not 100% tested.

Switching Waveforms

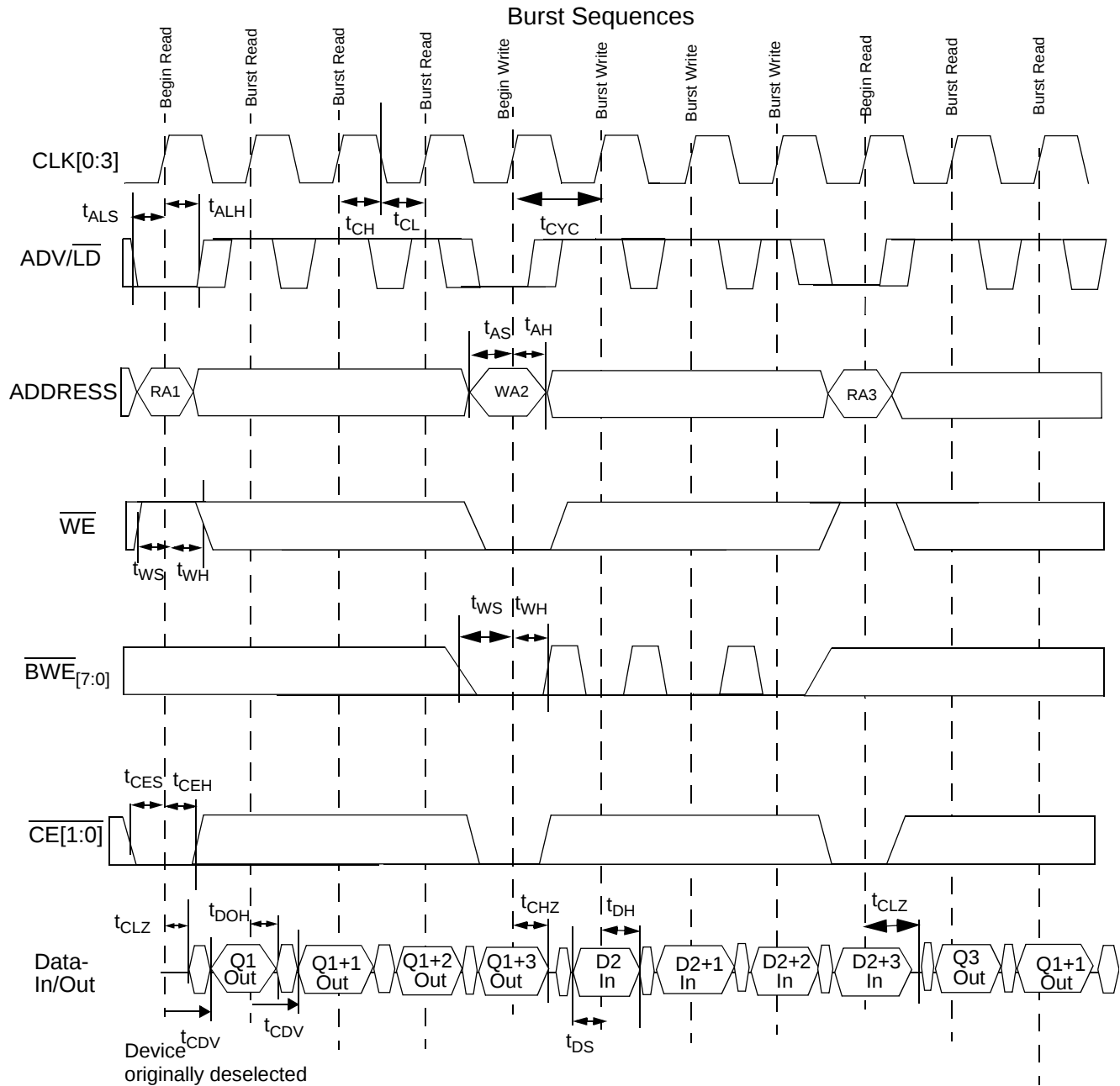
Read/Write/Deselect Timing



$\overline{WE}$ is the combination of $\overline{WE}$ & $\overline{BWE}_x$ to define a write cycle (see Write Cycle Description table).

RAx stands for Read Address X, WAx stands for Write Address X, Dx stands for Data-in X, Qx stands for Data-out X.

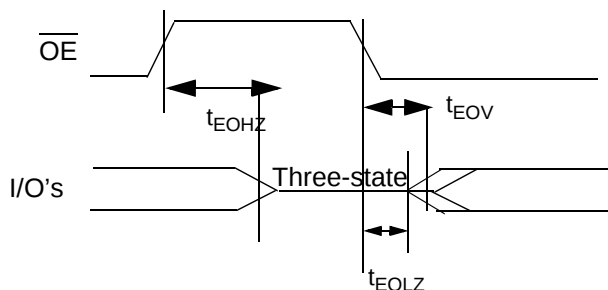
= DON'T CARE = UNDEFINED

Switching Waveforms (continued)
Read/Write/Deselect Timing


The combination of $\overline{WE}$ & $\overline{BWE}_{[7:0]}$ define a write cycle.

RAx stands for Read Address X, WAx stands for Write Address X, Dx stands for Data-in for location X, Qx stands for Data-out for location X. $\overline{CEN}$ held LOW. During burst writes, byte writes can be conducted by asserting the appropriate $\overline{BWE}_{[7:0]}$ input signals. Burst order determined by the state of the Mode input. $\overline{CEN}$ held LOW. $\overline{OE}$ held LOW.

□ = DON'T CARE □ = UNDEFINED

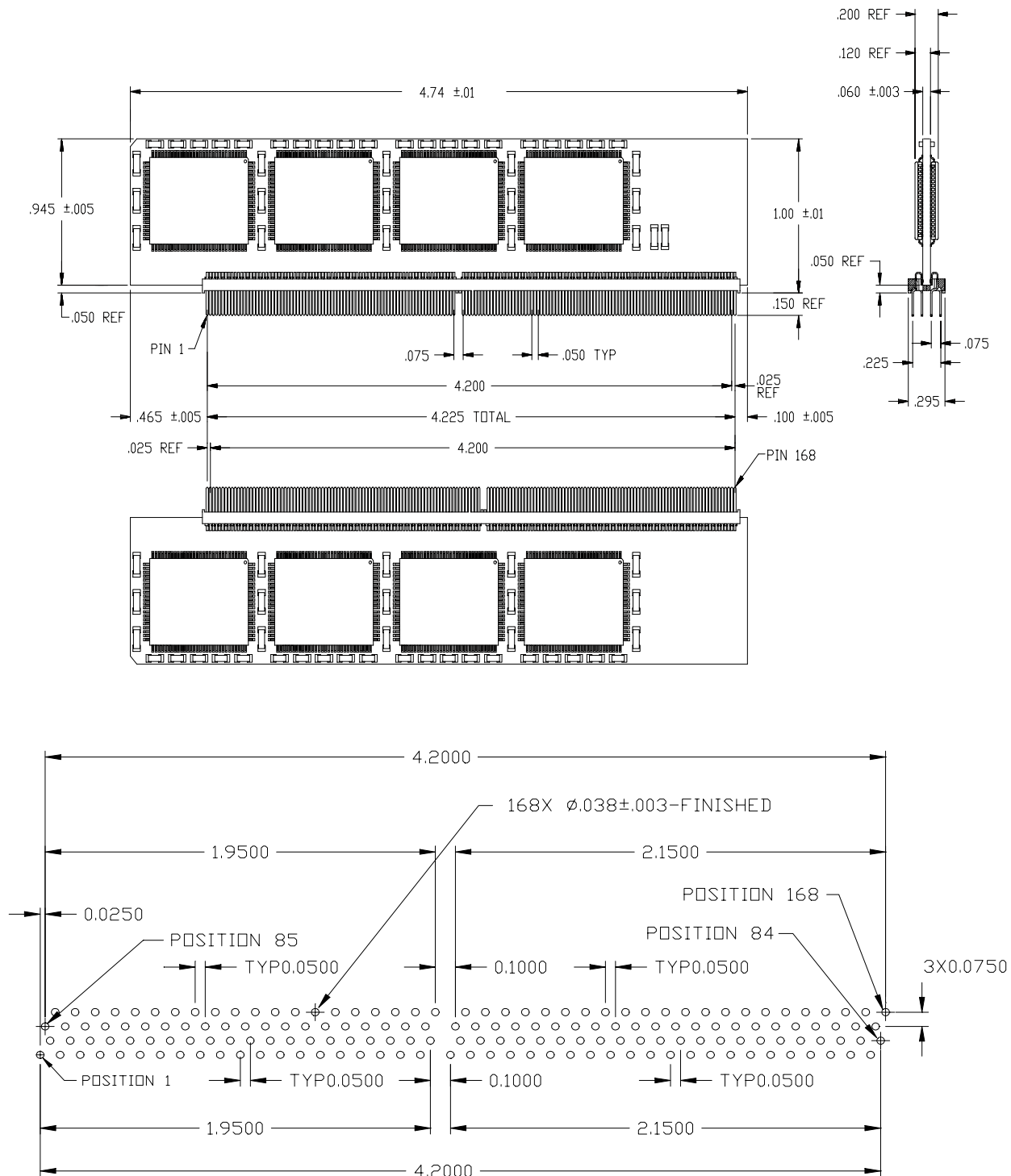
Switching Waveforms (continued)
 $\overline{\text{OE}}$ Timing

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM9288APZ-60C	PZ12	168-Pin Quad-Row ZIP	Flowthrough NoBL 512K x 72	Commercial
66	CYM9288APZ-66C			Flowthrough NoBL 512K x 72	
60	CYM9289BPZ-60C	PZ12	168-Pin Quad-Row ZIP	Flowthrough NoBL 1M x 72	Commercial
66	CYM9289BPZ-66C			Flowthrough NoBL 1M x 72	

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PZ12: 168 Pin Quad Row ZIP Module



RECOMMENDED HOST CARD LAYOUT (COMPONENT SIDE)