8Mx72 bits
PC100/PC133 SDRAM Registered DIMM

based on 8Mx8 SDRAM with LVTTL, 4 banks & 4K Refresh

GMM2739230EPTG

Description

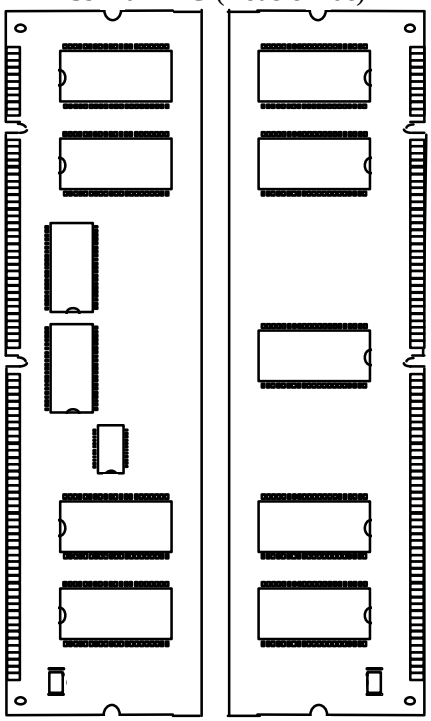
The GMM2739230EPTG is a 8M x 72bits Synchronous Dynamic RAM MODULE which is assembled 9 pieces of 8M x 8bits Synchronous DRAMs in 54 pin TSOP II package, 2 pieces of 16 bits Register in 48 pin TSSOP package, one clock distribution PLL in 24 pin SOP and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2739230EPTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2739230EPTG provides common data inputs and outputs.

Features

* PC133/PC100/PC66 Compatible
  -7(143MHz)/-75(133MHz)/8(125MHz)
  -7K(PC100,2-2-2)/7J(PC100,3-2-2)
* 3.3V +/- 0.3V Power supply
* Maximum Clock frequency
  100/125/133/143 MHz
* LVTTL Interface
* Burst read/write operation and burst read/ single write operation capability
* Programmable burst length ;
  1, 2, 4, 8, Full page
* Programmable burst sequence
  Sequential / Interleave
* Full Page burst length capability
  Sequential burst
  Burst stop capability
* Programmable $\overline{CAS}$ Latency ; 2, 3
* CKE power down mode
* Input / Output data masking
* 4096 Refresh Cycles / 64ms
* Auto refresh / Self refresh Capability
* Serial Presence Detect with EEPROM

GMM2739230EPTG (Double Side)



(Top) (Bottom)

Pin Name

CK0, 1, 2, 3	Clock input
CKE0	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
REGE	Register Enable
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
WP	Write Protect for SPD
DU	Don't Use

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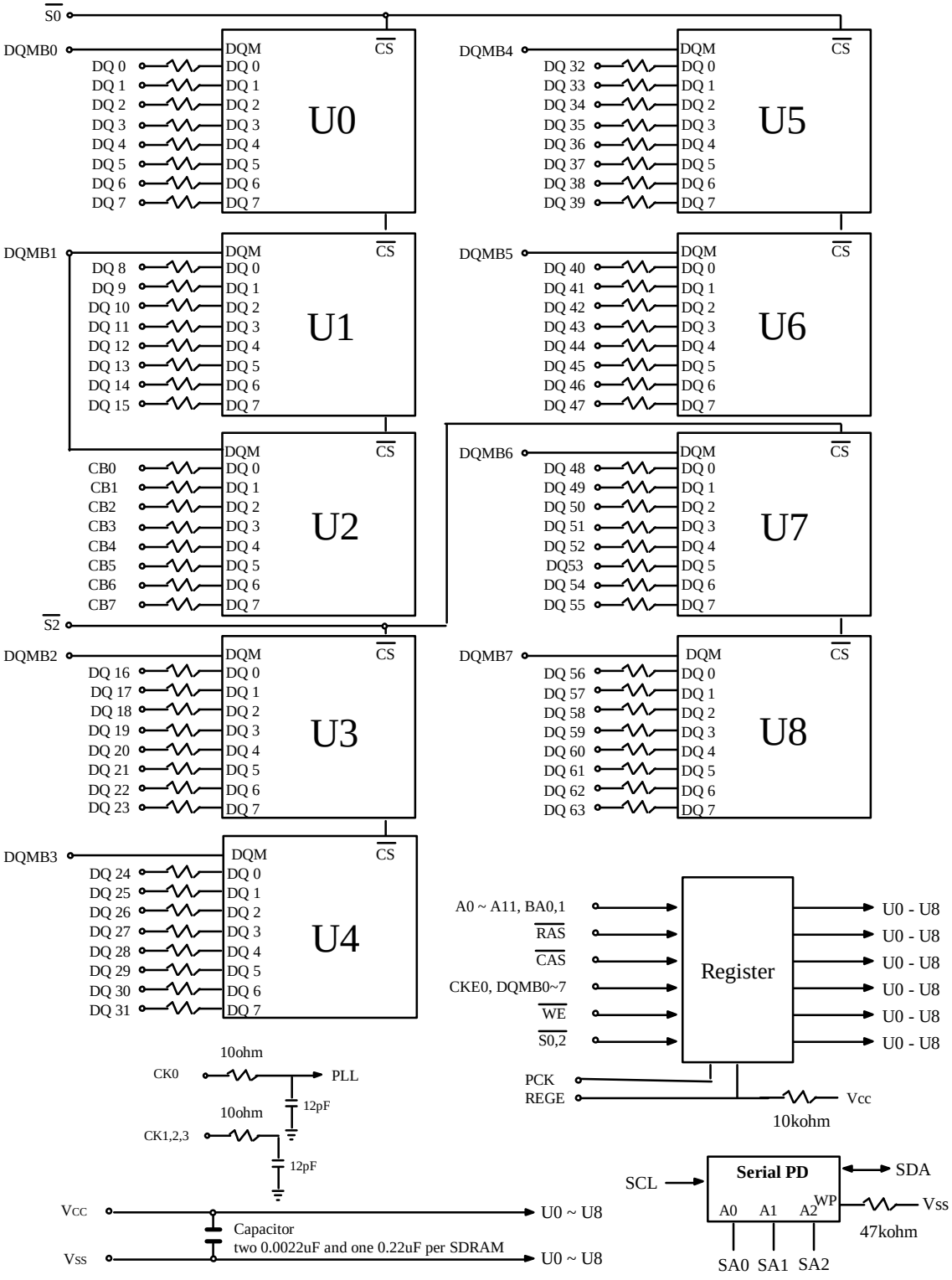
Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	29	DQMB1	57	DQ18	85	V_{SS}	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	V_{CC}	87	DQ33	115	$\overline{RAS}$	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	*V_{REF}, NC	90	V_{CC}	118	A3	146	*V_{REF}, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	V_{CC}	101	DQ45	129	$\overline{*S3}$	157	V_{CC}
18	V_{CC}	46	DQMB2	74	DQ28	102	V_{CC}	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	V_{CC}	77	DQ31	105	CB4	133	V_{CC}	161	DQ63
22	CB1	50	NC	78	V_{SS}	106	CB5	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CK2	107	V_{SS}	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	V_{CC}	54	V_{SS}	82	SDA	110	V_{CC}	138	V_{SS}	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	V_{CC}	112	DQMB4	140	DQ49	168	V_{CC}

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0, 2 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs. Data is not latched in the register.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC}	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS}	Ground is connected. (V_{SS} is for the internal circuit)
REGE (register enable pin)	If REGE input is high, permits the DIMM to operate in `registered mode`. If REGE input is low, permits the DIMM to operate in `buffered mode`.
NC	No Connection pins.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to Vcc+0.5 (<=4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	C	
Storage temperature	Tstg	-55 to +125	C	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70 C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1,3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.6V for pulse width <=3ns

3. V_{IL} (min) = -2.0V for pulse width <=3ns

Registered DIMM Operation

1. All control and address signals are registered on-DIMM register and hence delayed by one cycle in arriving at the SDRAMs. But data is not registered in the register.

2. CAS latency defines the delay from when a READ command is registered on a rising clock edge to when the data from that READ command becomes available at the outputs. Do not confuse DIMM CAS latency with the SDRAM CAS latency which is one clock less.

DC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ}= 0 V)

Parameter		Symbol	- 7	- 75	- 8	-7K	-7J	Unit	Test conditions	Notes
			Max	Max	Max	Max	Max			
Operating current		I_{CC1}	760	760	720	720	720	mA	Burst length= 1 t_{RC} = min	1, 2, 3
Standby current in power down		I_{CC2P}	20	20	20	20	20	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	20	20	20	20	20	mA	CKE=V_{IL}, t_{CK}= infinity	6
Standby current in non power down (CAS Latency=2)		I_{CC2N}	150	150	150	150	150	mA	CKE,CS = V_{IH}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	50	50	50	50	50	mA	CKE = V_{IH}, t_{CK} = infinity	4
Active standby current in power down		I_{CC3P}	60	60	60	60	60	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	50	50	50	50	50	mA	CKE = V_{IL}, t_{CK} = infinity	2,6
Active standby current in non power down		I_{CC3N}	300	300	300	300	300	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	200	200	200	200	200	mA	CKE = V_{IH}, t_{CK} = infinity	2,8
Burst operating current	(CL= 2)	I_{CC4}	1100	1100	1100	1100	1100	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	1400	1400	1400	1100	1100	mA		
Refresh current		I_{CC5}	1000	1000	1000	1000	1000	mA	t_{RC} = min	3
Self refresh current		I_{CC6}	10	10	10	10	10	mA	V_{IH} >=V_{CC} - 0.2 V_{IL} <=0.2V	7

Parameter	Symbol	- 7, - 75, - 8, - 7K, - 7J		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	I_{LI}	-1	1	u A	0 <=Vin <=V_{CC}	
Output leakage current	I_{LO}	-1.5	1.5	u A	0 <=Vout <=V_{CC} DQ = disable	
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.

2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After Power down mode, CLK operating current.
6. After Power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25C, V_{CC}, V_{CCQ} = 3.3V +/- 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A11, BA0, BA1)	7	10	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0)	15	17	pF	1, 3
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	33	35	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$,$\overline{S2}$)	7	10	pF	1, 3
C_{I6}	Input capacitance (DQMB0,1,2,3,4,5,6,7)	7	38	pF	1, 3
$C_{I/O}$	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	7	14	pF	1, 2, 3

Note :
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70 C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-75		-8		-7K		-7J		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	10	-	10	-	10	-	10	-	15	-	ns	1
	(CL=3)	t_{CK}	7	-	7.5	-	8	-	10	-	10	-		
CLK high pulse width		t_{CKH}	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	6	-	6	-	6	-	6	-	8	ns	1, 2
	(CL=3)	t_{AC}	-	5.4	-	5.4	-	6	-	6	-	6		
Data-out hold time		t_{OH}	2.7	-	2.7	-	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedance		t_{LZ}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2,3)		t_{HZ}	-	5.4	-	5.4	-	6	-	6	-	6	ns	1, 4
Data-in setup time		t_{DS}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	62	-	65	-	68	-	70	-	70	-	ns	1
Active to Precharge command period		t_{RAS}	42	120000	45	120000	48	120000	50	120000	50	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	20	-	20	-	20	-	20	-	ns	1
Precharge to active command period		t_{RP}	20	-	20	-	20	-	20	-	20	-	ns	1

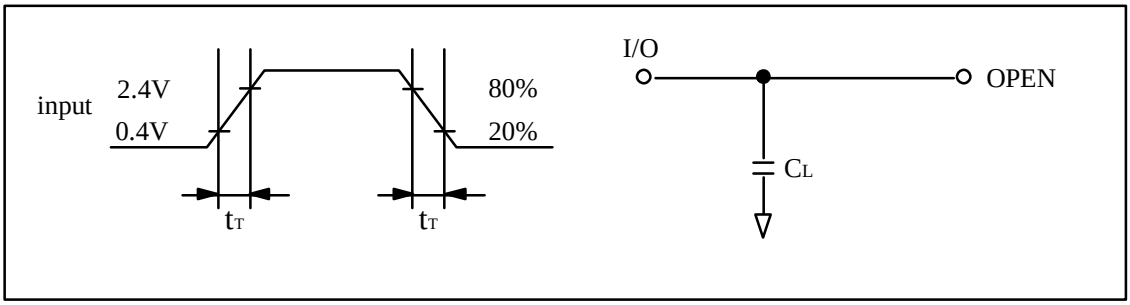
AC Characteristics (Ta = 0 to 70 C, V_{CC}, V_{CCQ} = 3.3 V +/ -0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	- 7		- 75		- 8		- 7K		- 7J		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	7	-	7.5	-	8	-	10	-	10	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	15	-	16	-	20	-	20	-	ns	1
Refresh period	t_{REF}	-	64	-	64	-	64	-	64	-	64	ms	
PLL Stabilization time	t_{STAB}	200	-	200	-	200	-	200	-	200	-	us	6

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V. If t_T is longer than 1ns,transition time compensation should be considered.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (min)defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.
5. t_{CES} define CKE setup time to CKE rising edge except Power down exit command.
6. The on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.

Test Condition

? Input and output-timing reference levels: 1.4V
? Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-75		-8		-7K		-7J		Notes
frequency(MHz)			143	100	133	100	125	100	100	100	100	66	
t_{CK} (ns)			7	10	7.5	10	8	10	10	10	10	15	
Active command to column command (same bank)		l_{RCD}	3	2	3	2	3	2	2	2	2	2	1
Active command to active command (same bank)		l_{RC}	9	7	9	7	9	7	7	7	7	6	= [l_{RAS} +l_{RP}], 1
Active command to Precharge command (same bank)		l_{RAS}	6	5	6	5	6	5	5	5	5	4	1
Precharge command to active command (same bank)		l_{RP}	3	2	3	2	3	2	2	2	2	2	1
Write recovery or last data-in to Precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	1	1	1	1	1	2	1	1	1	2	
Last data in to active command (Auto Precharge, same bank)		l_{APW}	4	3	4	3	4	3	3	3	3	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	7	9	7	9	7	7	7	7	6	= [l_{RC}]
Precharge command to high impedance	(CL=2)	l_{HZP}	-	2	-	2	-	2	2	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	3	3	3	3	
Last data out to active command (auto Precharge) (same bank)		l_{APR}	1	1	1	1	1	1	1	1	1	1	
Last data out to Precharge (early Precharge)	(CL=2)	l_{EP}	-	-1	-	-1	-	-1	- 1	- 1	-	-1	
	(CL=3)	l_{EP}	-2	-2	-2	-2	-2	-2	- 2	- 2	- 2	- 2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	1	1	1	1	

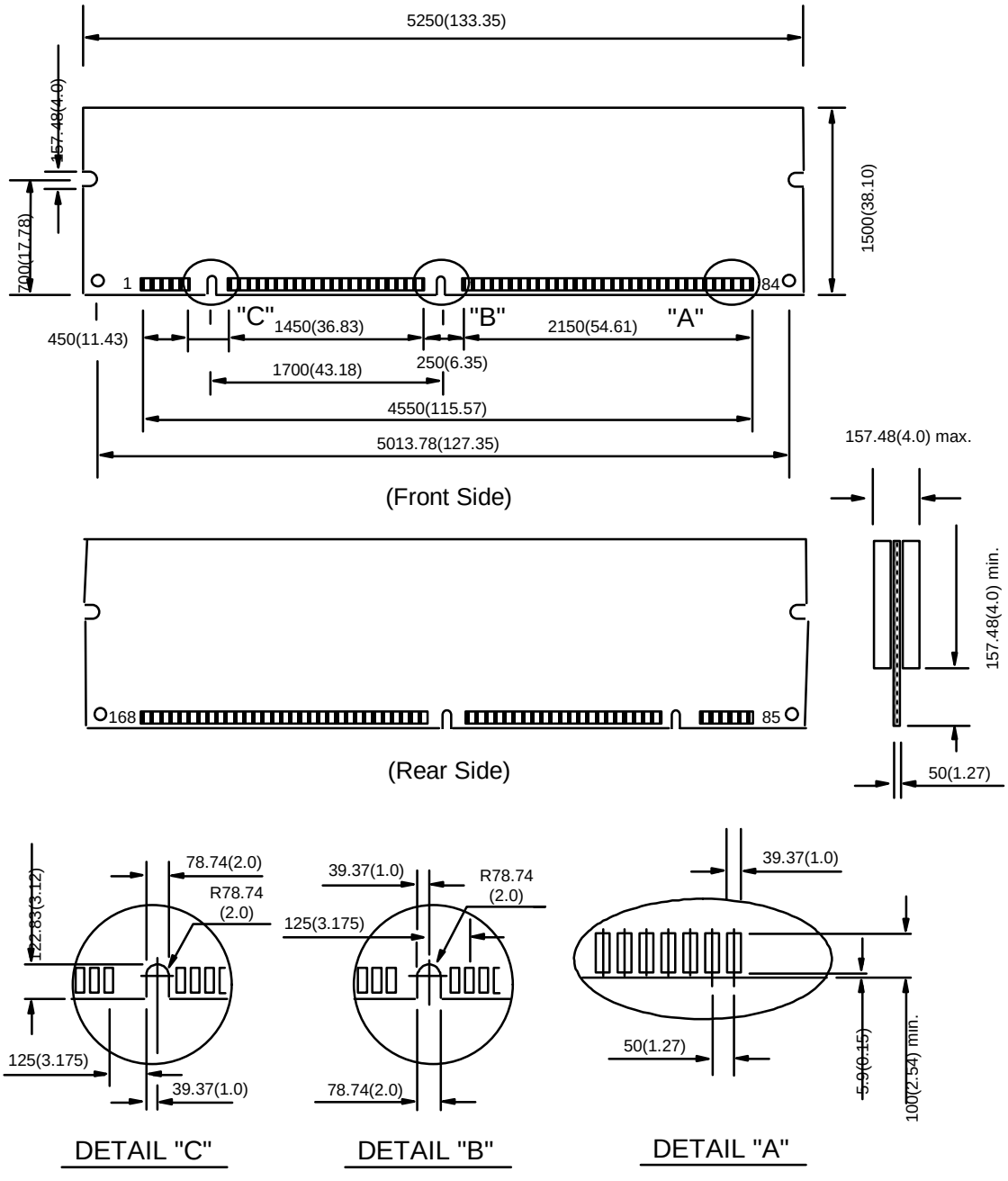
Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-75		- 8		- 7K		- 7J		Notes
frequency(MHz)			143	100	133	100	125	100	100	100	100	66	
t_{CK} (ns)			7	10	7.5	10	8	10	10	10	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	1	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	l_{BSH}	-	2	-	2	-	2	2	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	0	0	0	0	

Notes : 1. l_{RCD} to l_{RRD} are recommended value.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions +/-5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.